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A negative voltage generator with 4-Stage configurable parallel switching for smart window film applications

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ABSTRACT

A negative voltage generator was developed that can be used in the drivers of smart window films (SWF), which have typical operating voltages of ±8 to ±10 V. It consists of four Negative Charge Pump (NCP) stages and a 4-phase non-overlapping Clock Generator (CG), where the 4 NCP stages are configurable by external digital signals. This generates a wide output voltage range necessary to control different SWF modes, such as opaque, transparent, and tinted modes. TSMC 0.18-μm HV BCD (High-Voltage Bipolar-CMOS-DMOS) process was used to fabricate the proposed negative voltage generator on silicon. Measurement results demonstrate that at switching frequency (fsw) = 20 MHz, supplied voltage (VDD) = 4.5 V and Vin = GND, it generates a wide output voltage range of −3.9 to −14.0 V, achieving the widest voltage range among the prior works, which covers the required negative voltage range for SWF usage. The peak efficiency is measured on silicon to be 58.08% .

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HV BCD; charge pump; 4-phase clocking; negative voltage generation; stage-configurable; smart window film

1. Introduction

In many so-called green buildings, electrochromic windows have been extensively employed to demonstrate several modes based on the need or availability of sunlight. For example, when the sunshine is intense, the window may be shut or closed to offer a shield to withstand the sun's rays, allowing the internal temperature to remain relatively constant. In most cases, a thin film covers the surface of this form of window, with a liquid crystal sandwiched between layers in the centre of the film (Shim et al., 2017). If the proper voltages are supplied to this crystal, it will become polarised. A thin film called smart window film (SWF) requires digital driving signals with ±8 to ±10 V swings to function properly. By using SWF, the window can function in different modes, such as opaque (privacy mode), tinted (limited shade), and clear (transparent). However, some problems arise during the SWF's operation. One of these problems is the image-sticking effect that damages the SWF function. The image-sticking effect, which affects the SWF due to its

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residue voltage, can be prevented by generating negative voltages, i.e. the reverse of the polarity of the digital driving voltage swings. This fact demands that negative voltage signals be generated internally, provided that the power supply voltage is positive.

However, despite the fact that there are numerous negative voltage generators in the literature, they were not intended for integration and interfacing with restricted, inconsistent, and variable output voltage generators, such as photovoltaic cells, e.g. (Allen Madrigal et al., 2019; Deng, 2006; Gratela et al., 2019; Lakkas, 2016; T.-J. Lee et al., 2020; Tolentino et al., 2015; Wang, Jose, et al., 2021), piezoelectrics, e.g. (Fernandez et al., 2018; Wang et al., 2020; Wang, Tolentino, et al., 2021), and thermoelectrics, e.g. (Salvador & Sangalang, 2021). Although DC-DC converters can carry out the generation of negative voltages, an external negative reference voltage is required to perform the necessary generation (Kuo et al., 2011; Wang et al., 2011). Low driving current, poor efficiency, and limited voltage swing are exhibited by most of the previous CPs, making them inappropriate for SWF applications entirely (Aloulou et al., 2016; J.-C. Lee & Chung, 2010). However, capacitor-based charge pumps (CP), on the other hand, are more suitable for integrating and interfacing with solar cells, which is mostly required in SWF applications (Alameh et al., 2016; Hongchin & Chen, 2001; Lin & Ker, 2018, 2020; Patil et al., 2020; Racape & Daga, 2005). To eliminate the residual voltage of the SWF's prior condition, −8 to −10 V voltages should be generated, though this is a crucial element of the process. A 3-stage charge pump proposed by (Luo et al., 2019) may be a possible solution since it has output voltages ranging from 3 to 12.6 V and 3 to 10.8 V at output currents of 0.5 mA and 3.5 mA, respectively. However, a negative voltage is not generated.

A selectable order negative voltage charge pump architecture for biomedical applications, as shown in Fig. 0, proposes a switch (SW) and a bypass path that can switch on the negative voltage charge pump, which is characterised by the negative voltage charge pump at each stage (Lin & Ker, 2020). As shown in Figure 1, its opening sequence is as follows: path A → path B → path C → path D. When closing, it must be closed in reverse order: path D → path C → path B → path A. This means that it cannot be used to generate any negative voltage because its on-and-off sequence is fixed.

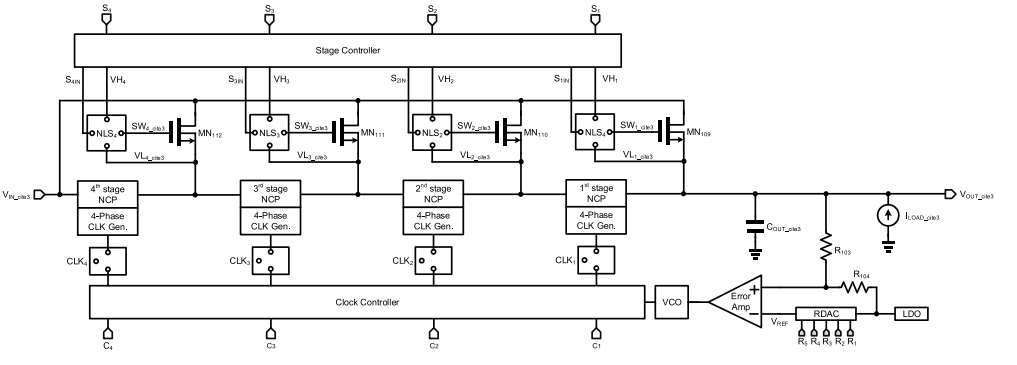


Figure 1. Selectable voltage charge pump architecture (Lin & Ker, 2020).

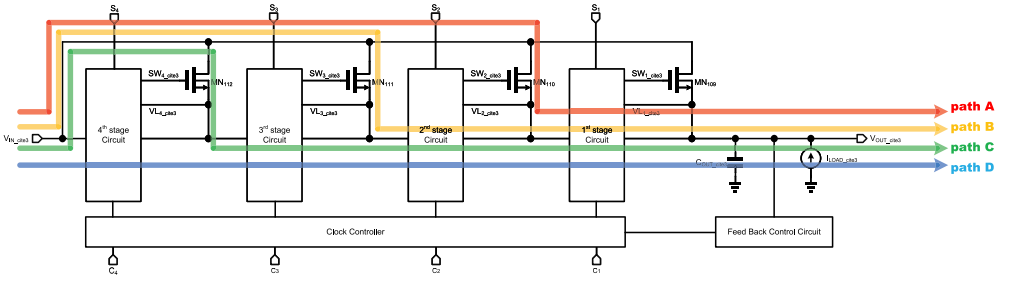


Figure 2. Selectable voltage charge pump's simplified diagram showing its bypass paths (Lin & Ker, 2020).

The prior work is both voltage- and current-limited, i.e. −0.3 to −9.3 V, which is not suitable for SWF (Lin & Ker, 2020). For this reason, a 4-stage CP-based negative voltage generator for SWF applications is presented in this paper as shown in Figure 2. It can be activated using parallel bypass switches, resulting in short settling time and lower switching loss. This removes the need for the resistive digital-to-analog converter (RDAC) used in the prior works (Lin & Ker, 2020; Luo et al., 2019), which dictates the output voltage of its error amplifier. Moreover, the proposed design does not require a Stage Controller that refines the switches' external digital signals and converts them into internal control signals. Notably, in our proposed system, the drain of MN4 is directly connected to Vin, and the drains of MN3, MN2, and MN1 are connected to the sources of the prior devices MN4, MN3, and MN2, respectively, which is not the same as the connections reported in (Lin & Ker, 2020). Finally, as shown in Figure 4, each stage of the Negative Charge Pump (NCP) is an independent operating stage, i.e. it can be randomly configurable. For example, Stage 1 → Stage 3 → Stage 2 → Stage 4. To turn on the 2nd Stage NCP, starting the 1st Stage first is unnecessary. Namely, the proposed Negative Voltage Generator is

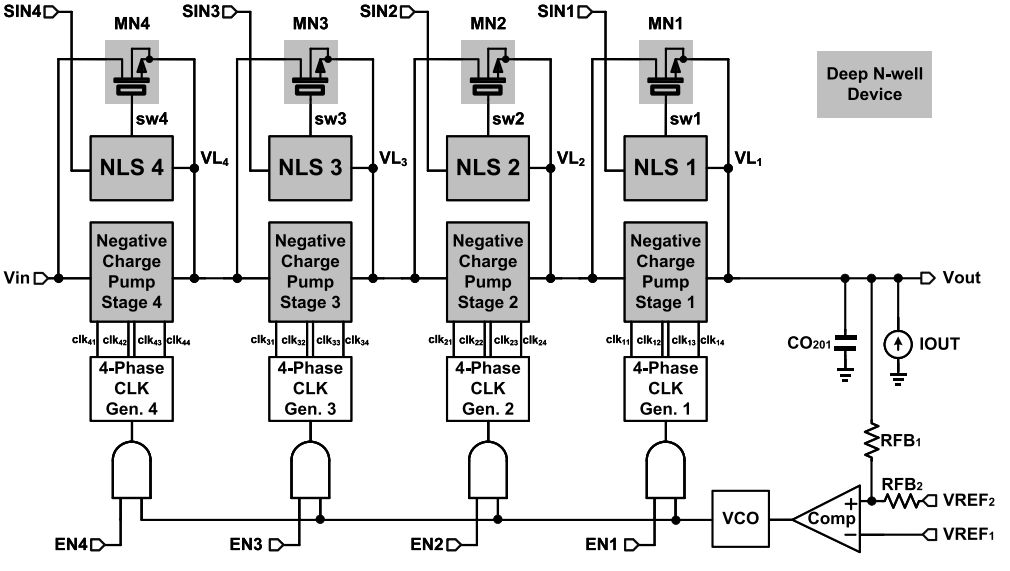


Figure 3. Proposed negative voltage generator's block diagram.

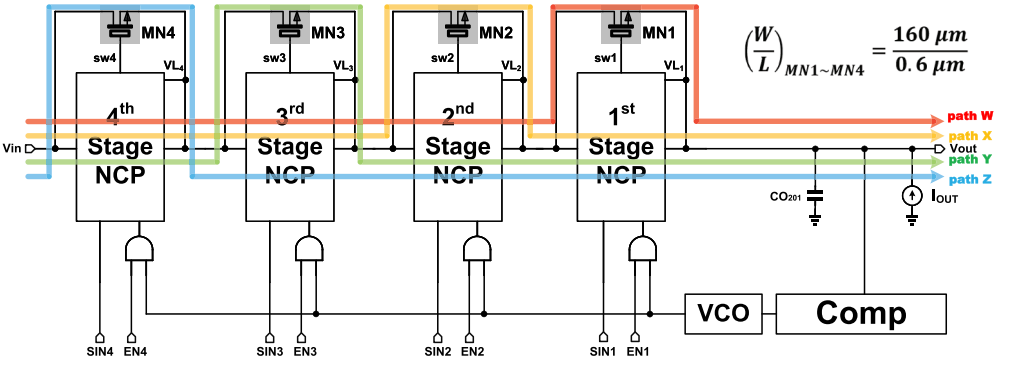


Figure 4. Proposed negative voltage generator's simplified diagram showing its bypass paths.

equipped with bypass switches that can be configured individually, allowing the selection of stages in any sequence. Finally, it was fabricated using the High Voltage (HV) BCD (Bipolar-CMOS-DMOS) process, which makes use of a Deep P-well and N+ Buried Layer/HV Deep N-well providing complete isolation between negative voltage layers and the ground (p-substrate), allowing for the generation of reliable negative voltages.

This paper is organised as follows: Section 2 presents the system architecture of the proposed wide range negative voltage generator architecture; Post-layout simulations proving the random configuration of the proposed system are presented in Section 3; Section 4 discusses the realisation and measurement results of the proposed design on the prototype chip; Finally, Section 5 concludes this study.

2. Wide voltage-range negative voltage generator architecture

The cause of the SWF image-sticking effect is demonstrated in Figure 5, where an organic light-emitting diode (OLED) driver circuit's supplied voltage (VDD) is intended for the said OLED to be switched on. When the OLED's prior condition is contrary to its current condition, a problem in reaching the next state will arise due to the capacitor Cs's residue charge. That is, the said residue charge will be discharged for too long. To resolve this problem, a negative voltage must be applied to Cs to neutralise the residue charge.

2.1 Negative voltage generator

As shown in Figure 3, the proposed Negative Voltage Generator consists of a Comparator (Comp), a Voltage-Controlled Oscillator (VCO), and four CPi stages, where i represents the stage number = (1, 2, 3, 4). An AND gate, parallel HV N-device MNi, Negative Level Shifter (NLSi), 4-Phase Clock Generator (CGi), and Negative Charge Pump (CP) stage are integrated into every CPi stage. Detailed functionality of these subcircuits will be stated in the following subsections.

- Generation of four non-overlapping clocks is carried out by the 4-phase CGi.

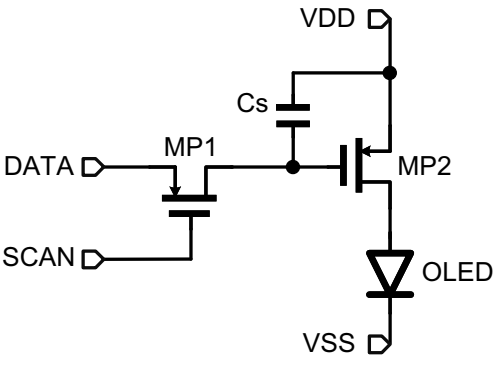


Figure 5. A simplified organic light-emitting diode's (OLED) driver circuit.

- An adjustment of the output capacitor, Co1, is needed for the output ripple elimination.
- The VCO, Comp, and feedback resistors (RFB1, RFB2) consist of the PFM (phase frequency modulation) feedback control circuit, which stabilises the overall system.
- When MNi in the CPi stage is not chosen, the corresponding bypass route is established such that the generated voltage in the preceding CP(i-1) stage is linked to the succeeding stage, CP(i+1), as shown in Figure 3. Furthermore, the bypass route assigned to MNi supports the four phases in our CP, which may be activated using enable inputs ENi depending on any selection, e.g. 1, 3, 4, 2, rather than being constrained to 1, 2, 3, 4. That is, any different random sequence of switching phases is allowed.
- A particular NLSi is driven by input SINi whose state is the inverted state of ENi in Figure 3. Then, appropriate gate drives were generated by the NLSi in every CP stage. With this, the bulk voltage in the said particular stage is suitably biased to switch the state of MNi completely.

2.2 Requirements of HV N-device

Transistors along the output path must have their bulk negatively biased for negative output voltage generation. For this reason, an N-type device was selected for four parallel HV devices (MNi) and transistors present in every CP stage. More importantly, referring to the HV N-device's cross-section in Figure 6, to prevent its PN junction from conducting, the selected HV N-device should be equipped with an Isolation Ring made of a Deep P-well and an N+ Buried Layer.

2.3 Negative Charge Pump (CP)

Figure 7 shows the Negative Charge Pump circuit for each CP stage, where all transistors are HV-type devices. Meanwhile, the 4-Phase CG in Figure 3 generates four non-overlapping clocks needed for every CP stage. These clocks, namely clki1, clki2, clki3, and clki4 (where i is the stage number), correspond to clk1, clk2, clk1aux, and clk2aux,

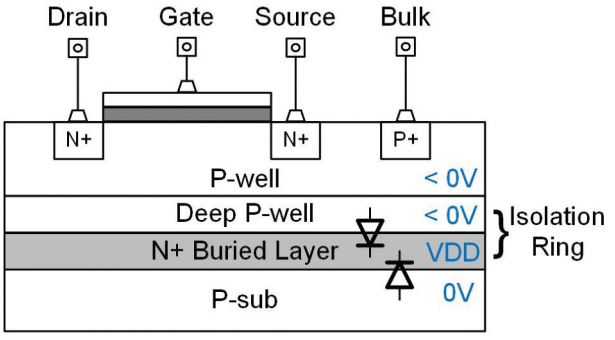


Figure 6. HV N-device's cross-section.

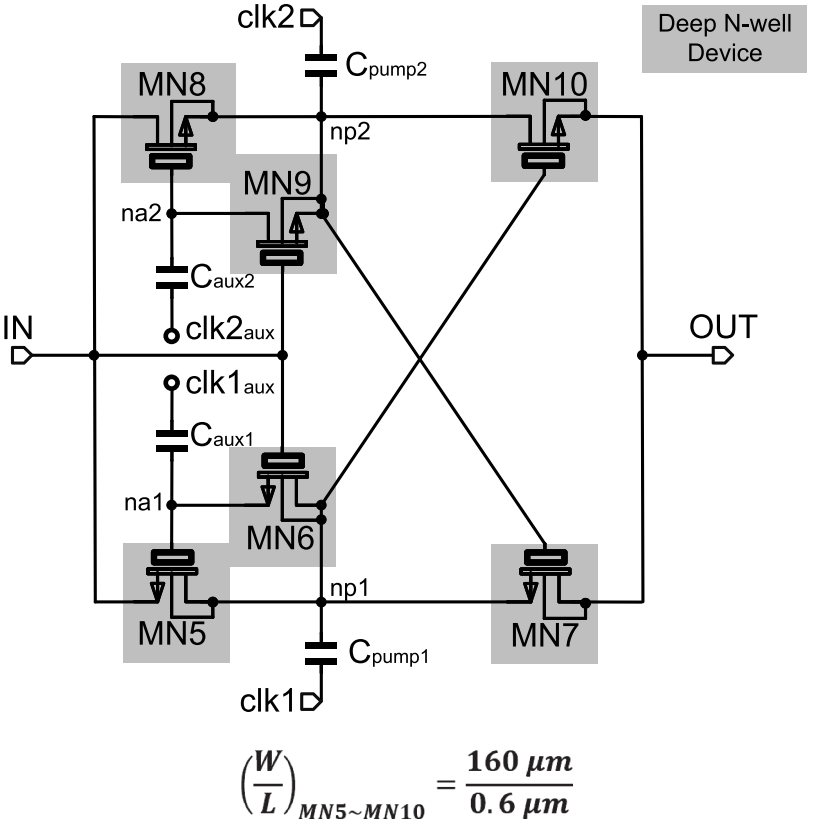


Figure 7. Negative charge pump schematic.

respectively, where they are shown in the circuit's timing diagram in Figure 8. During the first half period, the following five states of the CP are listed below:

- T1: IN is pulled down to GND. Nodes np1 and na1 are pulled low to -VDD. Node np2 is pulled high to GND, while na2 is equal to VDD-Vth.
- T2: For na1 to be driven to -Vth state, clk2 is logic 1.

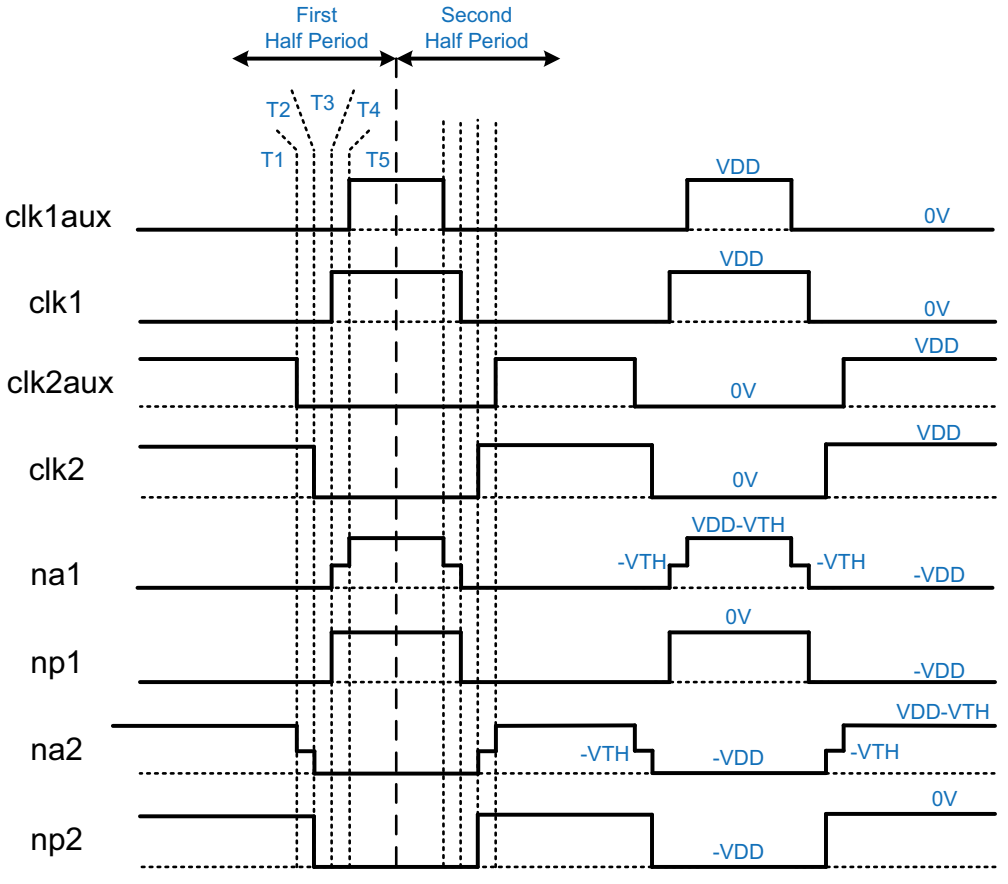


Figure 8. Negative charge pump timing diagram.

- T3: All four clocks are at logic 0, indicating that the system is in a steady-state condition.
- T4: To pull down node np1 at logic 0, clk1 is triggered to logic 1 when na1 is driven to -Vth.
- T5: clk1aux is at logic 1, resulting in node na1 becoming VDD-Vth.

It is worth noting that the behaviour of the CP during the second half period in Figure 8 is diametrically opposed to the operation during the first half period. In a nutshell, the voltages at nodes np1 and np2 are coupled to OUT and IN, respectively, during the first half period. A single CP stage will generate an output voltage of -VDD as a result of the action described above.

The value of the on-chip flying capacitors, Cpump1 and Cpump2, each at 72.9 pF, were chosen to achieve minimum chip area and keep ripple in an acceptable range (below 10%). Larger capacitors are better for resisting ripples, but they occupy a large chip area. By choosing the said value, the layout of the capacitors is regular, which is better for matching to resist process variations.

2.4 Negative Level Shifter (NLS)

Figure 9 shows the Negative Level Shifter (NLS) of every CP stage. VH is coupled to the supplied voltage (VDD). Inputs Bypass_ctrl, VL, and Bypass_sw correspond to toggle switch input SINi, negative voltage output outi, and MNi's switching signal swi in Figure 3, respectively. Particularly notable is that the bulks of MN11 and MN12 are negatively biased, similar to the devices in CPi. HV PMOS devices that are high VDS-drop tolerant P-devices were chosen for MP3 and MP4. When Bypass_ctrl is pulled up to VH, the off-transistors are MN12 and MP3 while the on-transistors are MN11 and MP4 and MN11, resulting in Bypass_sw equal to VDD. When Bypass_ctrl is pulled down to GND, the situation is reversed. Consequently, the input range is shifted from [0, VDD] to [-VDD, VDD] in this manner.

2.5 4-Phase Clock Generator (CG)

The 4-Phase Clock Generator in Figure 3 is shown in Figure 10. In this circuit, two delay cells are used, D1 and D2, which are based on the inverter with RC delay circuit, as shown in Figures 11 and 12, respectively. Notably, the D2 cell includes a buffer to generate two different signal delay durations. The operating principle of the four-phase clock generator is to input a clock through clkin. Then, two inverted clock signals are generated through INV1 passing through NOR1 and NOR2. Two-phase, non-overlapping clock signals are generated at nodes nc1 and nc2. Next, the said clock signals pass through INV2 and INV3 and the devices following them. The non-overlapping clock signals are then created: clk1, clk2, clk1aux, and clk2aux. Figure 13 shows the output waveforms of the generated clock signals; after clk1 drops to low potential, clk2aux rises to a high potential signal after a delay;, and after clk2 drops to low potential, clk1aux rises to a high potential signal after a delay.

2.6 7-stage Voltage-Controlled Oscillator (VCO)

The SWF driver does not need a high clock frequency to enable quick system functions, as is the case with other drivers. On the other hand, a low-power clock generator is preferably required to ensure proper operation if the said driver is powered by a battery. To accomplish this, we make use of the current-starved ring VCO, as seen in Figure 14, where a total of seven delay stages are used. Vvcoin in Figure 14 is in charge of determining which frequencies are used. The VCO limits

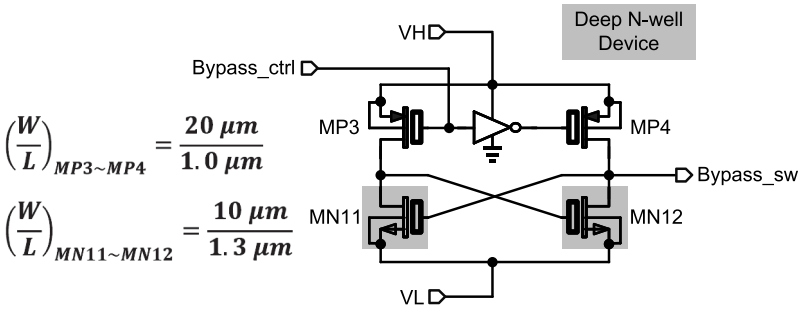


Figure 9. Negative level shifter (NLS) schematic.

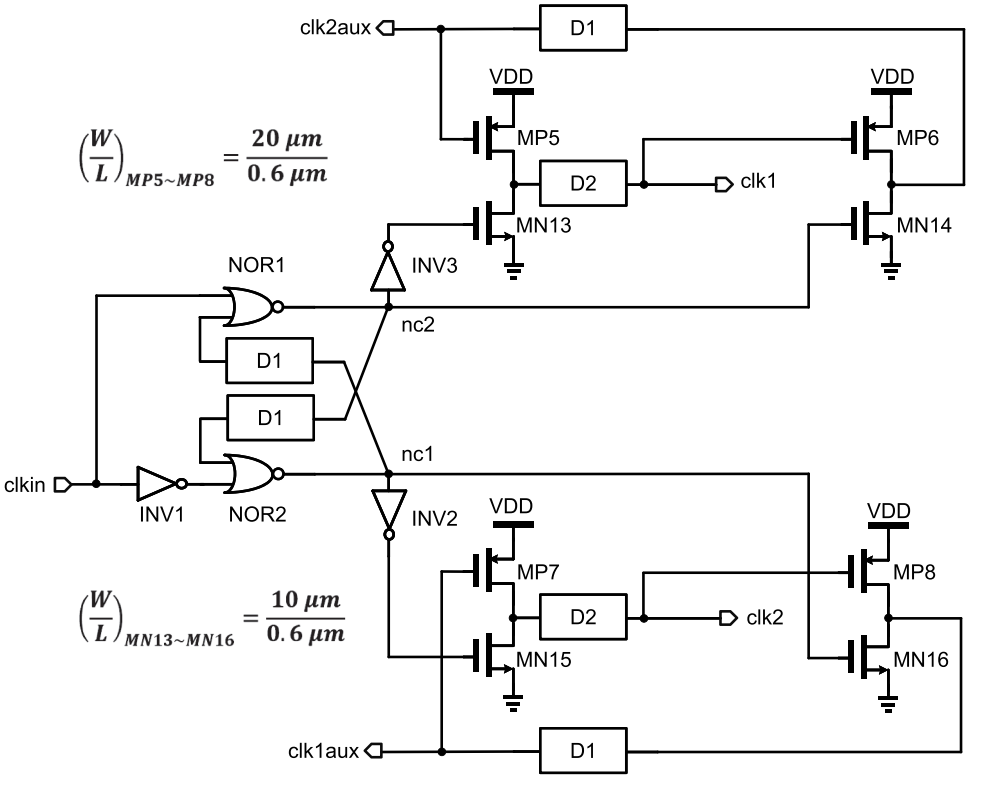


Figure 10. 4-Phase clock generator.

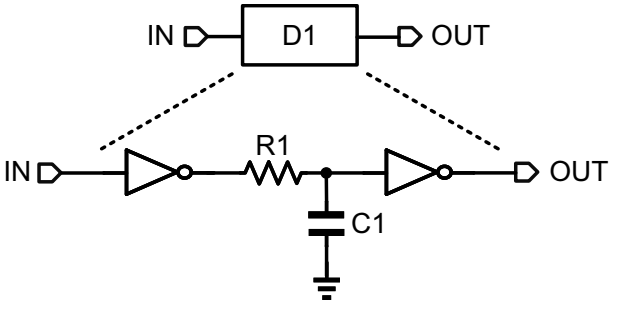


Figure 11. D1 delay cell in 4-Phase clock generator.

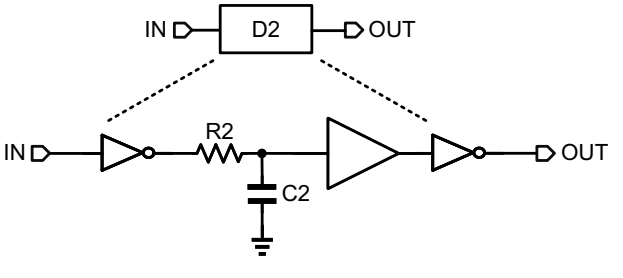


Figure 12. D2 delay cell in 4-Phase clock generator.

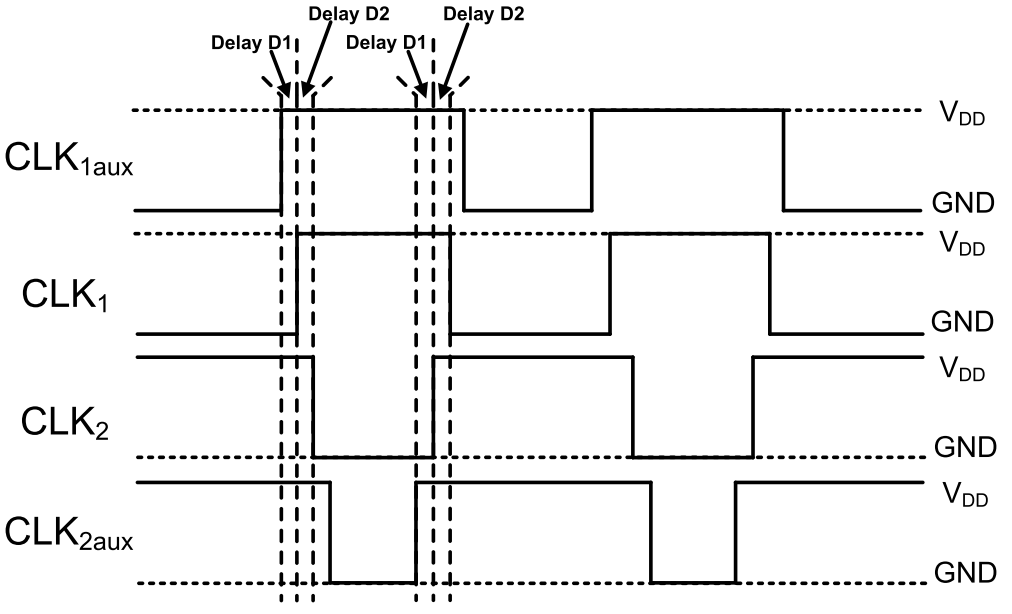


Figure 13. 4-Phase clock generator's output waveforms.

the PMOS (MP14 to MP21) and NMOS (MN24 to MN31) through PG and Vvcoin, and then controls the current flowing into the inverter chains so as to achieve the function of voltage controlling the frequency of the oscillator. The maximum frequency of this VCO is set at 20 MHz at Vvcoin = VDD.

2.7 Power analysis

The efficiency of any power electronic circuit is the most important factor to be considered. Switching loss (P_{SW}), driving loss (P_{drive}), and conduction loss (P_{cond}) represented by Equation. (1), (2) and (3), respectively, greatly affect the efficiency:

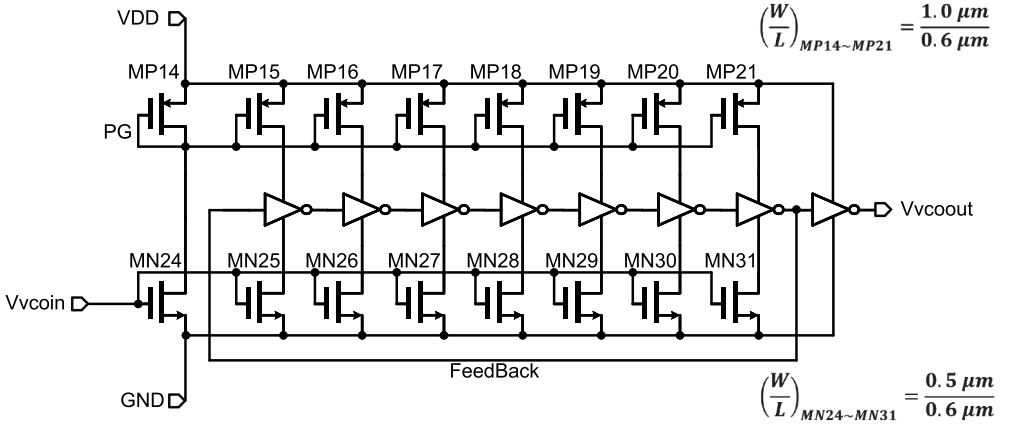


Figure 14. 7-stage VCO's schematic.

$$P_{SW} = V_{DS} \times I_D \times f_{sw} \times \frac{Q_{GS} + Q_{GD}}{I_G} \tag{1}$$

$$P_{drive} = V_{DS} \times I_D \times f_{sw} \tag{2}$$

$$P_{cond} = V_{DS} \times I_D \tag{3}$$

where *QGS* and *QGD* represent the gate-source and gate-drain charges, respectively, *ID* and *IG* are the drain and gate currents, respectively, *VDS* represents the drain-source voltage, and *fsw* denotes the switching frequency. Both switching loss and driving loss can happen in a power electronic device. However, the switching loss happens when the device is switching, and driving loss happens in the gate drive circuitry of the device. Both kinds of losses can have an adverse effect on the efficiency and dependability of power electronic systems, thus it is essential to minimise them to boost overall performance. Meanwhile, the drop in voltage, i.e. V_{DS}, that occurs across the power semiconductor device, causes conduction losses to occur, while the device is conducting current. The proposed work demonstrates three important low-power features that are advantageous:

(1) Because every CP stage employs parallel bypass power N-device, a minimised VDS on these routes is expected, resulting in a reduction of switching loss.
(2) There is no need to switch on every CP stage in sequence since all CP stages are configurable at will. As a result, there is a decrease in settling time at a specific output voltage.
(3) A reduced switching loss is expected when low-frequency 4-Phase Clock Generators are used.

2.8 Capacitor and parasitic losses analysis

The use of many large-area on-chip capacitance elements will generate a large amount of parasitic resistance and parasitic inductance. This will have a greater impact on the chip performance. In addition, with cross-coupling in the charge pump of the proposed generator, there is a reversion loss caused by the current reversal due to the path change by the switching of the MOS (Eid & Rodriguez-Villegas, 2017). The capacitors of the former and succeeding negatively charged pump stages also have redistribution loss as shown by the concept model in Figure 15 (Wing-Hung et al., 2005). When the capacitor (indicated by C203) of the first negative voltage charge pump stage is turned on, and the capacitor (indicated by C204) of the next stage is turned on at the same time, the two capacitors form a parallel connection. That is to say, the original energy of the circuit is stated in Equation (4). After being connected in parallel, it is modelled as shown in Equation (5), and the resulting energy loss is shown in Equation (6). Therefore, this fact results in lower output voltage and energy conversion efficiency.

$$E_{initial} = \frac{C_{203} \times V_{203}^2}{2} + \frac{C_{204} \times V_{204}^2}{2} \tag{4}$$

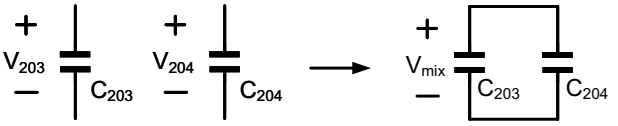


Figure 15. Redistribution loss model.

$$E_{final} = \frac{(C_{203} + C_{204}) \times V_{mix}^2}{2} \tag{5}$$

$$E_{loss} = \frac{(C_{203} || C_{204}) \times (V_{203} - V_{204})^2}{2} \tag{6}$$

3. All-PVT-corner post-layout simulations

The post-layout simulations are presented in this section showing that the capability of the NCP stages is adjustable; hence, there is no need to turn them on sequentially.

3.1 Step-by-step switching of a random order (Stage 1 → Stage 3 → Stage 2 → Stage 4)

Referring to Figure 3, toggle switches ENi (EN1, EN2, EN3, EN4) are used to enable a specific NCP stage. On the other hand, the toggle switches SINi (SIN1, SIN2, SIN3, SIN4) are used to trigger a specific NLS. For example, if the state of EN1 is high, the state of SIN1 is low.

Figure 16 shows the step-by-step enabling and disabling of the NCP stages (Stage 1 → Stage 3 → Stage 2 → Stage 4) and their corresponding changes in voltage waveforms at a load current of −0.5 mA at (TT, VDD, 25oC).

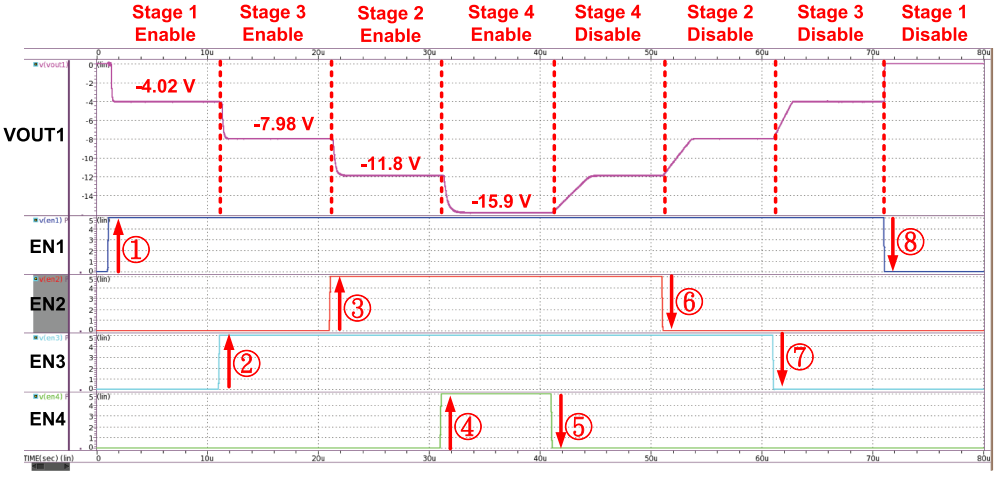


Figure 16. Post-layout simulation results showing the step-by-step switching of the proposed negative voltage generator (Stage 1 → Stage 3 → Stage 2 → Stage 4) at an output current of −0.5 mA, TT, VDD, 25oC.

3.2 Step-by-step switching of a sequential order (Stage 1 → Stage 2 → Stage 3 → Stage 4)

Meanwhile, post-layout simulations as shown in Figures 17, 18, 19 show the variations in voltage waveforms of the proposed Negative Voltage Generator's output as a result of step-by-step enabling and disabling in a different order of NCP stages (Stage 1 → Stage 2 → Stage 3 → Stage 4) under the output current of −0.5 mA at (TT, VDD, 25oC), (FF, VDD + 10% VDD, 75oC), and (SS, VDD − 10% VDD, 0oC) corners, respectively.

Hence, these results prove the ability of our proposed Negative Voltage Generator to be randomly configured.

4. On-chip measurement

The TSMC 0.18-μm HV BCD process was used to fabricate the proposed negative voltage generator on silicon. Its layout and die photo are shown in Figure 20, whose core area is 3321×1569 μm2. Its measurement setup is shown in Figure 21. ITech IT6333A power supply is utilised to generate the voltage inputs. LeCroy610Zi oscilloscope was used to observe the output waveforms.

Figure 21 shows the measurement results at −0.5 mA output current to demonstrate the performance of the proposed negative voltage generator. Figure 22 (a), (b), (c), (d) show Vout at a load current of 0.5 mA given that different stages are selected, respectively. The output voltage ranges from −3.9 to −14.0 V. A peak efficiency of 58.08% is verified. Meanwhile, the worst-case efficiency at a load current of −0.5 mA is 12.74%. The range of its output voltage is −4.67 to −18.5 V which satisfies the SWF driver's demands under this worst condition.

Based on Table 1, the highest Figure of Merit (FOM) by a wide margin was achieved by our proposed negative voltage charge pump, where the FOM is stated by Equation (7):

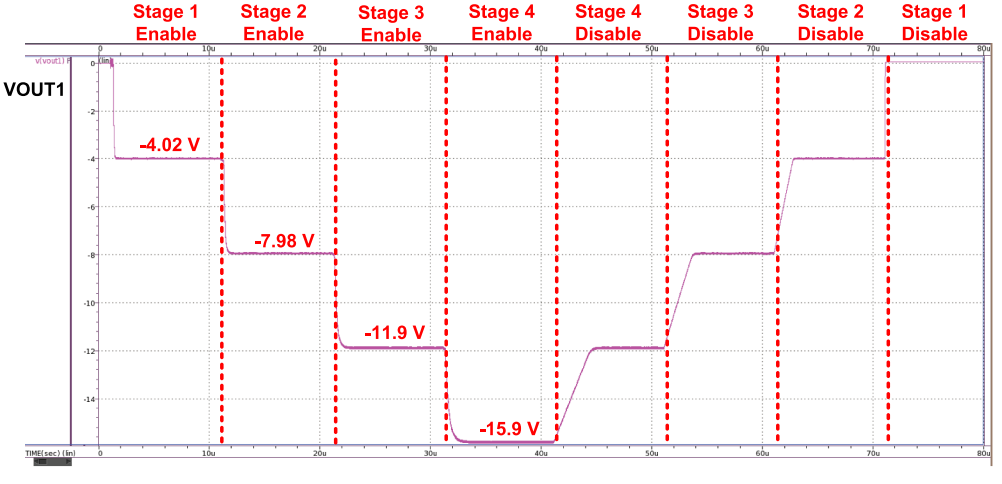


Figure 17. Post-layout simulation results showing the step-by-step switching of the proposed negative voltage generator (Stage 1 → Stage 2 → Stage 3 → Stage 4) at an output current of −0.5 mA, TT, VDD, 25oC.

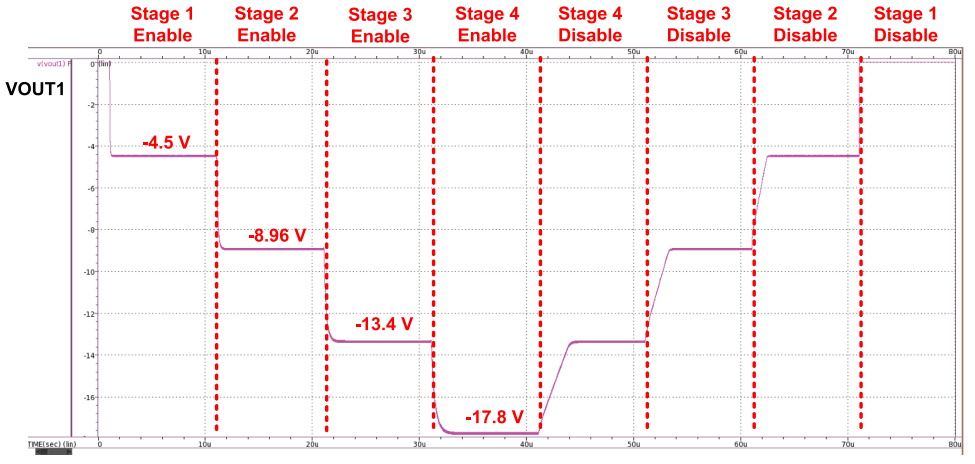


Figure 18. Post-layout simulation results showing the step-by-step switching of the proposed negative voltage generator (Stage 1 → Stage 2 → Stage 3 → Stage 4) at an output current of −0.5 mA, FF, VDD + 10%VDD, 75oC.

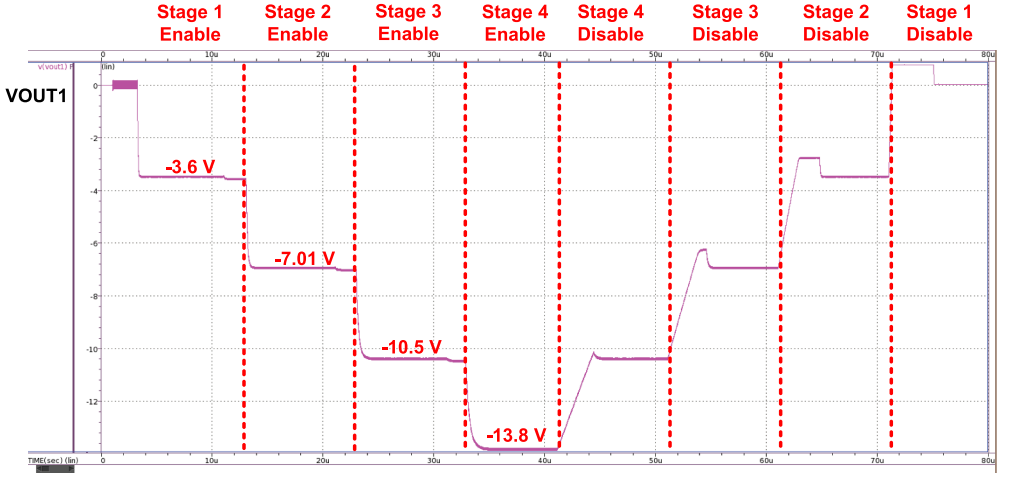


Figure 19. Post-layout simulation results showing the step-by-step switching of the proposed negative voltage generator (Stage 1 → Stage 2 → Stage 3 → Stage 4) at an output current of −0.5 mA, SS, VDD − 10%VDD, 0oC.

$$FOM = \frac{peak\ efficiency \times max.V_{out} \times max.I_{out}}{VDD} \tag{7}$$

Besides producing a broad range of voltage swings from −3.9 to −14.0 V, our charge pump also generates a current range from −0.5 to −5.5 mA. It is equipped with bypass switches that can be configured individually, allowing the selection of stages in any sequence. As a consequence, the switching loss is reduced, and the peak efficiency is increased to 58.08%. Apart from satisfying the SWF driver's requirement, our proposed

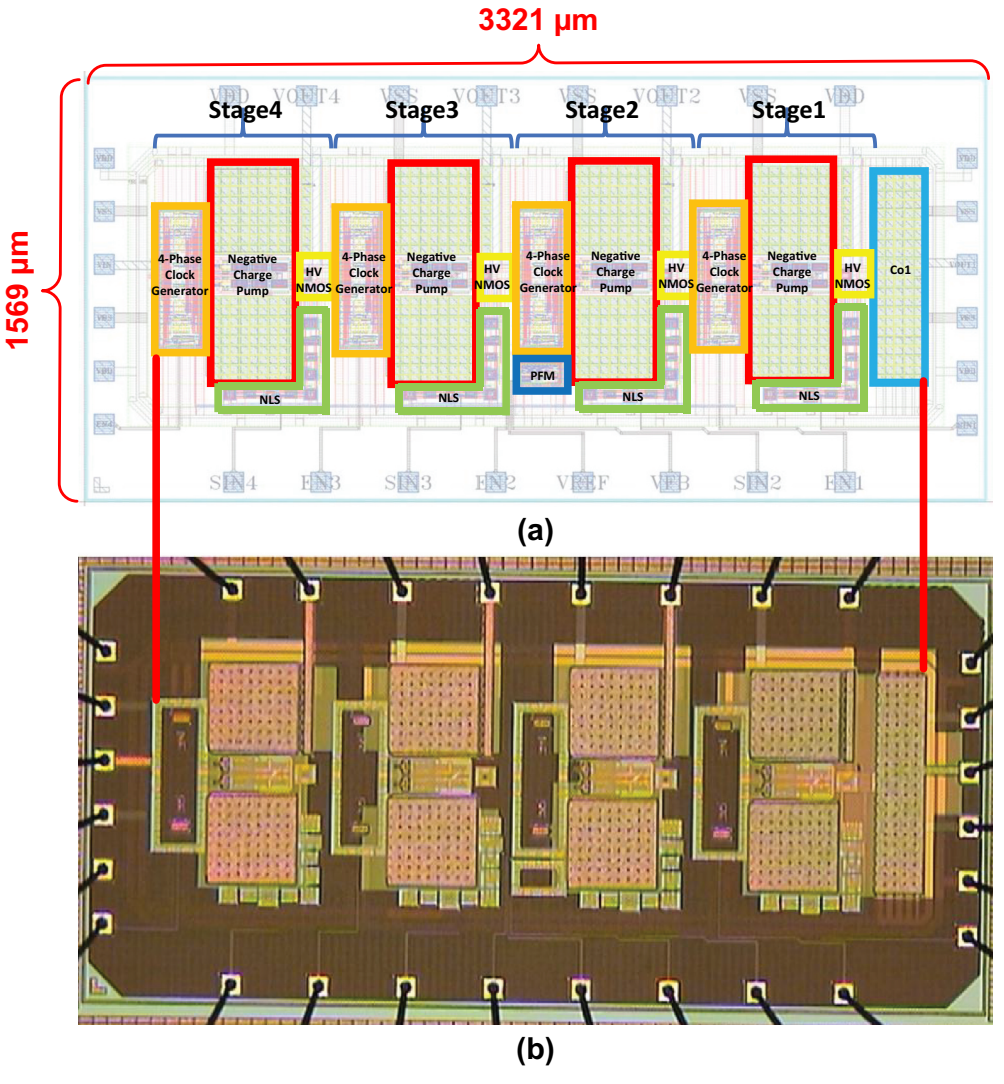


Figure 20. (a) Layout, and (b) die photo of the proposed negative voltage generator.

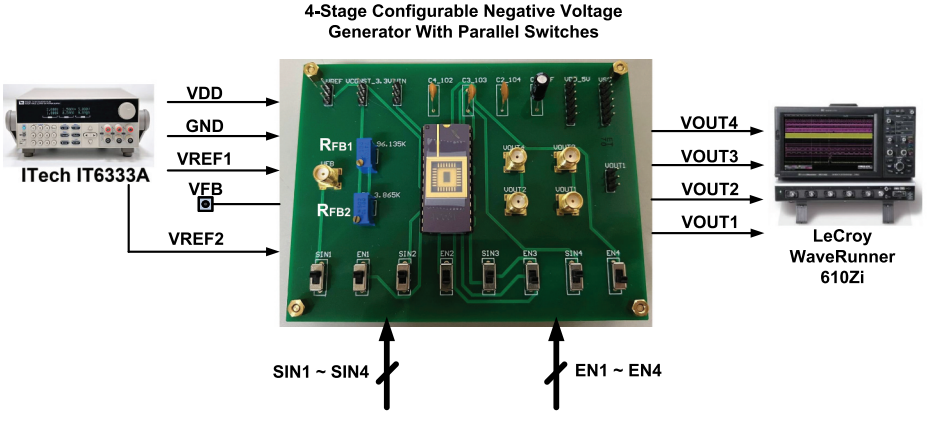


Figure 21. Measurement setup.

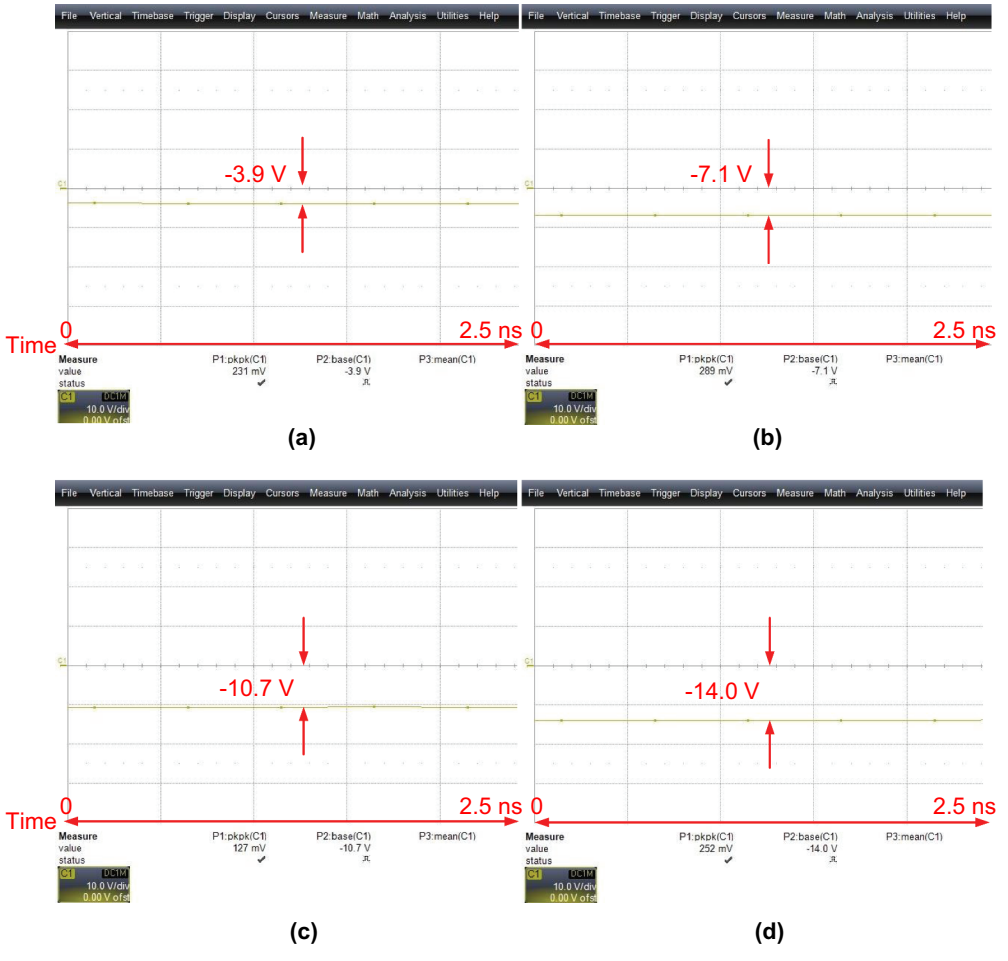


Figure 22. Output voltage Vout of the proposed negative voltage generator at a load current of 0.5 mA.

Table 1. Performance comparison of voltage generators.

	ICECS[1]	BioCAS[2]	TCAS-I[3]	VLSID[4]	TCAS-I[5]	This work
Year	2016	2018	2019	2020	2020	2023
Verification[6]	Sim.	Sim.	Meas.	Sim.	Meas.	Meas.
Process (nm)	130	180	180	180 BCD	250 BCD	180 BCD
No. of activated stages	8×(fixed)	3×(fixed)	3×(variable)	15×(fixed)	4×(variable)	4×(variable)
Switching frequency (MHz)	50	N.A.	N.A.	20	100	20
Flying Capacitance (pF)	1	100	50	N.A.	100	72.9
Vout range (V)	−9.4 to −16.1	−2.7 to −8.954	3.3 to 12.6	7.5 to 24	−0.3 to −9.3	**-3.9 to −14.0**
Max. Iout (mA)	−0.05	−5.5	3.5	+0.1	−5.5	−5.5
Max. Vout (V)	−9.4	−8.954	+12.6	+24.0	−9.3	**−14.0**
Peak efficiency (%)	67.43	55.28	70	49	52	58.08
FOM	26.41	909.1	935.45	65.33	886.6	**993.81**

Legend.
[1]= (Alameh et al., 2016).
[2]= (Lin & Ker, 2018).
[3]= (Luo et al., 2019).
[4]= (Patil et al., 2020).
[5]= (Lin & Ker, 2020).
[6]= Sim. = Simulation; Meas. = Measured results.

work achieves the best FOM and the widest negative voltage range when compared with prior works.

Notably, the efficiency of our work is lower compared to (Alameh et al., 2016) and (Luo et al., 2019) due to the lower flying capacitances used, i.e. 1 pF and 50 pF, respectively, as explained in Section 2.8. Future work may include using MOM capacitors as flying capacitances due to their advantage in higher voltage applications at an expense of larger area overhead and higher equivalent series resistance (ESR).

5. Conclusions

Our negative voltage generator was successfully fabricated and tested by generating currents from −0.5 to −5.5 mA and voltages from −3.9 to −14.0 V. It uses independent bypass switches to pick stages in any order. Switching loss decreases due to the low switching frequency of 20 MHz and peak efficiency of 58.08% was achieved. Our proposed work meets SWF driver requirements and has the best FOM and biggest negative voltage range by far.

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Disclosure statement

No potential conflict of interest was reported by the author(s).

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