INTERNATIONAL JOURNAL OF ELECTRONICS
https://doi.org/10.1080/00207217.2023.2235720

Taylor & Francis
Taylor & Francis Group

Check for updates

A 92.95%-efficiency high-voltage dual-mode buck converter using 0.5-μm HV CMOS process

Chua-Chin Wang [a,b], Lean Karlo S. Tolentino [a], Pin-Chuan Chen [a], Ralph Gerard B. Sangalang [a,c] and Oliver Lexter July A. Jose [a,c]

[a]Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan; [b]Institute of Undersea Technology, National Sun Yat-Sen University, Kaohsiung, Taiwan; [c]Department of Electronics Engineering, Batangas State University - the National Engineering University, Batangas City, Philippines

ABSTRACT

This paper presents a highly efficient dual-mode HV (high voltage) buck converter which operates at both light and heavy load currents. To improve the conversion efficiency at two different load conditions, a dual-mode design composed of pulse width modulation (PWM) and pulse frequency modulation (PFM) were implemented using TSMC 0.5-μm HV CMOS process. The chip area is 2038.05 $\times$ 1689.85 μm^2, while the input voltage ranges from 12 V to 15 V. A 92.95% peak efficiency at a load current of 10 mA was achieved based on on-silicon measurement results.

ARTICLE HISTORY
Received 24 May 2022
Accepted 31 May 2023

KEYWORDS
Buck converter; HV CMOS; dual-mode; pulse frequency modulation; pulse width modulation

1. Introduction

With the increasingly complex functions of modern electronic devices, the number of internal sub-circuits has also increased, and DC voltages required by the sub-circuits are also different from the voltage provided by a battery or an external power supply. A circuit that can convert the DC power supply voltage into different voltages is then needed, namely, DC–DC converters (Wang et al., 2011). There are various types of DC–DC converters, such as buck converters, boost converters, and buck-boost converters. According to the circuit operation principle, it can also be divided into isolated type, non-isolated type, forward type and flyback type (Lin et al., 2013). For instance, a buck converter steps down the input voltage from high to low voltage level which is normally used in battery management, communication, and other renewable energy applications (Bhattacharyya et al., 2012; Tolentino et al., 2015; Zastrow & Medeiros, 2021).

The performance of the DC–DC converter mainly depends on the conversion efficiency. To improve the conversion efficiency, the power control part becomes critical. There are two commonly used power control methods: pulse width modulation (PWM) and pulse frequency modulation (PFM) (Park et al., 2015). However, each of these two modulation methods has its advantages and disadvantages (Park et al., 2015; Wang et al., 2021). PFM converters work best at light loads, while PWM converters perform excellent at medium to heavy loads.

CONTACT Chua-Chin Wang ccwang@ee.nsysu.edu.tw Department of Electrical Engineering, National Sun Yat-Sen University, No. 70, Lienhai Road, Kaohsiung, Gushan, Taiwan

© 2023 Informa UK Limited, trading as Taylor & Francis Group

Many related works have been reported regarding buck DC–DC converters which attempted to achieve a higher peak efficiency. A buck mode was proposed in a solar energy harvesting system which accommodates a low input voltage of 3 V for a 1 V battery (El-Damak & Chandrakasan, 2015). It has an 87% peak efficiency. Meanwhile, a 92.90%-efficiency asynchronous buck converter for light and heavy loads was developed (Li et al., 2016). However, its highest step-down ratio is only 2 for the lowest input voltage of 6 V, while its lowest step-down ratio is only 1.11 for the highest input voltage of 30 V. To improve the buck converter which was proposed (El-Damak & Chandrakasan, 2015) by increasing its efficiency higher than 87%, this converter (Wu et al., 2017) for Bluetooth low energy (BLE) devices used a clocked hysteresis control method for the improvement of the efficiency at light load condition. Its highest efficiency is 90.4% at 1 μA load current. Meanwhile, a 1.2 V buck converter with a higher efficiency of 92% is proposed (Shin et al., 2020). It utilised a ramp generator which used only one amplifier instead of many amplifiers and two analogue level shifters that are commonly used in a traditional ramp generator. To resolve the buck converter's poor efficiency during light load conditions, a certain number of power MOSFETs were shut down and gate capacitance of power MOSFETs was reduced in the proposed PWM-based buck converter (Wang et al., 2022). The said buck converter accommodates a higher input voltage range of 10–14 V for a 91.68%-efficiency, 5-V output.

To resolve the trade-off between gate capacitance losses and on-resistance, segmented output switch transistors are proposed, which allow for switching of just a subset of the pass devices rather than all devices (Musunuri & Chapman, 2005; Williams et al., 1997). As a general rule, the number of switching segments is determined by keeping an eye on the load current; when the load is low, a smaller number of pass devices are switched. By contrast, when the load is large, all pass devices are switched. Meanwhile, a unique control approach, which uses the adaptive gm stage for comparing the power consumption of capacitive and resistive components in the analogue domain, is presented for dynamically determining the optimal size of a buck converter's pass device (Ozanoglu & Dundar, 2020).

As shown in Figure 1 (Wang et al., 2020), one of the applications that utilises DC–DC converter is Autonomous Underwater Vehicle (AUV) for underwater tasks, such as exploring the seabed terrain and ocean research. Due to the limitations of the underwater environment, lead-acid batteries where their voltages normally range from 12 to 15 V can be used as the main source of the AUV's power supply. To have a stable output voltage for



Figure 1. Autonomous underwater vehicle (AUV) (Wang et al., 2020).

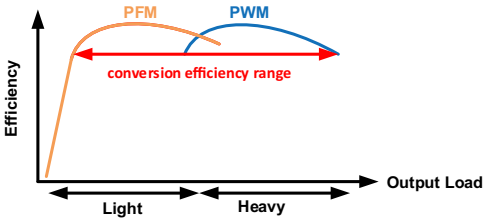


Figure 2. Conversion efficiency improvement in various load ranges.

other electronic instruments and devices inside the AUV where the normal output voltage is 5 V, the DC–DC converter must be used to stabilise the output voltage so that the electronic instruments and devices can be used correctly and safely.

As an improvement to the efficiency of the different buck DC–DC converters mentioned, a novel control method fully taking advantage of PWM and PFM for achieving a buck converter's higher efficiency is proposed in this study. It was then implemented using TSMC 0.5-μm HV CMOS process. It combines the two modulation modes' advantages into a single circuit on a single die to reduce power loss as illustrated in Figure 2. As a result, it has a better conversion efficiency no matter at light loads (load currents of 1 mA to 100 mA) or heavy loads (load currents of 100 mA to 500 mA).

This paper is organised as follows: Section 2 presents the system architecture of the proposed buck converter; Section 3 discusses the measurement results of the proposed chip; Finally, Section 4 concludes this study.

2. Dual-mode DC–DC converter system architecture

The proposed buck converter is shown in Figure 3. It consists of the following blocks which are discussed later in this section.

2.1. Core of buck converter

A traditional synchronous DC–DC converter type is shown in Figure 4, which is used as Core of Buck Converter in Figure 3. Its two power switches M_{HS} and M_{LS} are driven by Control Circuit. When M_{HS} is turned on and M_{LS} is turned off, the inductor L is charged and stored by the current I_L. Otherwise, the inductor will discharge. With regard to the input voltage, V_{in}, the stable output voltage V_{out} can be modulated by the duty cycle (D) as shown in Equation (1).

$$V_{out} = V_{in} \times \frac{D}{1 - D} \tag{1}$$

By contrast, Figure 5 shows our Core of Buck Converter. M_{HS} and M_{LS} are divided into M_{HS1}, M_{HS2} and M_{LS1}, M_{LS2}, respectively, so that these transistors can be switched based on sensed loading scenarios. All the driving signals, including *QPH*, *QNH*, V_{c_p}, V_{c_n}, are generated by other sub-circuits in Figure 3. Off-chip components L and C can be calculated using Equations (2) and (3) reported previously (Wang et al., 2011), where F_{sw} is the switching frequency and ΔV_{out} is the output voltage variation.

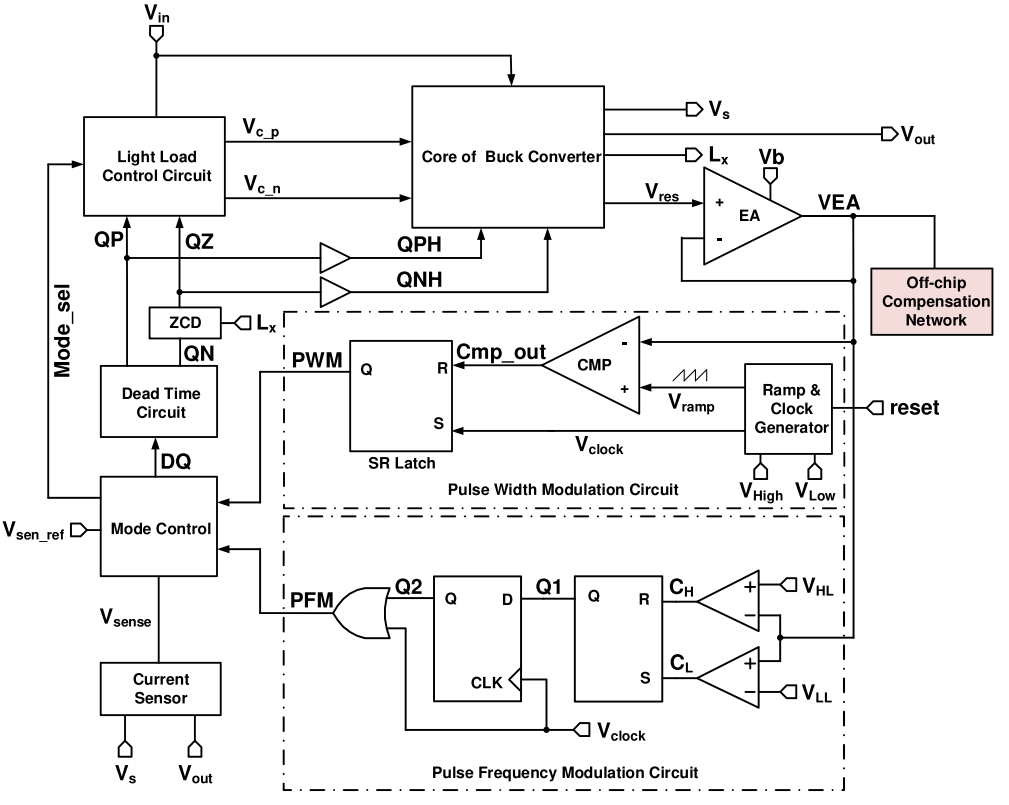


Figure 3. Proposed dual-mode DC–DC converter.

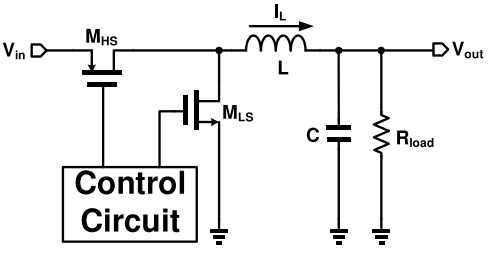


Figure 4. Traditional synchronous buck converter.

$$L \geq \frac{V_{out} \cdot (1 - D)}{2 \cdot I_{out} \cdot F_{sw}} \tag{2}$$

$$C = \frac{(V_{out}/\Delta V_{out})(1 - D)}{8 \cdot L \cdot (F_{sw})^2}; \frac{\Delta V_{out}}{V_{out}} < 1\% \tag{3}$$

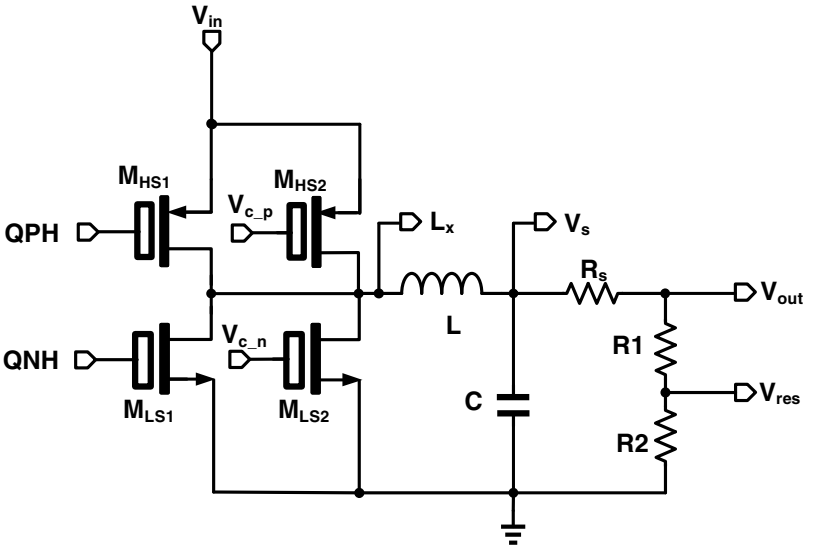


Figure 5. Proposed core of buck converter in Figure 3.

2.2. Error Amplifier (EA)

Figure 6 shows the schematic of the error amplifier (EA) in Figure 3. It consists of a set of differential pairs and current mirrors. It prevents the output current from flowing into the PWM circuit. In addition, it is also used to stabilise the reference voltage required by the PWM and reduce the output voltage ripple. To ensure the stability of the buck converter, especially in its output voltage during PFM mode, an off-chip compensation network of resistor (R_{comp}) and capacitor (C_{comp}) is added referring to Figures 3 and 7.

A Type II compensation method is implemented for the compensation network since the output capacitor used is an electrolytic type to satisfy the condition f_{ESR}/f_{LC} less than 5 and f_{ESR} less than the system bandwidth (Wang et al., 2011). f_{LC} and f_{ESR} refer to the double-pole frequency of converter's output filter (inductor L and C) and equivalent series

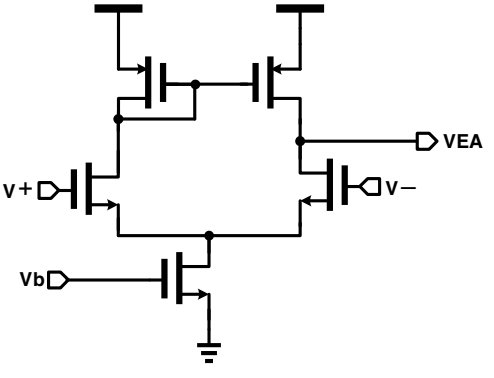


Figure 6. Error amplifier (EA).

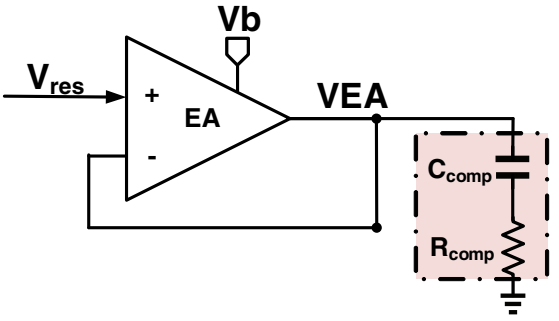


Figure 7. Compensation network for the error amplifier (EA).

resistance (ESR) zero frequency of the output capacitor (C) as shown in Figure 5, respectively. They are represented by Equations (4) and (5), respectively.

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} \tag{4}$$

$$f_{ESR} = \frac{1}{2\pi(ESR)(C)} \tag{5}$$

Meanwhile, R_{comp} and C_{comp} can be computed (Sipex, 2006; Wang et al., 2011) using Equation (6) and (7), respectively, where F_{sw} is the switching frequency, V_{ramp} is the ramp voltage, and $V_{in(max)}$ is the maximum input voltage of the converter.

$$R_{comp} = \frac{2\pi \cdot (0.2F_{sw}) \cdot L \cdot V_{ramp} \cdot R_2}{ESR \cdot V_{in(max)}} \tag{6}$$

$$C_{comp} = \frac{1}{0.6 \cdot R_{comp} \cdot (\sqrt{LC})^{-1}} \tag{7}$$

2.3. Pulse Width Modulator (PWM)

Figure 8 shows the pulse width modulator circuit (PWM) in Figure 3 which is used to generate a PWM signal. This signal controls the power transistors so that the output signal of the circuit can be stabilised within a pre-defined range (Baker, 2019). The triangle wave and clock generator are shown in Figure 9. When V_{Clock} is low, M_{High} is turned on and M_{Low}

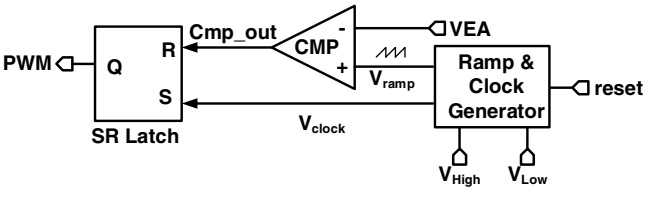


Figure 8. Pulse width modulator (PWM).

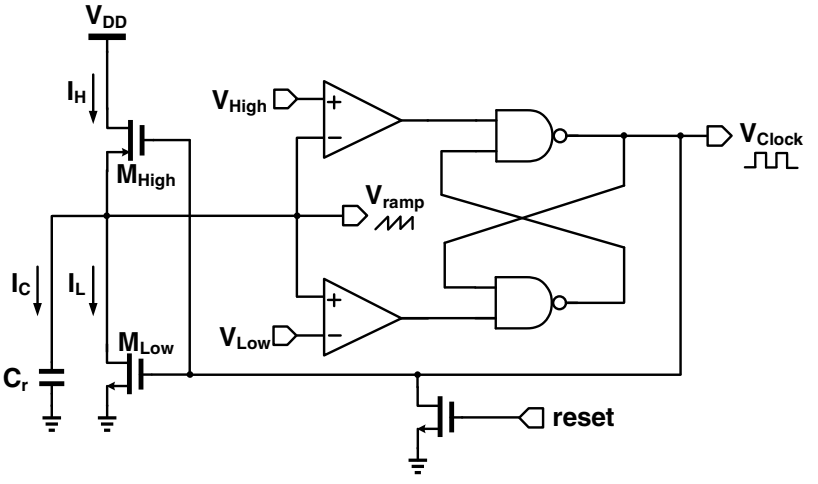


Figure 9. Ramp and clock generator.

is off. The capacitor C_r is charged with current I_H. At this time, V_{ramp} will rise. The frequency of the ramp voltage is represented by Equation (8).

$$f_{ramp} = \frac{I_H}{(V_{High} - V_{Low}) \times C_r} \tag{8}$$

When V_{ramp} is higher than V_{High}, V_{Clock} becomes high. Then, M_{High} is turned off and M_{Low} is on. The capacitor C_r is discharged by current I_L to drop V_{ramp}. When V_{ramp} is lower than V_{Low}, V_{Clock} becomes low. Then, the repeated cycle will generate a stable triangle wave and a clock signal. The comparator compares Error Amplifier's output voltage VEA with V_{ramp} and generates a square wave signal, Cmp_out. Cmp_out and V_{Clock} generate the PWM signals through the SR latch as shown in Figure 10.

2.4. Pulse Frequency Modulator (PFM)

Pulse Frequency Modulator (PFM) circuit in Figure 3 is shown in Figure 11. Its input, VEA signal, is compared with the high-level voltage V_{HL} in the first input comparator, and VEA signal is also compared with the low-level voltage V_{LL} in the other input comparator. Two comparators provide the hysteresis comparison. When VEA is higher than V_{HL}, SR latch output Q1 is high and DFF output Q2 is high. At this time, V_{Clock} will be masked out to reduce switching loss. On the contrary, when VEA is less than V_{LL}, SR latch output Q1 is low, and DFF output Q2 is low, V_{Clock} is now used as the control signal to generate the PFM signal. Table 1 summarises the logic truth table for the PFM.

2.5. Dead time circuit

Dead Time circuit in Figure 3 is shown in Figure 12 consisting of several inverters connected in series. The output of each inverter stage is connected to a capacitor. The output delay is generated to avoid QN and QP signals to have the same logic value at the same time which causes unwanted power loss.

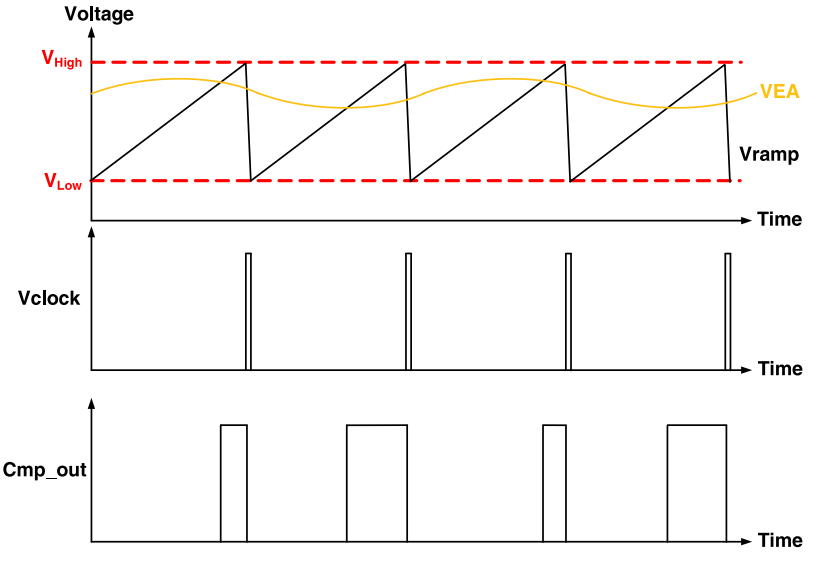


Figure 10. PWM waveform.

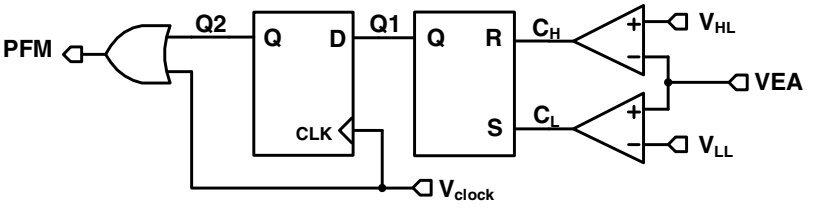


Figure 11. Pulse frequency modulator (PFM).

Table 1. Logic truth table for the PFM.

Condition	C_H	C_L	Q1	Q2	PFM
VEA $> V_{HL}$	Low	High	High	High	High
VEA $< V_{LL}$	High	Low	Low	Low	V_{Clock}

2.6. Light load control circuit

In the design of DC–DC converters, one of the most important indicators is conversion efficiency. To improve the conversion efficiency, it is necessary to identify the causes of the power loss in the circuit. From the system loss analysis, it can be clearly observed that the total power loss can be divided into two parts: (1) conduction loss and (2) switching loss (Kim & Rincón-Mora, 2009).

The conduction loss (P_{Con}) is related to the conduction resistance, conduction time, parasitic capacitance and inductance. Figure 13 shows the generic conduction loss analysis where a simple equivalent representation of the conduction resistance and parasitic capacitance of the power transistors in a power converter circuit is shown. When the power transistors MP and MN are turned on, on-resistances of $R_{on,p}$ and $R_{on,n}$, the on-times of D_p and D_n, and the parasitic capacitances of C_{gs} and C_{gd} are present.

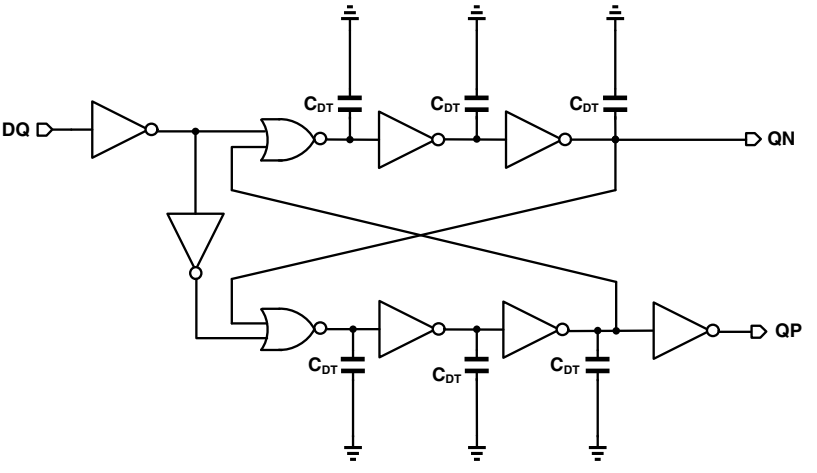


Figure 12. Dead time circuit.

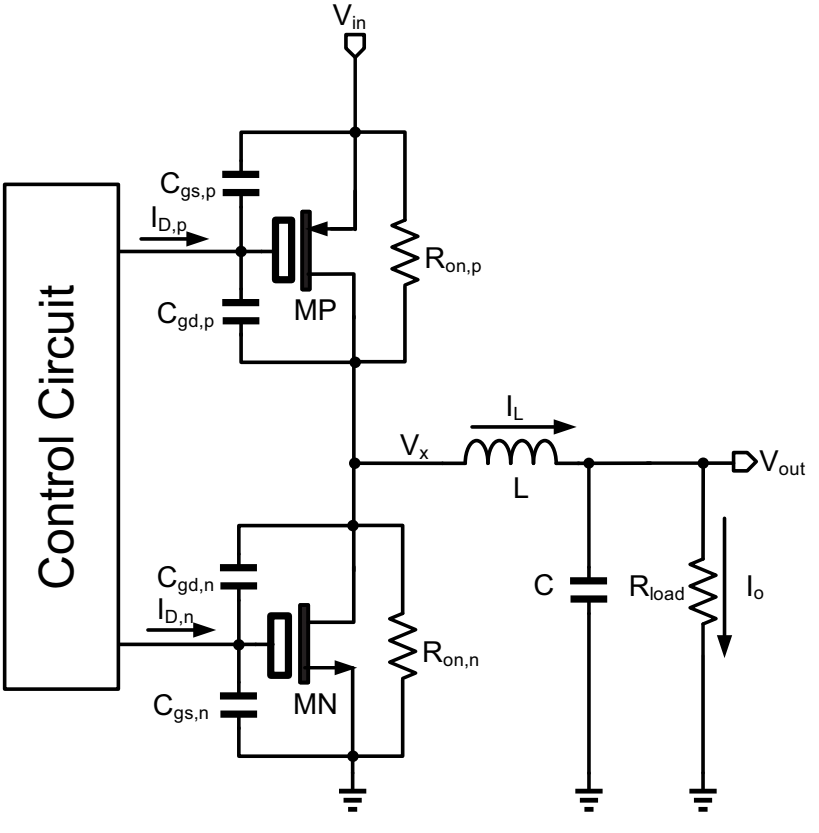


Figure 13. Conduction loss analysis.

Equation (9) represents the conduction loss, which is composed of the DC part, $P_{Con,dc}$ and the AC part, $P_{Con,ac}$.

$$P_{Con} = P_{Con,dc} + P_{Con,ac} \tag{9}$$

$$P_{Con} = I_{dc}^2 \cdot R_{on} + I_{ac,rms}^2 \cdot R_{on} \tag{10}$$

From Equation (10), the equivalent on-resistance R_{on} is represented by Equation (11).

$$R_{on} = R_{on,p} \cdot D_p + R_{on,n} \cdot D_n = R_{on,p} \cdot (1 - D_n) + R_{on,n} \cdot D_n \tag{11}$$

Since $R_{on,p}$ and $R_{on,n}$ are approximately equal when the widths of these two transistors are large, Equation (11) can be simplified to Equation (12).

$$R_{on} = R_{on,p} = R_{on,p} \tag{12}$$

As for the loss caused by the AC signal $I_{ac,rms}$ in Equation (10), it is related to the conduction time (D_p) of the transistor MP and the switching frequency F_{sw}, which can be expressed by Equation (13).

$$I_{ac,rms} = \frac{\Delta i_L}{\sqrt{12}} = \frac{(V_{in} - V_{out}) \cdot D_p}{\sqrt{12} \cdot L \cdot F_{sw}} = \frac{V_{in}(1 - D_p) \cdot D_p}{\sqrt{12} \cdot L \cdot F_{sw}} \tag{13}$$

Substituting Equation (13) into Equation (10) results in Equation (14):

$$P_{Con} = \left[I_o^2 + \frac{[D_p \times (1 - D_p) \times V_{in}]^2}{12 \times L^2 \times F_{sw}^2} \right] \times R_{on} \tag{14}$$

where D_p is the duration at ON state of the power transistor, I_o is the output current, V_{in} is the input voltage, F_{sw} is the switching frequency, R_{on} is the ON resistance of the power transistor, and L is the inductance of the filter.

Meanwhile, the switching loss (P_{sw}) occurs every time the power transistor switches, as shown in the waveform of Figure 14. That is, when the power transistor is turned on, the driving current I_D charges the gate parasitic capacitances (C_{gs} and C_{gd}) during the rising period t_1, and between the V_{DS} falling period

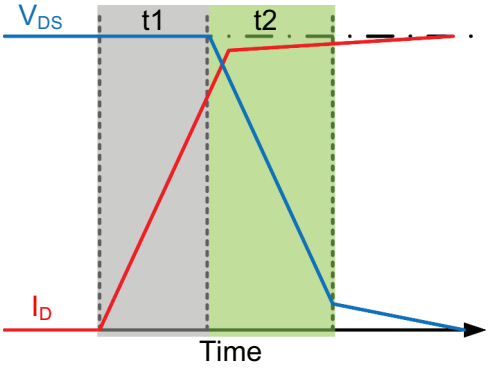


Figure 14. Switching loss analysis (Ayachit & Kazimierczuk, 2019).

t_2. It can be seen in Equation (14) that the switching frequency and switching loss are directly related.

$$P_{sw} = C_{g,eq} \times F_{sw} \times V_{in}^2 \tag{15}$$

where V_{in} is the input voltage, F_{sw} is the switching frequency, and $C_{g,eq}$ is the parasitic capacitance.

R_{on} and $C_{g,eq}$ can represented by Equation (16) and (17), respectively:

$$R_{on} = \frac{Length}{W \times \mu_p \times C_{ox} \times V_{od}} \tag{16}$$

$$C_{g,eq} = W \times Length \times C_{ox} \tag{17}$$

where W and $Length$ is the width and length of the power transistor, respectively, μ_p is the charge-carrier effective mobility, V_{od} is the overdrive voltage, and C_{ox} is the gate oxide capacitance. The total power loss P_{Loss} is equal to the sum of the conduction and switching losses. Thus,

$$P_{Loss} = \left(I_o^2 + \frac{[D_p(1 - D_p) \times V_{in}]^2}{12L^2 \times F_{sw}^2} \right) \times \frac{Length}{W \times \mu_p \times C_{ox} \times V_{od}}$$

$$+ W \times Length \times C_{ox} \times F_{sw} \times V_{in}^2$$

Parameterised to be related to the width W, P_{Loss} is denoted in Equation (18):

$$P_{Loss} = \frac{\alpha}{W} + \beta \times W \tag{18}$$

where

$$\alpha = I_o^2 + \frac{[D_p \times (1 - D_p) \times V_{in}]^2}{12 \times L^2 \times F_{sw}^2} \times \frac{Length}{\mu_p \times C_{ox} \times V_{od}} \tag{19}$$

$$\beta = Length \times C_{ox} \times F_{sw} \times V_{in}^2 \tag{20}$$

To have a minimum P_{Loss}, the slope of P_{Loss} was determined by differentiating P_{Loss} in Equation (18) with respect to width W and letting it equal to 0:

$$\frac{d}{dW} P_{Loss} = \frac{d}{dW} \frac{\alpha}{W} + \frac{d}{dW} \beta \times W$$

$$0 = \frac{-\alpha}{W^2} + \beta$$

$$W = \sqrt{\frac{\alpha}{\beta}} \tag{21}$$

Thus, Equation (21) is the formula for power transistor width at minimum power loss, which also gives the maximum efficiency.

Suppose $I_o = 10$ mA, $D = 0.5$, $V_{in} = 12$ V, $L = 10$ mH, $F_{sw} = 90$ kHz, W and $Length$ of the power transistor are 8000 and 0.5 , respectively, $C_{ox} = 1.8$ fF/μm^2,

$\mu_p C_{ox} = 120\ \mu A/V^2$, V_{od} of power transistor is 0.5 V, $P_{con} = 0.105$ mW and $P_{sw} = 0.093$ mW which represents 53% and 47% of the total power loss, respectively. The distribution of the said power losses is represented in a pie chart as shown in Figure 15.

The loss of the buck converter at light load is dominated by the switching loss. To reduce the switching loss, the frequency can be reduced. Thus, under light load, the buck converter will operate at PFM mode to reduce the switching frequency. In addition, the size of $C_{g,eq}$ can be reduced. To make $C_{g,eq}$ smaller, the width of the power transistor is decreased. This method is selected in this design procedure. Meanwhile, two modes of light load and heavy load are proposed. When the circuit is at light load, a certain number of power transistors are turned off. The Mode_sel signal is used to determine the load state to adjust power transistors which will be turned on or off to reduce conversion loss and enhance the efficiency.

Figure 16 shows the light load control circuit which adjusts the power transistors depending on the current sensor. This sensor will sense the load. If Mode_sel is logic 1, the current load is light load, and some power transistors will be turned off to reduce power loss and improve conversion efficiency. On the other hand, if Mode_sel is logic 0, a heavy load condition is expected, and all power transistors will be turned on, so that the circuit can have good conversion efficiency even under heavy load.

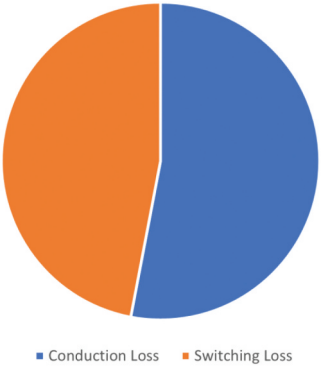


Figure 15. Power loss distribution of the proposed buck converter.

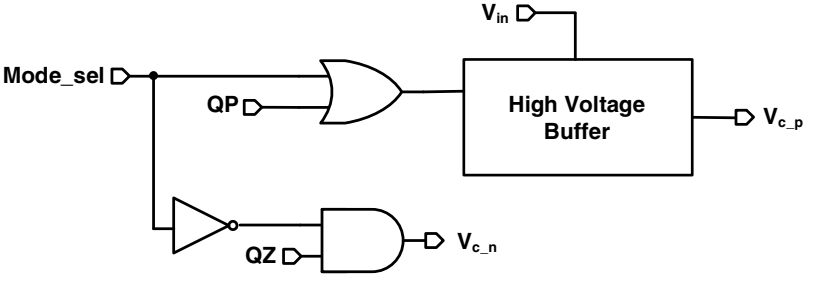


Figure 16. Light load control circuit.

2.7. Current sensor

Current Sensor of Figure 3 is given in Figure 17, where the current sense resistor R_s detects the magnitude of the current flowing through, and resistor KR_s maps an induced current I_s/K. The value of resistor R_s is selected to be very small so that the output load will not be affected. With this, *Is* will vary with the load current and will not affect greatly the current sensor's functionality. As a result, the output of the current sensor corresponds to the sensed voltage V_s and the load status is determined. To elaborate further, V_a and V_{out} are represented by Equations (22) and (23), respectively:

$$V_a = Vs - \left(\frac{I_s}{K}\right) K \cdot R_s \tag{22}$$

$$V_{out} = Vs - I_s \cdot R_s \tag{23}$$

One set of current mirrors (transistors M_{p302}, M_{p303} and M_{n302}, and M_{n303}) generates two identical currents ($I_{302} = I_{303}$), making V_a and V_{out} equal. The other set of current mirrors (I_{301} and I_{302}) ensures that the circuit will not be over-charged. The corresponding voltage V_c is generated by I_{304} and represented by Equation (24).

$$V_c = V_{GS,M_{n304}} \approx V_{GS,M_{p304}} \cdot \sqrt{\frac{W_{M_{p304}} \cdot L_{M_{n304}}}{2 \cdot W_{M_{n304}} \cdot L_{M_{p304}}}} \tag{24}$$

where $W_{M_{p304}}$ and $L_{M_{p304}}$ are the M_{p304}'s width and length, respectively; $W_{M_{n304}}$ and $L_{M_{n304}}$ are the M_{n304}'s width and length, respectively. Using Equations (22), (23), and (24), V_c is now stated as Equation (25):

$$V_c \approx \left(V_{G,M_{p304}} - V_{out}\right) \cdot \sqrt{\frac{W_{M_{p304}} \cdot L_{M_{n304}}}{2 \cdot W_{M_{n304}} \cdot L_{M_{p304}}}} \tag{25}$$

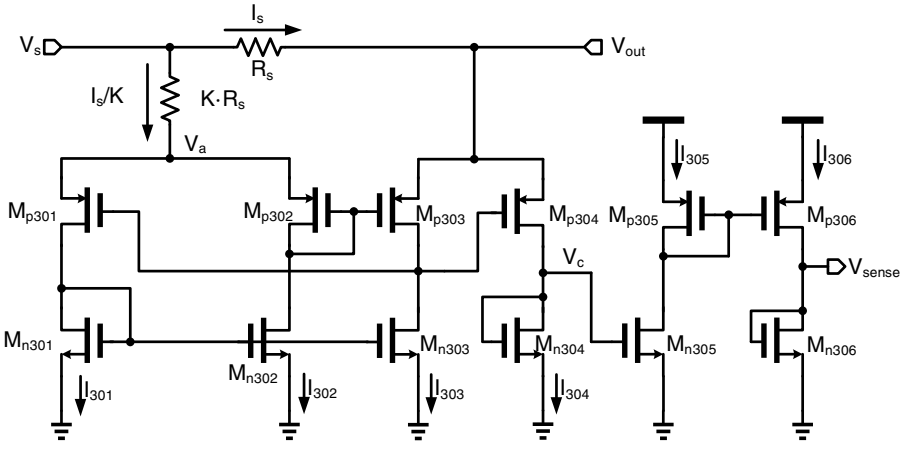


Figure 17. Current sensor (Wang et al., 2016).

The said equation proves the current sensing of the circuit where V_c changes with V_{out} as well as V_{out} changes with I_s. Finally, the output voltage linearity is adjusted through the output stage (transistors M_{p305}, M_{p306}, M_{n305}, and M_{p306}).

2.8. Mode control

Figure 18 shows Mode Control in Figure 3, where the V_{sense} generated by the current sensor is compared with V_{sen_ref} to determine the load condition. The resulting output is the Mode_sel signal. If the condition is heavy load, Mode_sel is logic 0, and the multiplexer selects PWM as the power transistor control signal. Otherwise, the multiplexer selects PFM as the power transistor control signal.

2.9. Zero Current Detector (ZCD)

Figure 19 shows the Zero Current Detector circuit in Figure 3, which is primarily used in discontinuous conduction mode (DCM), to avoid the reverse flow of the inductor current. In this circuit, if L_x is lower than 0, the comparator outputs the reset signal C_{Reset}, turning off the power transistors M_{LS} in Figure 5.

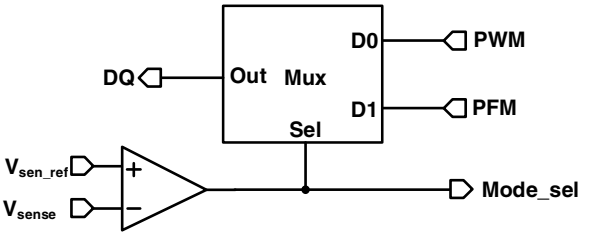


Figure 18. Mode control schematic.

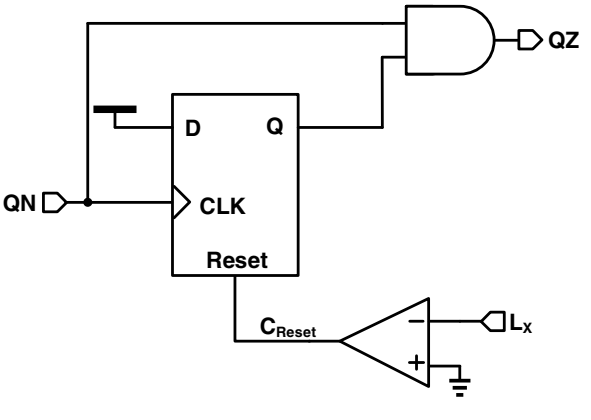


Figure 19. Zero current detector (ZCD).

3. Measurement results

The proposed DC–DC buck converter was implemented using TSMC 0.5-μm HV CMOS process. Figure 20 shows the chip layout, floor plan, and die micrograph of the proposed buck converter. Figure 21 shows the measurement setup of the chip. ITECH IT6333A and Keysight 33500B were used as power supply and signal generator, respectively. Chip measurements were conducted using WaveRunner 610Zi. As shown in Figures 22 and 23, under heavy load condition, it is operating at PWM mode and a regulated output voltage V_{out} of 5 ± 0.1 V is achieved. At a light load scenario, it is at PFM mode; transistors will be turned off by QPH and QNH, but V_{out} of 5 ± 0.1 V is still achieved. Vc_p and Vc_n control a part of the normal operation of the transistors. These signals contribute to achieve the smooth switching during mode change without causing any stability issues. The said converter has an output ripple of 16 mV. The power dissipation is 110 mW at 90 kHz switching frequency.

As shown in Figure 24, at different output currents, a better efficiency is exhibited by the proposed converter based on the measurement results compared to the efficiency of the conventional buck converter in Figure 4 based on simulation results. When the load is light, the efficiency advantage of our design is even more highlighted. The peak efficiency of the proposed converter is 92.95% at an output current of 10 mA. The worst-case efficiency is 65% at a light load current of 1 mA; this is higher compared to that of the

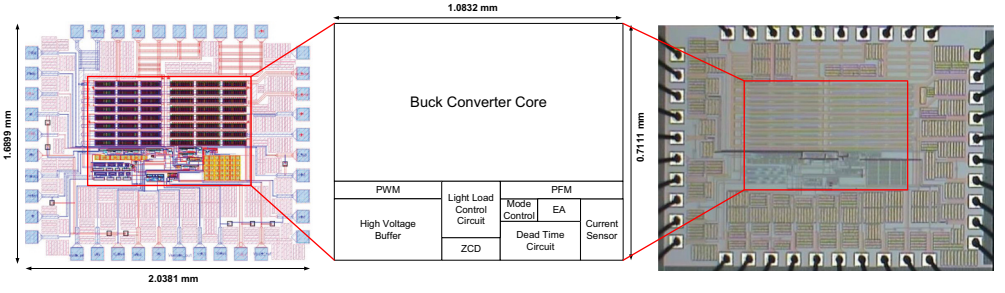


Figure 20. Chip layout (right), floor plan (centered) and die micrograph (right) of the proposed buck converter.

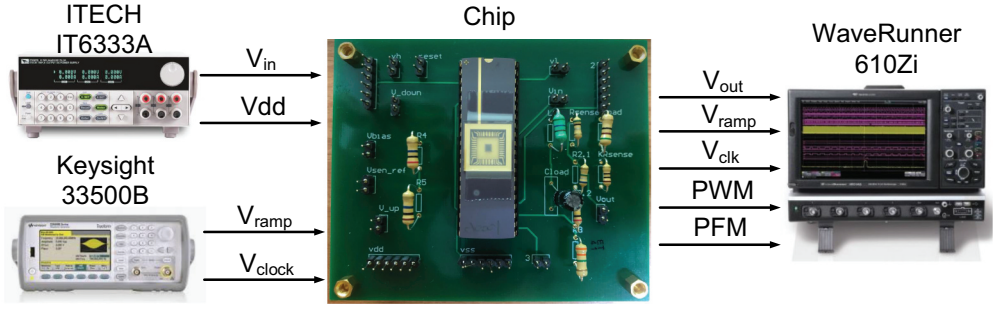


Figure 21. Measurement setup.

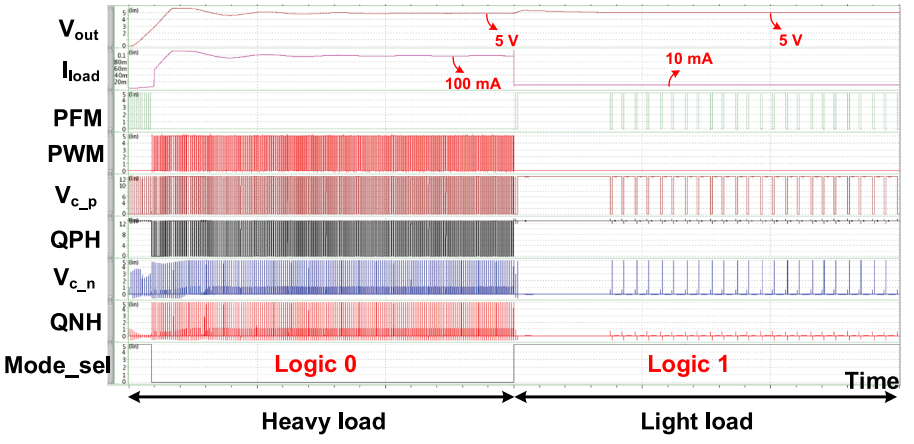


Figure 22. Waveform of the control circuits of the proposed buck converter at different load conditions.

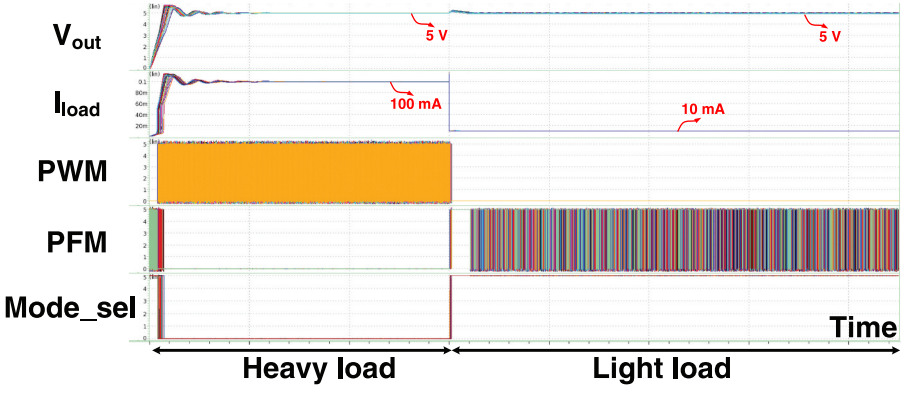


Figure 23. Waveform of the proposed buck converter at different load conditions.

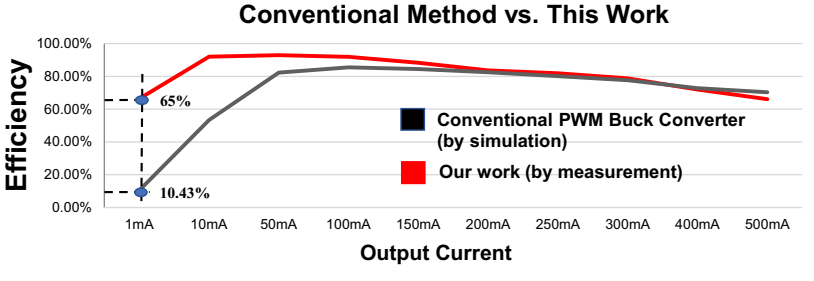


Figure 24. Efficiencies of the proposed buck converter vs. conventional PWM buck converter at different output currents.

conventional one. It is also higher compared to the previous work (Wang et al., 2022) which is about 30%. Equation (26) shows the calculation of the peak efficiency.

$$Efficiency = \frac{P_{out}}{P_{in}} = \frac{V_{out} \times I_{out}}{V_{in} \times I_{in}} \tag{26}$$

where $V_{out} = 5$ V, $I_{out} = 10$ mA, $V_{in} = 15$ V, and $I_{in} = 3.586$ mA. Figure 25 shows the output voltage waveform for an input voltage of 15 V at a peak efficiency of 92.95%. Meanwhile, Figure 26 shows the measured output voltage waveform at a light load current of 1 mA which shows the worst efficiency of 65% where the input voltage is 13 V and the output voltage is 4.91 V.

Table 2 summarises the performance comparison between the proposed converter with previous works. If the step-down ratio is taken into account, a Figure of Merit (FOM) is defined as the product of the step-down ratio and the efficiency. Notably, the converter of Ozanoglu and Dundar (2020) exhibited the highest peak

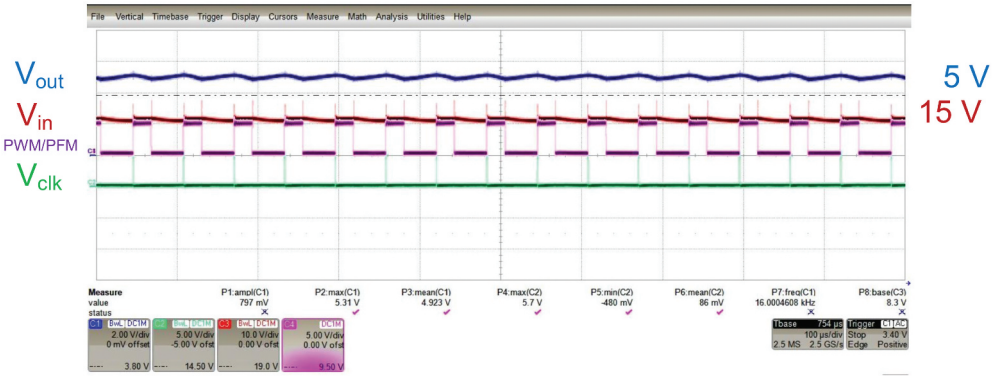


Figure 25. Output voltage waveform of the DC–DC converter at the peak efficiency of 92.95%.

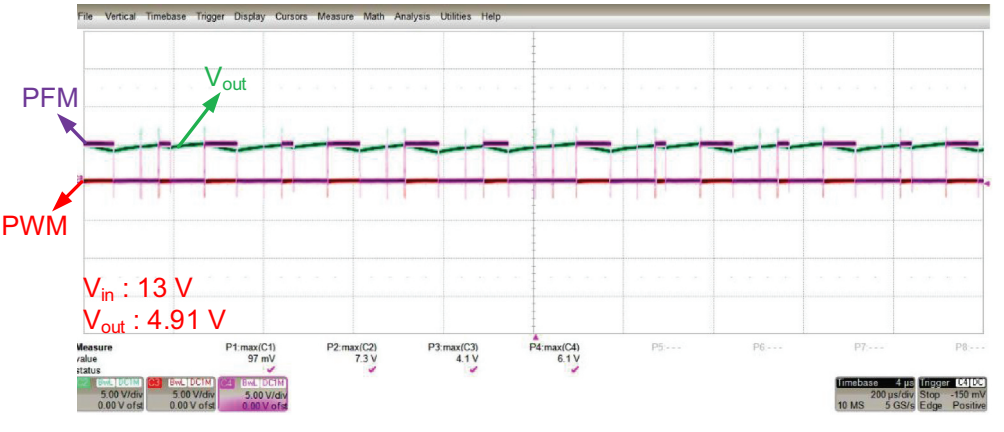


Figure 26. Output voltage waveform of the DC–DC converter at the worst efficiency of 65%.

Table 2. Performance comparison of the proposed work with the previous works.

	PEL[a]	VLSI[b]	JCSC[c]	CICC[d]	ICEIC[e]	IJEC[f]	IJEL[g]	This work
Year	1997	2015	2016	2017	2020	2020	2022	2022
Process	1.5-m CMOS	0.18-μm CMOS	0.35-μm BCDMOS	0.18-μm CMOS	65-nm CMOS	0.13-μm CMOS	0.5-μm HV CMOS	0.5-μm HV CMOS
Result[8]	Meas.	Meas.	Meas.	Meas.	Sim.	Sim.	Meas.	Meas.
Operation mode	PWM	DPWM	PWM/ PSM	Clock Hysteresis	PWM	PWM	PWM	PWM/ PFM
V_{in} (V)	5	3	6–30	2.4–3.3	1.8	3.8	10–14	12–15
V_{out} (V)	2.5	1	V_{in} − 3	1.5–1.6	1.2	1	5	5
Max. I_{out}	80 mA	1 μA	3A	10 mA	0.2 A	1.5 A	0.5 A	0.5 A
Output current range (mA)	20–80	0.00001–0.001	100–3000	0.0005–10	0–200	10–1500	4–500	1–500
Efficiency	60%	87%	92.90%	90.4%	92%	93%	91.68%	92.95%
Load Regulation (V/A)	N/A	N/A	0.320	N/A	N/A	N/A	N/A	0.551
Line Regulation (V/V)	N/A	N/A	N/A	0.111	N/A	N/A	N/A	0.056
Core Area (mm^2)	15.5	2.42	1.32	0.71	5.77	0.696	1.287	3.445
FOM	120	261	103.22	247	138	353.4	256.70	278.85

[1]Musunuri and Chapman (2005).
[2]El-Damak and Chandrakasan (2015).
[3]Li et al. (2016).
[4]Wu et al. (2017).
[5]Shin et al. (2020).
[6]Ozanoglu and Dundar (2020).
[7]Wang et al. (2022).
[8]Sim. = simulation; Meas. = Measurement.

efficiency and best FOM only based on simulation results presented. However, our design attains the best line regulation, peak efficiency, & FOM and the second best of load regulation and output current among all works with physical measurement results.

4. Conclusions

In this paper, a highly efficient dual-mode buck converter based on TSMC 0.5-μm HV CMOS process is proposed. Due to its dual-mode implementation, it maintained the output voltage and improved the conversion efficiency at different load conditions. It achieved the best efficiency and FOM and can be operated with a wide input voltage range among all reported works based on measurement results. Finally, it has better conversion efficiency than the conventional counterparts.

Acknowledgements

The authors would like to acknowledge Taiwan Semiconductor Research Institute (TSRI) for providing the EDA tool used in this study.

Disclosure statement

No potential conflict of interest was reported by the author(s).

Funding

This project was supported by the National Science and Technology Council (NSTC), Taiwan under grants NSTC 109-2218-E-110-007-, 109-2224-E-110-001-, 110-2221-E-110-063-MY2, and 110-2218-E-110-008-.

ORCID

Chua-Chin Wang http://orcid.org/0000-0002-2426-2879
Ralph Gerard B. Sangalang http://orcid.org/0000-0002-4120-382X
Oliver Lexter July A. Jose http://orcid.org/0000-0003-4565-9506

References

Ayachit, A. & Kazimierczuk, M. K. (2019, February). Averaged small-signal model of PWM DC-DC converters in CCM including switching power loss. *IEEE Transactions on Circuits & Systems II: Express Briefs*, *66*(2), 262–266. https://doi.org/10.1109/TCSII.2018.2848623

Baker, R. J. (2019). *CMOS: Circuit design, layout, and simulation*. John Wiley & Sons.

Bhattacharyya, K., Kumar, P. R., & Mandal, P. (2012, February). Improvement of power efficiency and output voltage ripple of embedded DC–DC converters with three step down ratios. *Journal of Circuits, Systems and Computers*, *21*(1), 1–23. https://doi.org/10.1142/S0218126612500077

El-Damak, D., & Chandrakasan, A. P. (2015, June). Solar energy harvesting system with integrated battery management and startup using single inductor and 3.2 nW quiescent power. In *Proc. 2015 Symposium on VLSI Circuits (VLSI Circuits)*, (pp. C280–C281), Kyoto, Japan. IEEE.

Kim, S., & Rincón-Mora, G. A. (2009, August). Achieving high efficiency under micro-watt loads with switching buck DC–DC converters. *Journal of Low Power Electronics*, *5*(2), 229–240. https://doi.org/10.1166/jolpe.2009.1023

Li, Z., Ji, Y., Yang, S., & Chang, Y. (2016, November). A dual-mode high-voltage high-efficiency peak-current-mode asynchronous buck converter. *Journal of Circuits, Systems and Computers*, *25*(11), 1–16. https://doi.org/10.1142/S021812661650136X

Lin, C.-C., Yang, L.-S., & Wu, G. W. (2013, June). Study of a non-isolated bidirectional DC-DC converter. *IET Power Electronics*, *6*(1), 30–37. https://doi.org/10.1049/iet-pel.2012.0338

Musunuri, S., & Chapman, P. L. (2005, September). Improvement of light-load efficiency using width-switching scheme for CMOS transistors. *IEEE Power Electronics Letters*, *3*(3), 105–110. https://doi.org/10.1109/LPEL.2005.859769

Ozanoglu, K., & Dundar, G. (2020, February). Buck converter with adaptive pass device employing capacitive and resistive power loss equalization. *AEU-International Journal of Electronics and Communications*, *115*, 1–9. https://doi.org/10.1016/j.aeue.2019.153060

Park, S. Y., Cho, J., Lee, K., & Yoon, E. (2015, December). A PWM buck converter with load-adaptive power transistor scaling scheme using analog-digital hybrid control for high energy efficiency in implantable biomedical systems. *IEEE Transactions on Biomedical Circuits and Systems*, *9*(6), 885–895. https://doi.org/10.1109/TBCAS.2015.2501304

Shin, H.-S., Lee, S.-H., Kim, J.-H., & Yang, B.-D. (2020, January). A simple ramp generator with an active ramp tracking control for a fast response PWM buck converter. In *Proc. 2020 International Conference on Electronics, Information, and Communication (ICEIC)*, Barcelona, Spain (pp. 1–4), Barcelona, Spain. IEEE.

Sipex. (2006, December). *Selecting Appropriate Compensation: Type-II or Type-III*. Retrieved from https://www.maxlinear.com/Files/Documents/sipex/ApplicationNotes/ANP-18_SelectTypeIIorTypeIII_120506.pdf.

Tolentino, L. K. S., Cruz, F. R. G., Garcia, R. G., & Chung, W.-Y. (2015, December). Maximum power point tracking controller IC based on ripple correlation control algorithm. In *Proc. 2015*

International Conference on Humanoid, Nanotechnology, Information Technology,Communication and Control, Environment and Management (HNICEM) (pp. 1–6), Cebu, Philippines. IEEE.

Wang, C.-C., Chen, C.-L., Sung, G.-N., & Wang, C.-L. (2011, May). A high-efficiency DC–DC buck converter for sub-2× VDD power supply. *Microelectronics Journal*, *42*(5), 709–717. https://doi.org/10.1016/j.mejo.2011.02.004

Wang, C.-C., Hou, Z.-Y., Lu, W.-J., & Wang, S.-S. (2016, November). High-voltage on-chip current sensor design and analysis for battery modules. *IET Circuits, Devices & Systems*, *10*(6), 492–496. https://doi.org/10.1049/iet-cds.2015.0374

Wang, C.-C., Huang, C.-Y., Lin, C.-H., Yeh, C.-H., Liu, G.-X., & Chou, Y.-C. (2020, December). 3D-modeling dataset augmentation for underwater AUV real-time manipulations. In *Proc. 2020 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)* (pp. 145–148), Ha Long, Vietnam. IEEE.

Wang, C.-C., Jose, O. L. J. A., Lou, P.-Y., Hsu, C.-J., Tolentino, L. K. S., & Sangalang, R. G. B. (2022, May). Single-chip DC–DC buck converter design based on PWM with high-efficiency in light load. *International Journal of Electronics Letters*, 1–13. https://doi.org/10.1080/21681724.2022.2068661

Wang, C.-C., Jose, O. L. J. A., Su, P.-K., Tolentino, L. K. S., Sangalang, R. G. B., Velasco, J. S., & Lee, T.-J. (2021, December). An adaptive constant current and voltage mode P&O-based Maximum Power Point Tracking controller IC using 0.5- μ m HV CMOS. *Microelectronics Journal*, *118*, 1–12. https://doi.org/10.1016/j.mejo.2021.105295

Williams, R. K., Grabowski, W., Cowell, A., Darwish, M., & Berwick, J. (1997, May). The dual-gate W-switched power MOSFET: A new concept for improving light load efficiency in DC/DC converters. In *Proceedings of 9th International Symposium on Power Semiconductor Devices and IC's* (pp. 193–196), Weimar, Germany. IEEE.

Wu, C.-S., Takamiya, M., & Sakurai, T. (2017, April). Buck converter with higher than 87% efficiency over 500nA to 20mA load current range for IoT sensor nodes by clocked hysteresis control. In *Proc. 2017 IEEE Custom Integrated Circuits Conference (CICC)* (pp. 1–4), Austin, TX. IEEE.

Zastrow, J. V., & Medeiros, H. D. S. (2021, March). Mathematical modeling and analysis of the DC–DC buck converter transient response. *Journal of Circuits, Systems and Computers*, *30*(4), 1–23. https://doi.org/10.1142/S0218126621500705