INTEGRATION, the VLSI journal 102 (2025) 102362

Contents lists available at ScienceDirect

Integration, the VLSI Journal

journal homepage: www.elsevier.com/locate/vlsi

An on-chip temperature sensor with 0.5 °C resolution and 0.34% linearity error using 180-nm CMOS process

Chua-Chin Wang [a,*,1], Pradyumna Vellanki [b], Shih-Heng Luo [b], Ralph Gerard B. Sangalang [c,d]

[a] Institute of Integrated Circuit Design, National Sun Yat-sen University, No. 70 Lien-hai Road, Gushan District, Kaohsiung City, 80424, Taiwan
[b] Department of Electrical Engineering, National Sun Yat-sen University, No. 70 Lien-hai Road, Gushan District, Kaohsiung City, 80424, Taiwan
[c] Department of Electronics Engineering, Batangas State University - The National Engineering University, Alangilan, Batangas City, 4200, Philippines
[d] Electronic Systems Research Center, Batangas State University - The National Engineering University, Alangilan, Batangas City, 4200, Philippines

ARTICLE INFO

Keywords:
Current to frequency conversion
High linearity
CTAT
PTAT
Current mirror
Temperature detection

ABSTRACT

This investigation demonstrates an on-chip temperature sensor with a maximum linear error less than 0.4% and 0.5 °C resolution. The design comprises Current-to-Frequency Converters (CFC), complementary (CTAT), and proportional (PTAT) to absolute temperature current generator circuits. Most important of all, the proposed sensor is featured with the ratio of these two currents to enhance the linearity and high resolution. The proposed sensor was realized using a 180-nm CMOS process. The core area is 0.196 mm^2. The measurement results show 0.3484% maximum linearity error for the PTAT/CTAT ratio. The maximum output frequency of the temperature detector is 4.817 MHz, with the highest power consumption of 20.13 mW. It was proved to be used in a –40 °C~100 °C temperature detection range with 0.5 °C resolution.

1. Introduction

Nowadays, security control and temperature detection are critical aspects in various industries, commercial applications, equipment systems, biomedical devices, etc., for many reasons. Excessive heat leads to the performance degradation of components such as integrated circuits, motors, and other sensitive parts, and increased temperatures often correlate with higher power consumption. Temperature monitoring systems with temperature sensors as a critical component play a vital role in maintaining the reliability, safety, and efficiency of industrial and commercial equipment and processes [1].

On-chip temperature sensors are becoming increasingly popular due to advancements in silicon technology. These sensors offer low power consumption, excellent accuracy, and compact size, and they can be integrated seamlessly into existing chips for monitoring temperatures. Most of the temperature sensors provide outputs in the forms of resistance, frequency, current, or voltage which are complementary or proportional to the measured temperature [2–7]. The signal-processing circuitry is usually incorporated for post-processing.

The report is divided into the subsequent sections. In Section 2, a comprehensive explanation of the circuit design is presented, including theoretical derivations of the proposed system. Section 3 encompasses the practical implementation of the circuit and the corresponding measurement outcomes. Lastly, Section 4 concludes the research.

2. Circuit design of the proposed temperature sensor

The proposed sensor consists of the following main parts: Current-to-Frequency Converters (CFC); a CTAT current generator; a PTAT current generator; and a Corner Detection Circuit, as shown in Fig. 1. The temperature of the circuit is first converted into a current and then into a frequency, respectively. A post-processing circuit, such as FPGAs, helps to process the signals in the form of frequencies.

Two major types of current generators, PTAT and CTAT, can be used to enhance the temperature sensor resolution through the process of division to generate the frequency ratio output, where temperature-dependent variations from each current partially will be canceled out, leaving a more stable and temperature-sensitive signal. As a result, the phase error is minimized in the PTAT/CTAT ratio output, reducing its impact on temperature readings and making the circuit response more consistent across temperature ranges. This approach allows the CFC circuit to more accurately represent the target temperature changes with better resolution, as small variations in temperature have a more pronounced effect on the output frequency ratio than if a single current with only one temperature coefficient were used. This enhancement ultimately improves the sensor's sensitivity and precision. In this manner, we may analyze the PTAT and CTAT behaviors to understand the influence of changes in temperature on the circuit during post-processing. Prior research usually featured outputs that were only

* Corresponding author.
E-mail address: ccwang@ee.nsysu.edu.tw (C.-C. Wang).
[1] Also with Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung City, 80424, Taiwan.

https://doi.org/10.1016/j.vlsi.2025.102362
Received 19 September 2024; Received in revised form 13 January 2025; Accepted 17 January 2025
Available online 24 January 2025

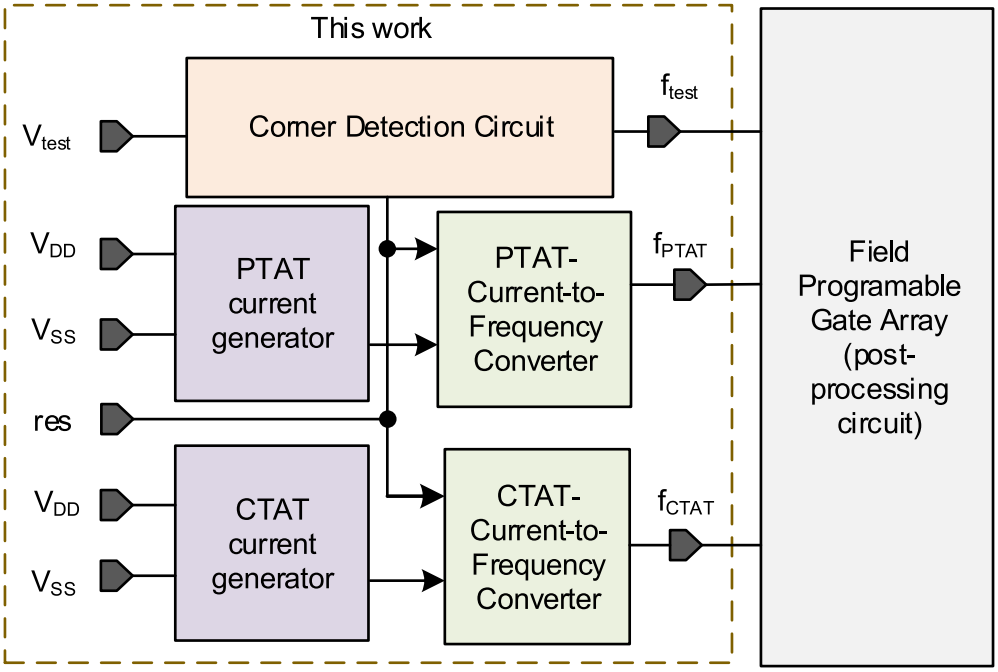

Fig. 1. Temperature sensor architecture.

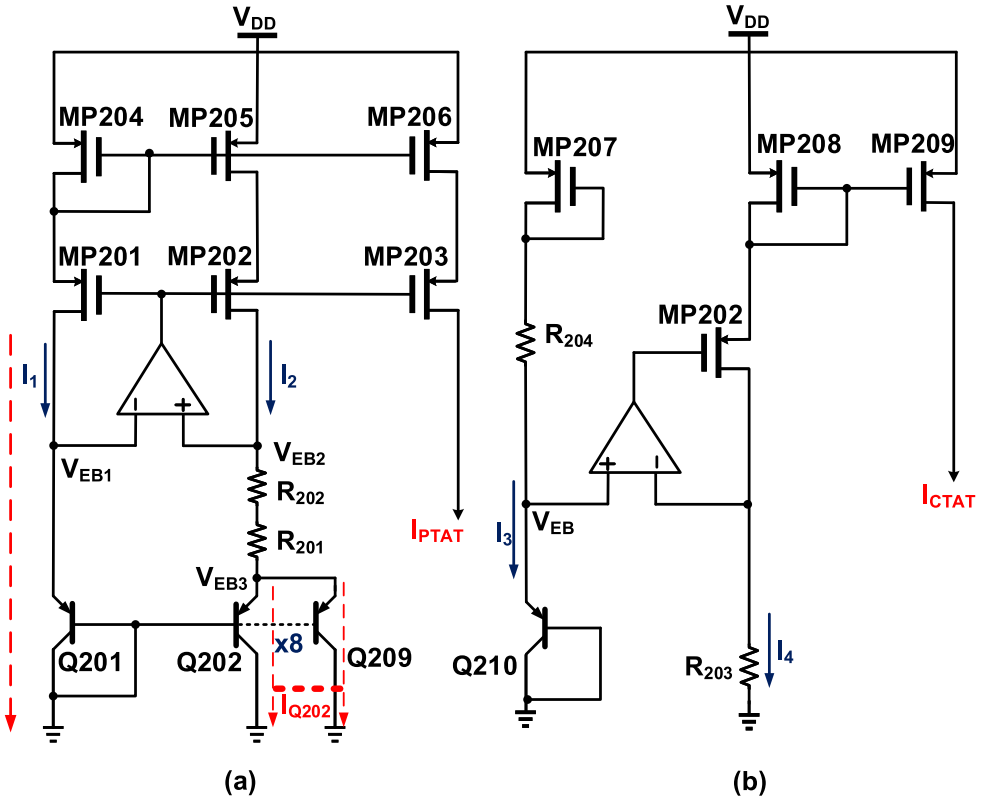

Fig. 2. (a) PTAT current generator; (b) CTAT current generator.

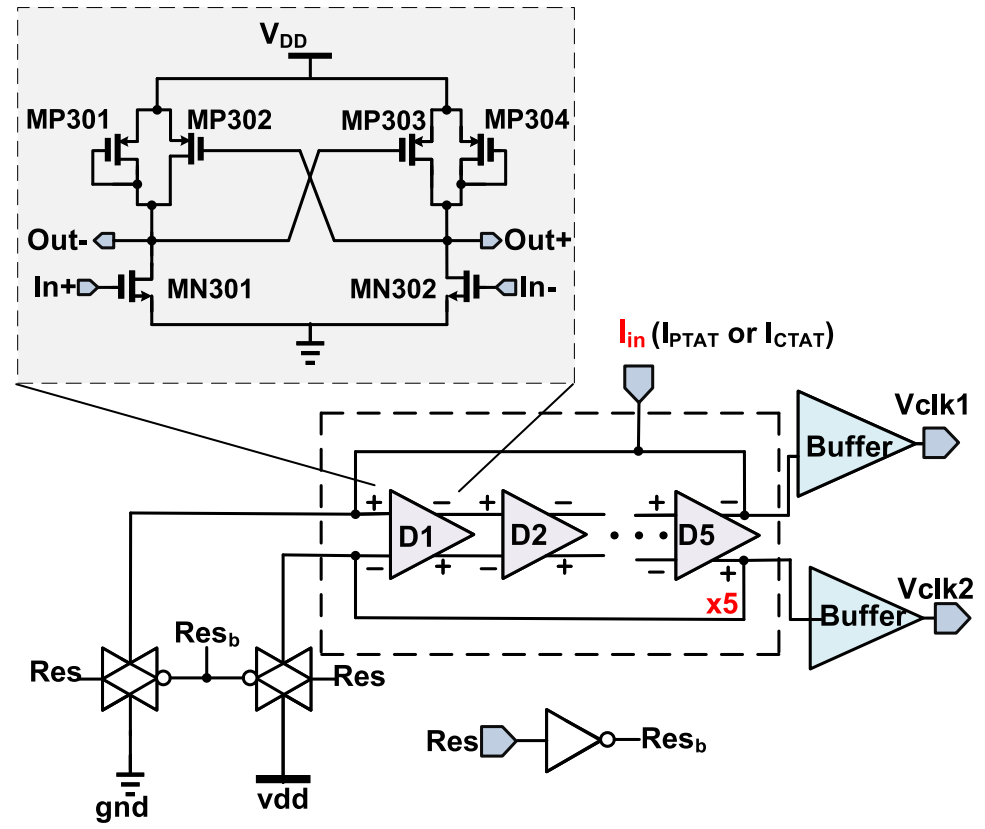

Fig. 3. Current-to-frequency converter (CFC).

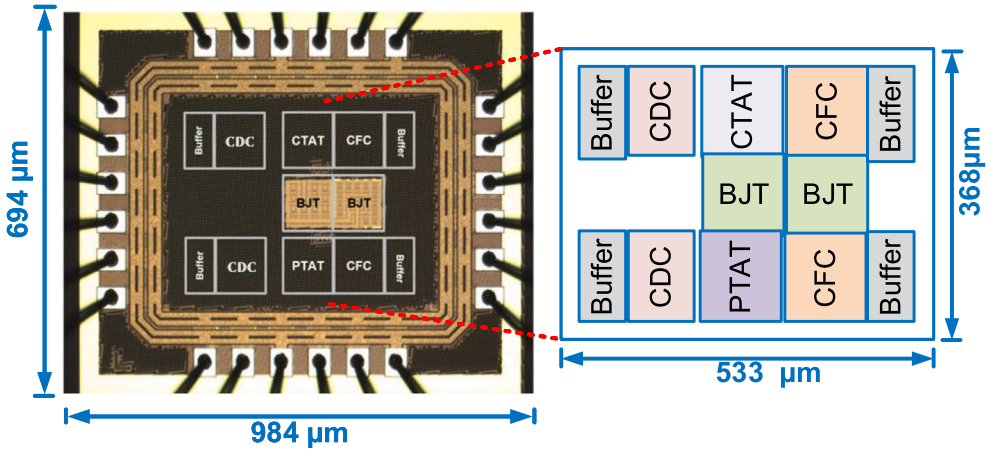

Fig. 4. Proposed temperature sensor die photo.

proportional to temperature. In-turns deprived linearity due to leakage threats and channel length modulation [2–4,8]. An exception was found in [9], but the temperature range in this report was very limited.

2.1. PTAT current generator

Fig. 2(a) shows the PTAT current generator in Fig. 1. The bandgap reference circuit takes advantage of the current in bipolar devices, which varies exponentially with the input voltage. The base-emitter potential of transistor Q201 is $V_{EB1}(T)$ and Q202 is $V_{EB3}(T)$ as shown in Eq. (1). Eq. (2) shows the relation between the current I_2 and I_{Q202}. The PTAT current equation is shown in Eq. (3). One more design decision taken was to use calibrated polysilicon (R_{201}) and N-WELL (R_{202}) resistors to mitigate first-order and second-order variations of temperatures [4]. Eq. (3) shows that the output current is proportional to variations in temperature.

$$V_{EB1}(T) = V_{EB2}(T) = V_T(T) \cdot \ln\left(\frac{I_1}{I_S}\right)$$
$$V_{EB3}(T) = V_T(T) \cdot \ln\left(\frac{I_{Q210}}{I_S}\right) \quad (1)$$

$$I_2 = 8 \times I_{Q202} \quad (2)$$

$$I_{PTAT}(T) = \frac{V_{EB2}(T) - V_{EB3}(T)}{R_{201}(T) + R_{202}(T)} = \frac{V_T(T) \cdot \ln(8)}{R_{total}(T)} = \frac{k \cdot T \cdot \ln(8)}{q \cdot R_{total}(T)} \quad (3)$$

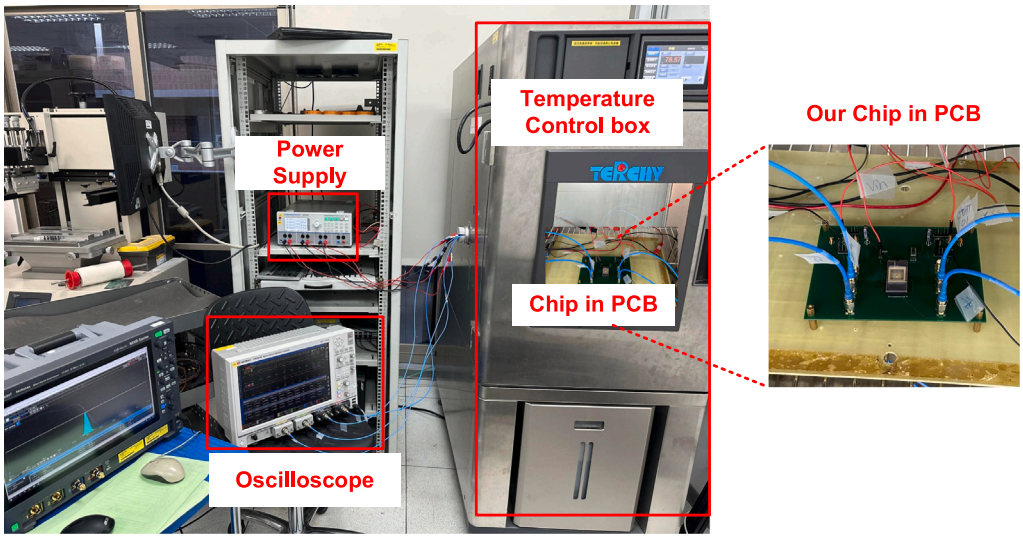

Fig. 5. Measurement setup at TSRI, Tainan.

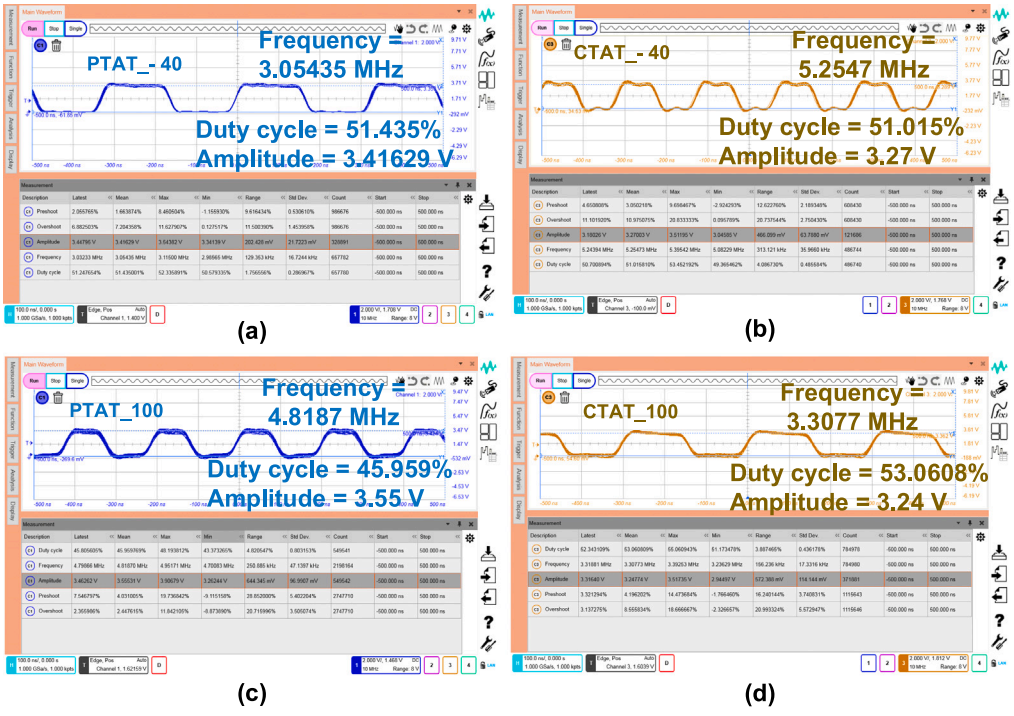

Fig. 6. The temperature to frequency measurement waveforms at (a) PTAT_-40 °C; (b) CTAT_-40 °C; (c) PTAT_100 °C; (d) CTAT_100 °C.

In Eq. (3), $V_T(T)$ denotes the thermal voltage, k stands for Boltzmann's constant, $R_{total}(T)$ represents the series combination of polysilicon resistor (R_{201}) and N-WELL resistor (R_{202}), and q denotes the charge of an electron.

2.2. CTAT current generator

According to Fig. 2(b), the low dropout (LDO) regulator current mirror is the basis of the CTAT current generator. To achieve the CTAT behavior, the design makes use of the temperature coefficient of R_{203}. The CTAT current equation is given in Eq. (4). It is obtained as a mirror current, that is flowing through the resistor R_{203}, namely, $I_4(T)$, by the regulated voltage $V_{EB}(T)$, where $V_{EB}(T)$ is the voltage drop in transistor Q210. Eq. (5) illustrates the temperature-induced fluctuation in the current, which is derived using the chain rule of differentiation as shown in Eq. (6). If the second term in Eq. (6) is much less than the first term, the output current will exhibit CTAT behavior.

$$I_{CTAT}(T) = I_4(T) = \frac{V_{EB}(T)}{R_{203}(T)} \tag{4}$$

$$\frac{\partial I_{CTAT}(T)}{\partial T} = \frac{\partial}{\partial T}\left(\frac{V_{EB}(T)}{R_{203}(T)}\right) \tag{5}$$

$$\frac{\partial I_{CTAT}(T)}{\partial T} = -\frac{V_{EB}}{R_{203}^2} \cdot \frac{\partial R_{203}(T)}{\partial T} + \frac{1}{R_{203}} \cdot \frac{\partial V_{EB}(T)}{\partial T} \tag{6}$$

2.3. Current-to-Frequency Converter (CFC)

An all-MOS voltage-to-frequency converter, based on capacitor charging and discharging cycles, provides a very low frequency difference per degree and lower stability [10,11]. An oscillator based on

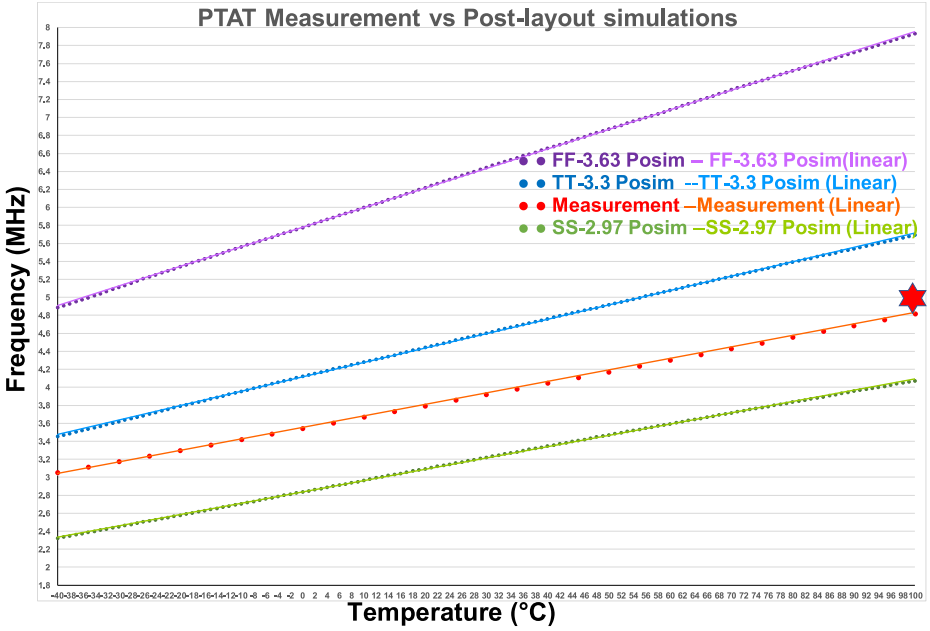

Fig. 7. The PTAT temperature vs. frequency curves for TT, FF, SS corners.

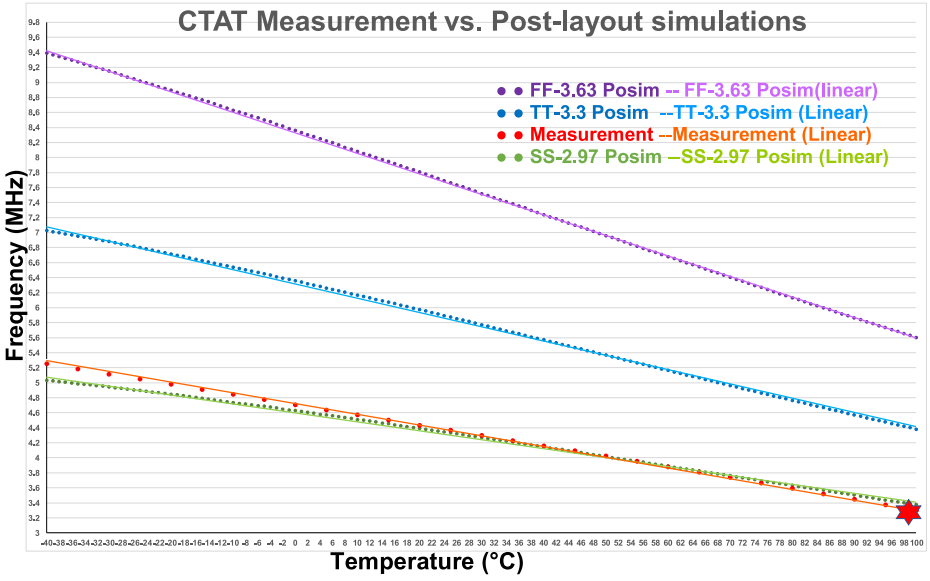

Fig. 8. The CTAT temperature vs. frequency curves for TT, FF, SS corners.

current-starved delay provides low linearity and insufficient frequency difference per degree [12]. As a trade-off, a differential ring oscillator is designed for current-to-frequency conversion to achieve high linearity, and a high frequency difference per degree. The schematic of the differential ring oscillator utilized to convert current to frequency is illustrated in Fig. 3. This oscillator is composed of a startup circuit and five stages of differential ring oscillators. The currents $I_{PTAT}(T)$ and $I_{CTAT}(T)$ are given to input terminal I_{in} in PTAT-CFC and CTAT-CFC, these currents drive the MN301 transistor in the oscillator. To achieve an optimal balance between linearity and resolution, each stage of the oscillator employs a differential pair based on symmetrical load cross-coupling, as emphasized in Fig. 3. The estimated oscillator frequency is stated in Eq. (7) [13]. The current driving the oscillator (I_{in}) is the same as the $I_{PTAT}(T)$ and $I_{CTAT}(T)$ mentioned earlier, thus obtaining a linear positive and negative temperature coefficient frequency output.

$$f_{osc} = \frac{1}{2N \cdot T_{delay}} \tag{7}$$

In Eq. (7), N denotes the number of stages in the ring oscillator, and T_{delay} denotes the delay per stage.

$$T_{delay} = \frac{C_L \cdot V_{swing}}{I_{in}} \tag{8}$$

In Eq. (8), V_{swing} means Voltage swing (typically V_{DD} or a fraction of it) and C_L is the load capacitance of each stage. Combining the Eqs. (7) and (8), the oscillator frequency is:

$$f_{osc} = \frac{I_{in}}{2N \cdot C_L \cdot V_{swing}} \tag{9}$$

2.4. Corner Detection Circuit (CDC)

The Corner Detection Circuit in Fig. 1 is an autonomous current-to-frequency converter, with the identical structure the same as Fig. 3, which is present on the same chip [14]. This additional information

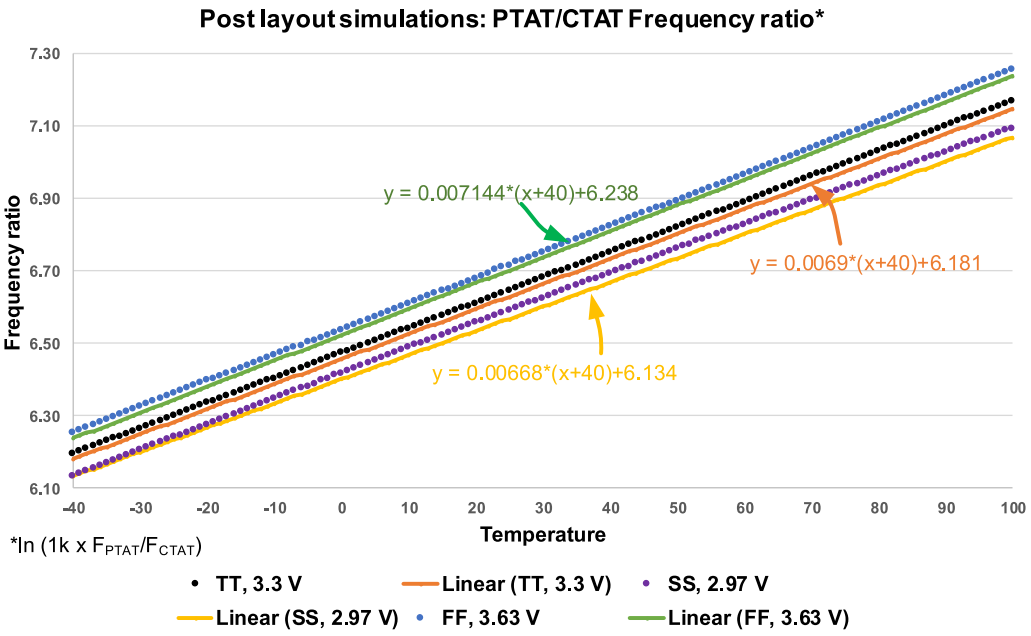

Fig. 9. The PTAT/CTAT frequency ratio curves by post-layout simulations.

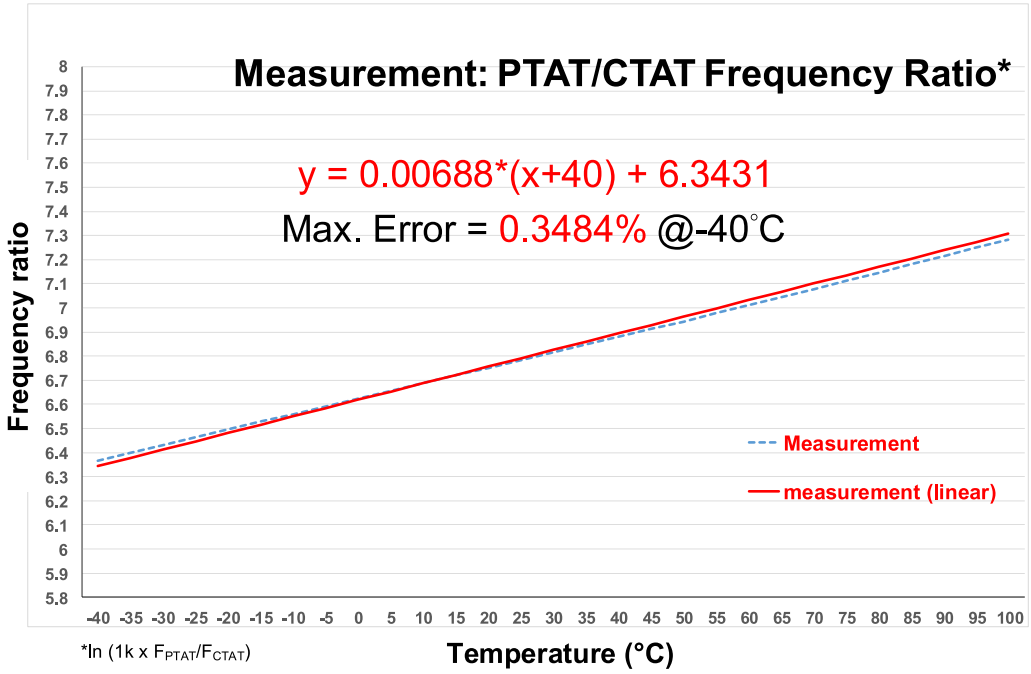

Fig. 10. The PTAT/CTAT curve.

helps to estimate the corner status of the chip. The frequency output of the CDC has significant differences, allowing it to be useful for further process corner predictions.

3. Measurement and analysis

The die photo with the floor plan of the proposed temperature sensor is shown in Fig. 4. The sensor was designed and fabricated using a typical 180-nm CMOS technology. Its full chip area and core area are 694 × 984 μm^2 and 368 × 533 μm^2, respectively. Fig. 5 depicts the measurement setup.

Fig. 6 displays the measurement results obtained at temperatures −40 °C and 100 °C for PTAT and CTAT currents. The current-to-frequency conversion for PTAT currents yields frequencies of 3.05435 MHz, 3.54649 MHz, 3.9223 MHz, and 4.8187 MHz at −40 °C, 0 °C, 30 °C, and 100 °C, respectively. Similarly, for CTAT currents, the frequencies attained are 5.2547 MHz, 4.71105 MHz, 4.30293 MHz, and 3.3077 MHz, respectively.

Figs. 7 and 8 show the PTAT and CTAT temperature vs. frequency curves for TT, FF, and SS corners simulation, and the measurement, respectively. In the post-layout simulations, as a worst-case scenario, 0.466% @ 37 °C and 0.871% @ 15 °C maximal errors are possessed by the PTAT and CTAT currents, respectively in the SS corner.

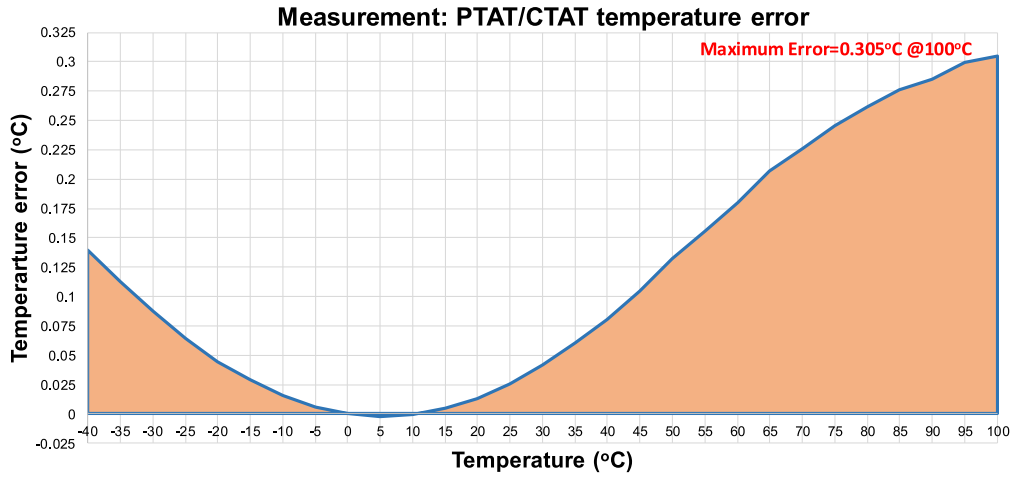

Fig. 11. Measured temperature error.

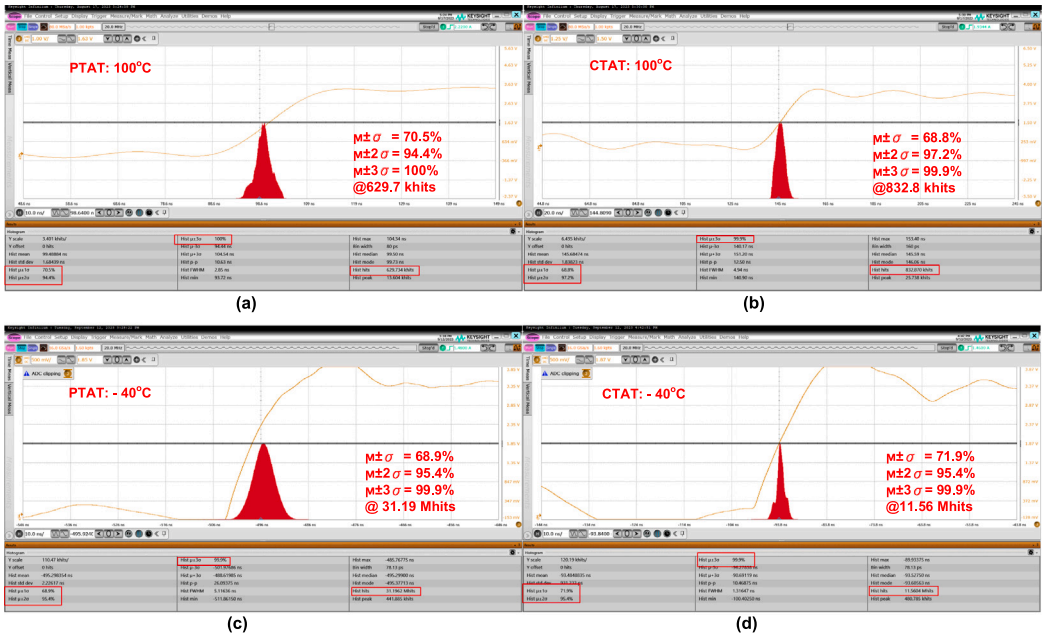

Fig. 12. Histograms of (a) PTAT at 100 °C; (b) CTAT at 100 °C; (C)PTAT at −40 °C and; (d) CTAT at −40 °C.

In Fig. 9, the post-layout simulations of PTAT/CTAT frequency ratio curve for −40 °C to 100 °C temperature range is depicted. The post-layout simulation results for three different corners [SS, VDD-10%], [TT, VDD], and [FF, VDD+10%] demonstrate that the PTAT/CTAT frequency ratio is predominantly influenced by temperature, exhibiting a PTAT behavior. In the post-layout simulations of PTAT/CTAT frequency ratio curve, as a worst-case scenario, 0.406% @ 51 °C maximum linearity error is obtained in the [SS, VDD-10%] corner.

In the measurement results, the temperature sensor also showed high linear characteristics. The maximum error for the PTAT current is 0.436% at 50 °C, and the CTAT current is 0.724% at −40 °C. Based on these findings, our temperature sensor operates between the corners of SS and TT by post-simulation results [14].

The utilization of PTAT and CTAT currents offers significant advantages in temperature measurement. These currents inherently compensate for process variations and improve linearity in the CFC by leveraging their predictable temperature dependence. This synergy ensures reliable temperature measurements under varying conditions.

We can take advantage of the temperature sensor's PTAT and CTAT currents. Correlating these currents increases linearity. The ratio is proportional to the temperature and possesses the linear property as shown in Fig. 10 with a 0.3484% maximum linearity error.

The measured temperature error of our sensor is shown in Fig. 11. The maximum error is 0.305 °C @ 100 °C. The frequency histograms measured at 100 °C, and −40 °C temperatures can be analyzed to assess the stability of the frequency distribution, as shown in Fig. 12. The sample size comprises tens of millions of data points. At each temperature, the frequencies of PTAT and CTAT fall within three standard deviations, satisfying the reliability criteria. Fig. 13 displays the eye diagram of the PTAT output at temperatures of −40 °C and 100 °C. The eye width is measured at 100.61 ns and 88.47 ns, with corresponding eye heights of 1.738 V and 1.203 V. The jitter RMS values are recorded as 10.95 ns and 3.20 ns, respectively. On the other hand, Fig. 14 exhibits the eye diagram of the CTAT output at the same temperatures. The eye width is measured at 82.686 ns and 111.4 ns, with corresponding eye heights of 511 mV and 1.593 V. The jitter RMS values are recorded as 2.11 ns and 6.34 ns, respectively. It is evident that as the temperatures increase, the eye width decreases in PTAT and increases in CTAT. This observation indicates an inverse relationship between the eye width and the output frequency.

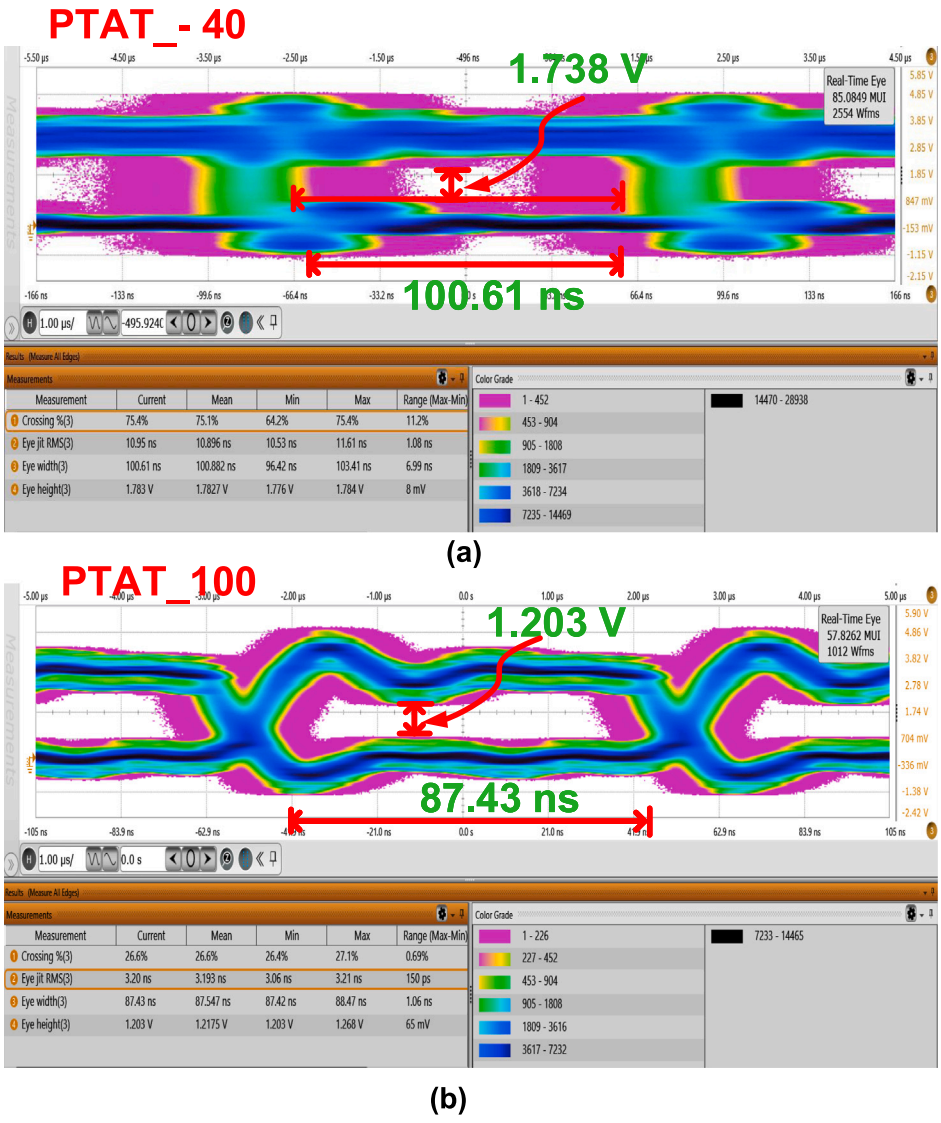

Fig. 13. PTAT Eye diagram of our temperature sensor at (a) −40 °C and ; (b) 100 °C.

The performance of different temperature sensors in previous years is summarized in Table 1. It can be observed that 0.5 °C is the best resolution attained by our design. In terms of the linearity, our design has the highest linearity in both post-layout and measurement outcomes namely 0.466% and 0.3484%, respectively. The maximum temperature error observed in the measurement is 0.305 °C @ 100 °C. Our temperature sensor is compared with previous temperature sensors using an FOM, which includes the temperature range (°C), temperature detection error (°C), and the linearity error (%). The technology roadmap is shown in Fig. 15. Based on this figure, we are assured to state that our approach is the best so far of all the different temperature sensors mentioned [3,7,15–17].

4. Conclusion

This investigation presents a temperature sensor developed using the TSMC 180-nm CMOS process. A −40 °C ~ 100 °C of temperature range with a 0.5 °C resolution is detected by the sensor. Based on the measurement results, this sensor demonstrates excellent linearity, with a maximum linearity error of only 0.3484%. Overall, this on-chip temperature sensor offers accurate and reliable temperature detection within a wide range, making it suitable for various applications.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

TSRI in NARL is recognized for the substantial EDA assistance provided. Partial funding for this work has been provided by NSTC of Taiwan through Grants NSTC 112-2218-E-110-005-, NSTC 112-2221-E-110-063-MY3, and NSTC 112-2218-E-110-009-.

Data availability

Data will be made available on request.

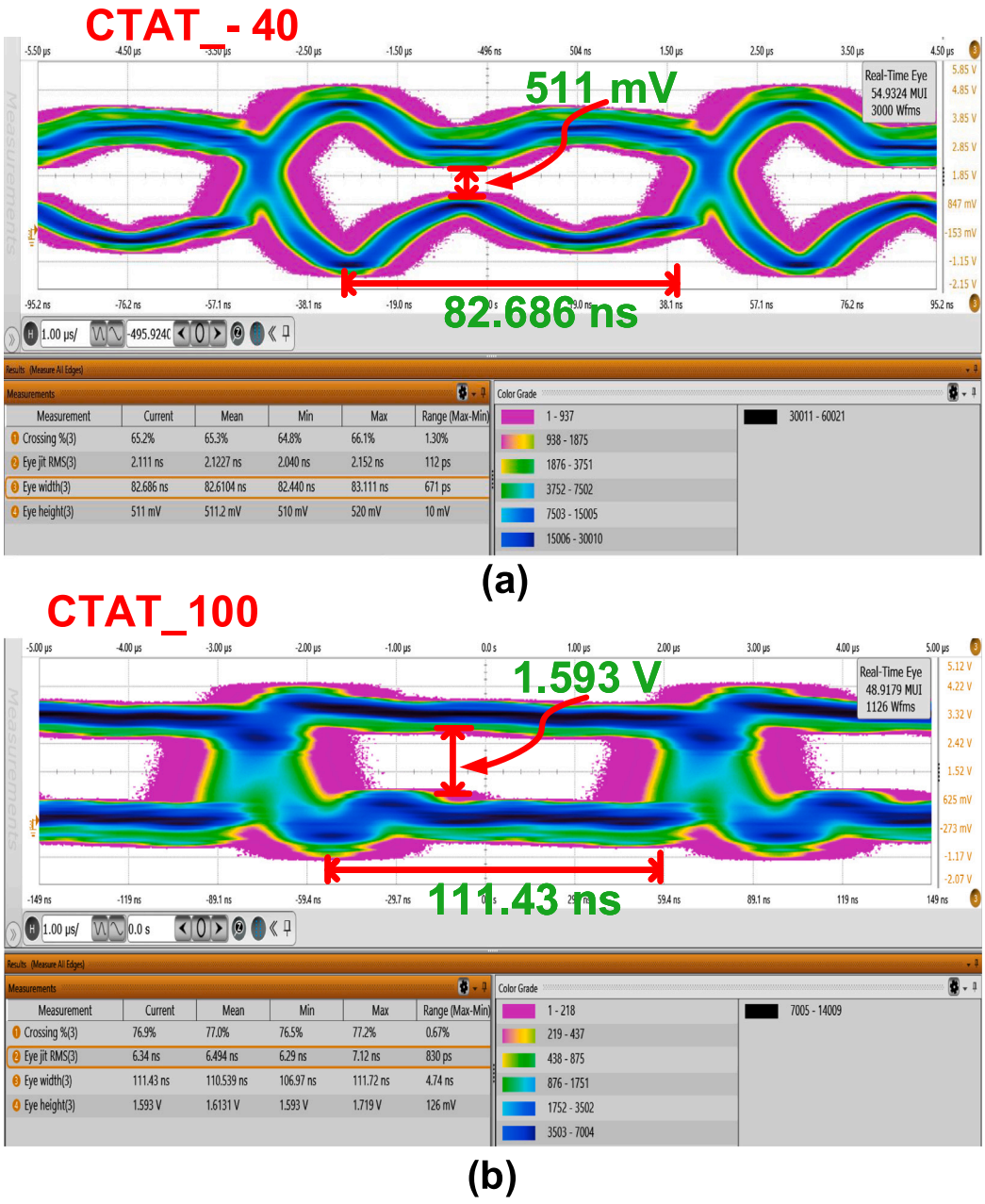

Fig. 14. CTAT Eye diagram of our temperature sensor at (a) −40 °C and ; (b) 100 °C.

Table 1
Table of performance comparisons with prior works.

	[3]	[8]	[15]	[16]	[6]	[17]	[7]	[18]	Ours
Year	2013	2015	2017	2018	2019	2020	2021	2023	2024
Process (μm)	0.18	0.25	0.18	0.5 (HV)	0.065	0.065	0.18	0.18	0.18
Verif.	Meas.	Meas.	Meas.	Meas.	Simu.	Meas.	Simu.	Meas.	Meas.
VDD (V)	1.2	5	0.6	5.0	0.8	0.9	3.3	1	3.3
Core area (mm^2)	0.09	0.09	0.45	2.39	N/A	0.32	1.64	0.055	0.196
Power (mW)	0.000065	0.384	0.0000297	11	0.0009	0.00000064	48.5	0.00002	20.13
f_{out} (kHz)	175~ 275	N/A	29.95	1620~ 2270	60~ 85	N/A	403~ 465	2.8~ 560	3054~ 4817
Temp. range (°C)	0~ 100	−40~ 150	0~ 100	−5~ 40	0~ 80	−30~ 70	−40~ 80	0~ 100	−40~ 100
Res. (°C)	0.3	N/A	0.1	1	1	N/A	3	0.03	**0.5**
Temp. error (°C)	1.3	2.06	−1.6	1.01	−1	−1	0.5	0.8	**0.305**
Lin. error (%)	0.974	N/A	5.5	1.42	N/A	1.7	0.392	N/A	**0.3484**
FOM	78.98	N/A	11.36	31.38	N/A	58.82	612.24	N/A	**840.66**

FOM = Temp. Range/(Temp. Error × Lin. Error).

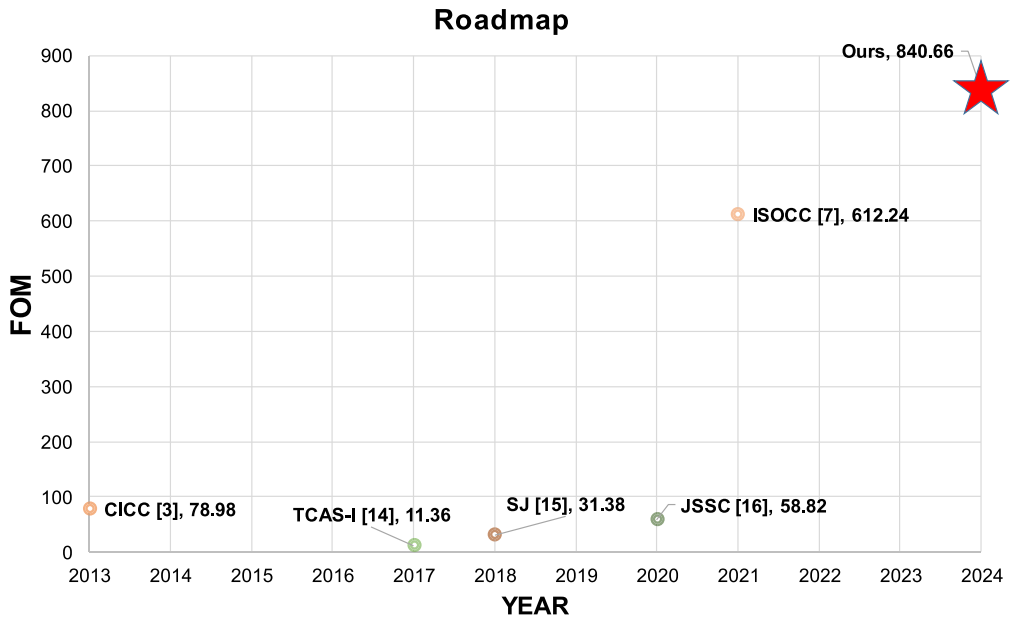

Fig. 15. Technology roadmap of temperature sensors.

References

[1] C.-Z. Shao, Y.-T. Liao, A 950-pW, 39-pJ/conversion leakage-based temperature-to-digital converter with 43 mK resolution, in: Proc. 2020 IEEE Asian Solid-State Circuits Conf, A-SSCC, 2020, pp. 1–4.

[2] C.-C. Wang, W.-J. Lu, T.-Y. Tsai, T.-C. Wu, C.-Y. Juan, A temperature detector with process compensation and non-linear calibration for battery management systems with HV ESD protection, in: Proc. 2013 Int. SoC Des. Conf, ISOCC, 2013, pp. 095–098.

[3] S. Jeong, J.-Y. Sim, D. Blaauw, D. Sylvester, 65 nW CMOS temperature sensor for ultra-low power microsystems, in: Proc. IEEE 2013 Custom Integr. Circuits Conf, 2013, pp. 1–4.

[4] C.-C. Wang, W.-J. Lu, T.-C. Wu, C.-Y. Juan, A CMOS wide-range temperature sensor with process compensation and second-order calibration for battery management systems, in: Proc. 2014 IEEE Int. Symp. Circuits Syst, ISCAS, 2014, pp. 586–589.

[5] S. Joshi, P.K. Jain, Design of 180 nm CMOS linear temperature sensor, in: Proc. 2017 Int. Conf. Recent Innovations Signal Process. Embedded Syst, RISE, 2017, pp. 469–472.

[6] H. Shi, B. Zhou, F. Zhao, A high-linear low-power temperature-to-frequency converter with high robustness, in: Proc. 2019 IEEE 3rd Adv. Inf. Manage. Communicates Electron. Autom. Control Conf, IMCEC, 2019, pp. 828–831.

[7] P.-Y. Lou, Y.-X. Chen, C.-C. Wang, On-chip CMOS corner detector design for panel drivers, in: Proc. 2021 18th Int. SoC Des. Conf, ISOCC, 2021, pp. 11–12.

[8] C.-C. Wang, W.-J. Lu, T.-Y. Tsai, Analysis of calibrated on-chip temperature sensor with process compensation for HV chips, IEEE Trans. Circuits Syst. II 62 (3) (2015) 217–221.

[9] R.G.B. Sangalang, C.-L. Lee, Y.-W. Shen, C.B. Co, C.-C. Wang, A 4–kHz per °C high linearity temperature sensor implemented using 40–nm CMOS process, in: Proc. 2023 IEEE Asia-Pac. Conf. Circuits Syst, 2023.

[10] C.-C. Wang, T.-J. Lee, C.-C. Li, R. Hu, An all-MOS high-linearity voltage-to-frequency converter chip with 520-kHz/V sensitivity, IEEE Trans. Circuits Syst. 53 (8) (2006) 744–747.

[11] P. Vellanki, H.-C. Tseng, Y.-X. Chen, L.S.S.P. Kumar Chodisetti, C.-C. Wang, An on-chip temperature sensor with 1 °C resolution and wide detection range using 180-nm CMOS process, in: Proc. 2024 21st International SoC Design Conference, ISOCC, 2024, pp. 11–12.

[12] J.A. McNeill, D.S. Ricketts, Low jitter VCO design examples, in: The Designer's Guide To Jitter in Ring Oscillators, Springer, New York, USA, 2009, pp. 239–242, ch.9.

[13] S. Docking, M. Sachdev, A method to derive an equation for the oscillation frequency of a ring oscillator, IEEE Trans. Circuits Syst. I 50 (2) (2003) 259–264.

[14] R.G.B. Sangalang, S.-H. Luo, C.-C. Wang, A high resolution and wide range temperature detector using 180-nm CMOS process, in: Proc. 2023 Int. Conf. IC Des. Tech, ICICDT, 2023, pp. 64–67.

[15] X. Wang, P.-H.P. Wang, Y. Cao, P.P. Mercier, A 0.6 V 75 nW all-CMOS temperature sensor with 1.67 m°C/mV supply sensitivity, IEEE Trans. Circuits Syst. I 64 (9) (2017) 2274–2283.

[16] C.-C. Wang, Z.-Y. Hou, J.-C. You, Temperature-to-frequency converter with 1.47% error using thermistor linearity calibration, IEEE Sens. J. 19 (13) (2019) 4804–4811.

[17] T. Someya, A.K.M.M. Islam, K. Okada, A 6.4 nW 1.7% relative inaccuracy CMOS temperature sensor utilizing sub-thermal drain voltage stabilization and frequency-locked loop, IEEE Solid- State Circuits Lett. 3 (2020) 458–461.

[18] J. Li, B. Yao, L. Fan, T. Zhang, Y. Zhang, K. Wu, Z. Zhang, Q. Zhang, Y. Wang, N. Ning, Q. Yu, A 20 nW +0.8 °C/-0.8 °C inaccuracy (3σ) leakage-based CMOS temperature sensor with supply sensitivity of 0.9 °C/V, IEEE Trans. Circuits Syst. I 70 (8) (2023) 3142–3153.