RESEARCH ARTICLE

A Power-Efficient 0.5668 TOPS/W Digital Logic Accelerator Implemented Using 40-nm CMOS Process for Underwater Object Recognition Usage

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ABSTRACT DNN (deep neural network) and CNN (convolution neural network) have been widely used in real-time artificial intelligent (AI) applications, particularly image or video recognitions, because they have been proved physically in many occasions. However, most prior AI hardware works either suffered from high on-silicon area cost or low usage thereof. This investigation presents a power efficient and high performance implementation of a digital logic accelerator (DLA) for the real-time underwater object recognition. The proposed DLA is also featured with 2-dimensional PE (processing element) array to increase the processing throughput by the enhancement of parallelism. The DLA design was realized and fabricated using TSMC 40-nm CMOS process. Not only the post-layout simulation results are shown, the on-silicon measurement outcome as well as the system validation in water are also demonstrated to prove the function correctness and the performance. The area efficiency (GOPS/mm^2) is 4.562, and the power efficiency (TOPS/W) is 0.5668 on silicon, which both are the best to date.

INDEX TERMS Deep neural networks (DNN), digital logic accelerator (DLA), high degree of parallelism, underwater object recognition, low power.

I. INTRODUCTION

Artificial intelligence (AI) has been booming in the past years owing to its capacity to discover unnoticed patterns and links within data sets such that it paves the way for data fusion and decision making, which is considered to be superior in certain occasions to human capabilities especially in the field of medical diagnosis, anomaly detection, financial fraud detection, real-time sensor data analysis, and predictive maintenance. AI based on neural networks utilizing electronics become field applications that greatly benefited the fields of sound processing, video processing, communication systems,

pattern analysis, etc. Notably, the core of the neural network applications is either CNN or DNN, which is inspired by extracting features in a small region of a specific specimen to attain patterns in other regions thereof. Most of prior reports were focused on development of better algorithms to achieve detection and prediction with high accuracy and fast convergence. Apparently, the overhead is high complexity to realize these algorithms. Thus, the electronic platforms for the developed complicated algorithms are composed of CPUs, GPUs, and maybe FPGAs, which are all power hungry devices.

As pointed out earlier, one of the biggest challenges in AI-related applications is to equip AI hardware into applications where the power/energy source is limited, such as
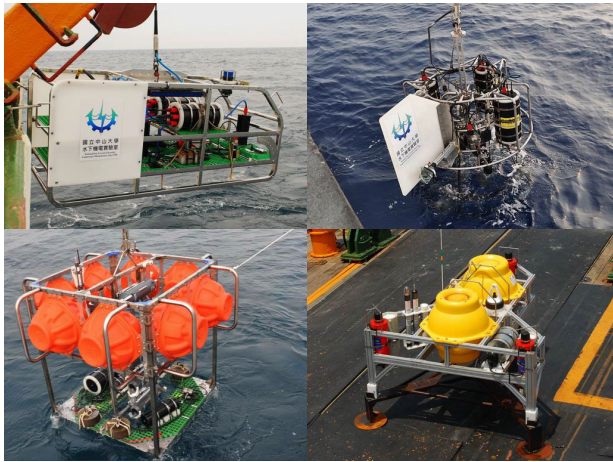
The associate editor coordinating the review of this manuscript and approving it for publication was Mario Donato Marino.

FIGURE 1. Underwater vehicles developed at NSYSU [1].

battery-powered autonomous underwater vehicles (AUV), as shown in Fig. 1 [1]. It is impossible to supply enough power directly and constantly to such underwater systems to carry out all the required missions. That is, the overall power in these underwater applications is constrained by the battery size of the vehicle systems. Several works were reported to be focused on the control architectures of an AUV to gain efficient computing capability hence, also saving energy resource [2], [3], [4]. Wang et al. [5] used artificial lateral line systems (ALSS) to detect moving objects while Tian et al. [6] focused on energy efficient underwater acoustic networks. Huang et al. [7] on the other hand proposed a finite-time distributed control that is used to control multiple AUVs. Besides the development of light-weight training algorithms, another approach is to seek more power-efficient hardware solutions to overcome the mentioned power limitation issues for these battery-driven AI systems.

Many research teams already put out tremendous efforts to resolve the power-effective AI hardware demand. For instance, Reck et al. presented one interesting design for chip-integrated optical neural networks [8]. The feature is that they proposed to use optical device, which are considered to attain less power consumption, to overcome the power hungry problems encountered by electronic platforms. However, the overhead caused by the interfacing circuits to carry out optical-electrical data conversion was ignored. Another similar approach was reported, combining the capabilities of electronic and optical neural networks [9], where data transfers between layers and modules can be done at the speed of light using high speed fiber optic cables. Again, the overhead for signal conversions between electrical domain and optical domain in such an approach was not seriously considered and analyzed.

Many researchers still paid their attention to existing CMOS-based electronic solution such that many AI hardware accelerators have been reported in past years. The systolic architecture has reconfigurable designs for different convolution kernels [10], [11], [12], [13], [14], [15], [16], [17], etc. However, a large area overhead becomes the cost to pay

due to the complexity of the control structure is found [10]. The systolic data flow is only allowed to run in the PE rows rather than the entire 2D plane to achieve data reuse of filters along with convolution kernel reuse, which results in throughput degradation [11]. Another hardware design is the spatial architecture reported in [12], which is an improved version of [13]. It mainly took advantage of clustering of sparse CNNs to achieve higher throughput, but it required a larger area. A filter and input reuse in the streaming architecture was reported to be energy efficient, but it has a low hardware utilization [14]. A potential optical solution to realize DNN was reported by Sangalang, et al., [18]. However, this report was simply a proof of concept research and it was not really realized for underwater applications, either. The only DNN/CNN research report dedicated for underwater object recognition was given in [19], where sophisticated algorithms were introduced in detail. However, their proposed methods were never implemented on hardware to prove the feasibility. More importantly, none of the above works were focused on power-limited underwater object recognition applications.

A. CONTRIBUTIONS OF THIS WORK
Considering the above existing difficulties in the realization of AI applications in underwater edge devices, particularly in the battery-operated edge devices, e.g., AUVs, novel DLA featured with high degree of hardware parallelism is disclosed in this investigation so that the throughput would not be degraded due to the limited power and the simplification of DNN/CNN architectures besides the adoption of a light weight YOLOv3-tiny algorithm.

II. LOW-POWER AND HIGH-THROUGHPUT DLA DESIGN
Fig. 2 shows the required interface for the proposed DLA to co-work with auxiliary circuits. Besides the AXI wrapper, the control and data paths of accelerator, DMA, and Inter-Controller are also defined to drive the DLA. More specifically, the circuitry in the green dashed area is meant to serve as the wrapper I/Os, where many channels are needed to carry out the AXI protocol. The blue dashed area mainly consisting of controller circuitry in charge of the state transition of a FSM (finite state machine) generating all the commands of data flow control, instruction control, and timing control. Last but not least, the yellow area is the core of DLA where all the convolution operations, MAC computation and management, and realization of parallelism are realized.

A. DLA HARDWARE ARCHITECTURE
Referring to Fig. 2 again, the proposed DLA is mainly composed of a DNN Accelerator, an Inter-controller, and a AXI Wrapper Direct Memory Access (DMA). Most importantly, the DNN Accelerator consists of an 8×32 PE array to increase the degree of parallelism, an intra-controller, SRAMs, reshape modules, and line buffers. Apparently, the core of DNN or CNN is the convolution operation, namely MAC operations. To elevate the throughput without serious power overhead, the convolution operation is realized by
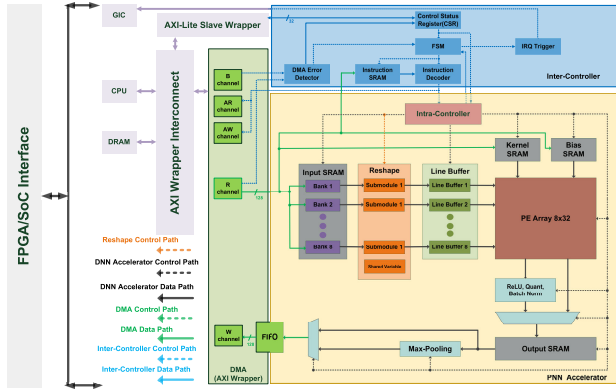
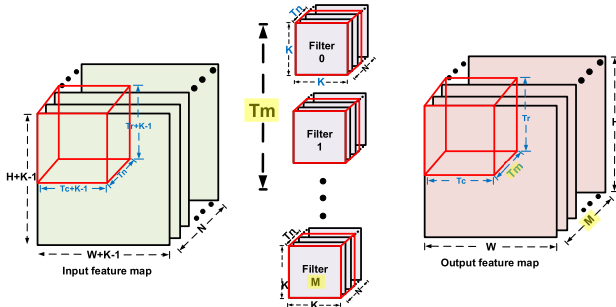**FIGURE 2. Interface of the proposed DLA with auxiliary units.**

FIGURE 3. Core of convolution calculations.

three parallel computing steps as follows, 1.) Input feature map (IM), 2.) Input Channel Parallel (ICP), and 3.) Output Channels (OCH). The above computing steps are shown in Fig. 3, where H is the frame length, W is the frame width, and K is the size of the Filters.

Notably, the size of IM can be derived based on Fig. 3, which are H+K-1 and W+K-1, respectively. The number of IM parallel input channels is N. The number of output channels is M after the output feature map (OM) is generated by M K×K Filters processing the IM. Apparently, the size of the output feature map is M×H×W.

However, the realization of the above convolution is not straightforward at all owing to the limitations posted by the hardware availability. For instance, it is impossible to have an unlimited size of buffer to store the computation outcome of all the IMs and Kernels in the left hand side of Fig. 3. Thus, we propose to divide the IMs into plural sections, as indicated by those red boxed in Fig. 3, which will then be processed, tiled, and padded later by Reshape module, which will be described later in the text. T_m stands for the memory sizes which are needed in an internal batch computation. Apparently, numerous PEs (processing element) will be needed to carry out the computation of all the tiles in one single cycle, as shown by Eqn. (1). If the number of PEs is limited, on the other hand, it will take a long time, i.e., many cycles, to execute the computation resulting the decrease of throughput. To estimate the number of PEs, we can predict by the following facts.
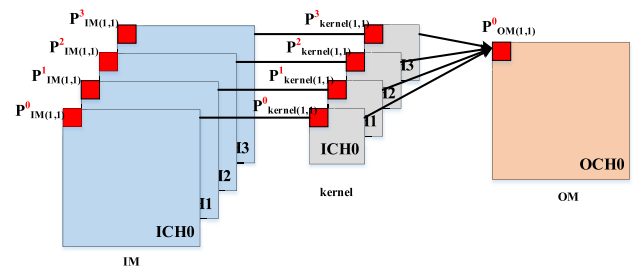
1). T_m is the number of OCH in one cycle
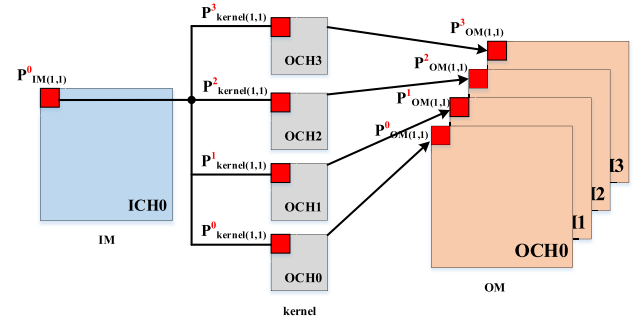

FIGURE 4. Illustrative diagram of ICP.

FIGURE 5. Illustrative diagram of OCP.

2). T_n is the number of ICH in one cycle

3). T_r, and T_c are the length and width of output window, respectively

Thus, the number of PEs to carry out the batch computation in one cycle is summarized as follows.

$$PE_{all} = T_m \times T_n \times T_r \times T_c \times K^2 \qquad (1)$$

A total of three possible parallel hardware arrangements to carry out the above convolution computation are highlighted as follows.

● Input Channel Parallel (ICP): As shown in Fig. 4, the superscript of P stands for the number of channel, while the subscript is the coordinate of the selected pixel. For instance, ICP=4 in Fig. 4 indicates that there are 4 channels, P_{IM}^0 to P_{IM}^3, where each channel is for one pixel. They are delivered to 4-channel kernel to carry out MAC operations in parallel, and the outcome is written into the corresponding one-channel one-pixel output feature map. The required least hardware to carry out this ICP operation needs 4 input/kernel buffers.

● Output Channel Parallel (OCP): Similarly, OCP=4 in Fig. 5 denotes there are 4 channels, P_{OM}^0 to P_{OM}^3, needed to generate output feature map (OM). Certainly, the required least hardware to carry out the MAC operations is 4 output/kernel buffers.

● Window Parallel (WP) : The major difference of WP vs. ICP and OCP is that all the MAC operations are carried out in one channel and multiple pixels, unlike the multiple channel and one pixel in ICP and OCP. WP operations can be divided into two types, namely Output Window Parallel (OWP) and Kernel Window Parallel (KWP), depending on what the data source is. As shown by Fig. 6(a), OWP selects 4 pixels in
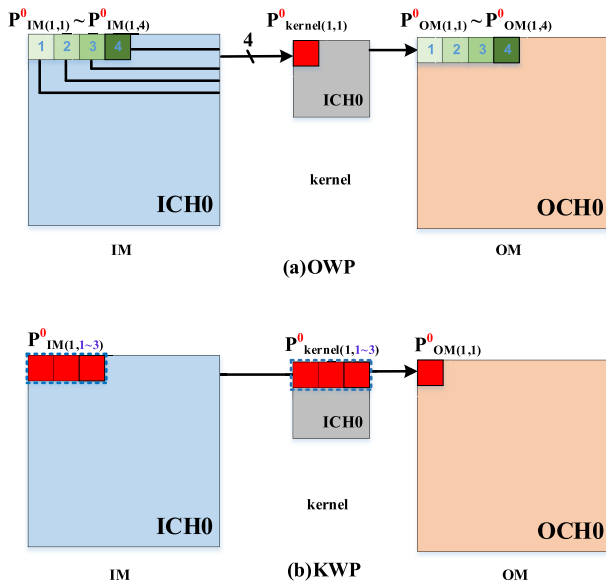
FIGURE 6. Illustrative diagram of WP (a) OWP; (b) KWP.

IM, $P^0_{OM(1,1)}$ to $P^3_{OM(1,4)}$, to multiply with $P^0_{OM(1,1)}$ of the kernel. The product is then written into the single channel 4 pixels in the OM. As for the KWP operation as shown in Fig. 6, 3 pixels in one channel of IM, $P^0_{OM(1,1)}$ to $P^3_{OM(1,3)}$ are multiplied with the 3 pixels in the kernel, $P^0_{OM(1,1)}$ to $P^3_{OM(1,3)}$. Then, the MAC result is written in the one channel and one pixel in OM. Since all the WP operations are executed in one channel, the hardware demand is significantly reduced at the expense of a little bit longer delay.

B. CONTROLLER

The DLA controller relies on the Inter-Controller to generate timing signals to drive the DMA and all the other hardware modules. In other words, the controller is the main driver of DLA to generate control signals for the operation of the modules to be activated or not, including the finite-state machine (FSM) state transfer, circuit switching, and power consumption. The Inter-Controller has five states: 1. Idle (S0) state, 2. Load (S1) state, 3. Calculate & Load (S2) state, 4. Calculate (S3) state, and 5. Store (S4) state, as shown in Fig. 7. Each state is assigned to carry out different modes by generating corresponding signals.

C. PROCESSING ELEMENT (PE)

Most of the prior processing element (PE) was based on a multi-resolution architecture, e.g., [25], which was for different weight resolutions used in MAC operations. Though it attained an advantage of diversity, the trade-off is long delay caused by the cascaded stages. A very fatal issue, on top of the delay, is that the overflow or underflow can not be detected or fixed, if they appear during the MAC operations. Namely, the error will be accumulated and passed downstream if it happens.
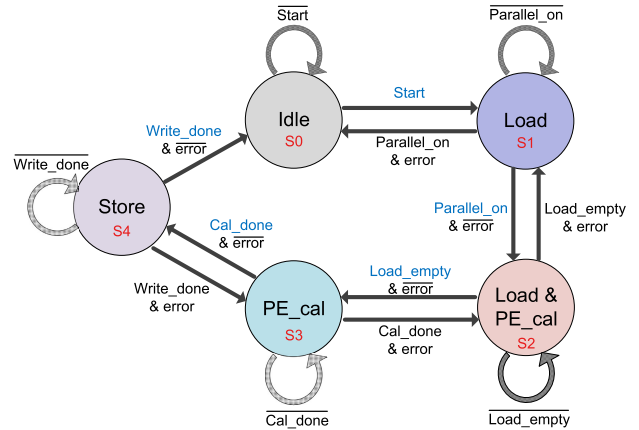

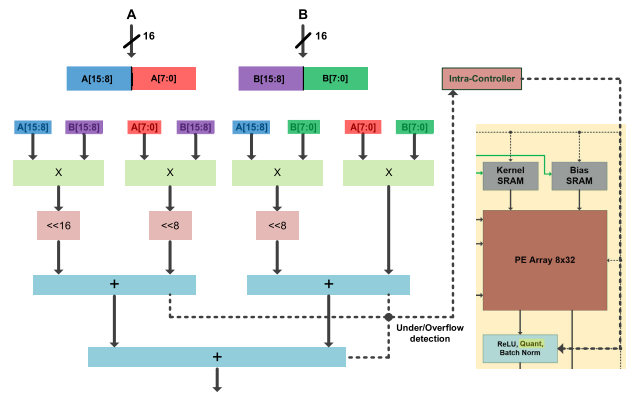**FIGURE 7.** State transition diagram of the DLA controller.

FIGURE 8. Proposed processing element (PE) with overflow and underflow detector.

To resolve the long delay and inevitable overflow & underflow problems, a new processing element was presented as shown in Fig. 8, where the proposed PE element will only use 16-b resolution integer without loss of robustness for underwater object recognition. It is composed of four 8 × 8 multipliers, one 16-b logical shifter, two 8-b logical shifters, three 16-b adders, and an underflow/overflow detector. The number of shifting steps are drastically reduced by such an architecture, because the element no longer needs to generate trailing bits for the inputs of the PE. Moreover, less number of stages is needed compared to the prior designs, thus reducing the delay. An underflow and an overflow detector are also introduced to co-work with the intra-controller and send notification signals to the quantization module of the DLA. More specifically, Overflow is detected when the output result is over 16'h7FFF and underflow when it is 16'h8000.

D. PE ARRAY

Fig. 9 shows the PE array architecture composed of 8 rows of output window parallel (OWP) and 32 columns of output channel parallel (OCP). The outputs are generated and passed to the left and a set of kernel values are shared by the same column. To reduce the area and power consumption of the array, the excitation functions, quantization, and batch
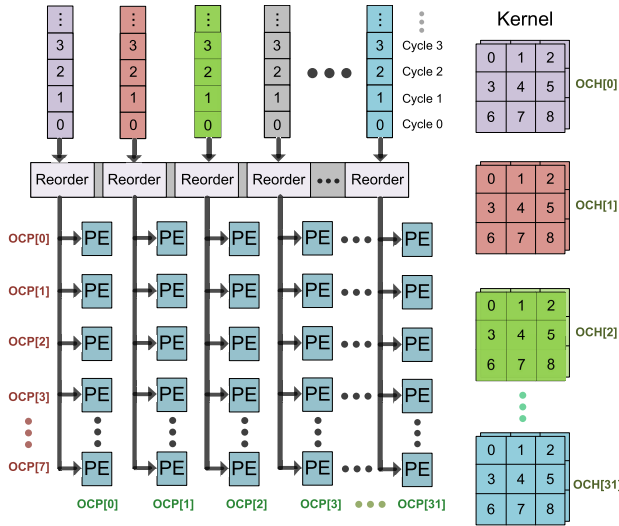
FIGURE 9. PE array architecture.

TABLE 1. Comparison of bit length vs. hardware/timing cost.

In x Kernel	2x2	4x4	8x8	16x16
#PE	64	16	4	1
MUL area (16x16, μm^2)	42340	10479	6268	3615
delay (ms)	10	7.08	7.05	5.7

normalization of the pixels are performed outside the array prior to the output SRAM.

One important design consideration is how to determine the trade-off between data bit length, accuracy, delay, and possible timing violation. The bottom is when the bit length is large intending to attain high accuracy, the penalty is the increase of sign extended bits and the timing violation caused by the generation of massive clock tree routes. Table 1 summarizes all the multiplier (MUL) designs for various selections of bit lengths of input vectors and kernels. Apparently, the 4 × 4 and 16 PEs are the better option when considering the chip area, complexity, and throughout at the same time.

E. MEMORY ARRANGEMENT FOR INPUT, KERNEL, AND OUTPUT

The input and kernel SRAMs of the proposed DLA was realized with 8 banks 2-port 8-b 1R1W SRAMs, respectively. Double buffers are employed at the outputs thereof to reduce the access time and increase the slew rate. The double buffer design also attains another advantage, which is that the resource can be allocated to other operations when it is not in use. For instance, if only half of the bank is used, the other half is allocated to load the required data. By contrast, the output SRAM of the DLA uses 4 banks of 128-b dual-port SRAMs (2R or 2W or 1R1W). The SRAMs for Input, Kernel, and Output are shown in Fig. 10, respectively.

F. RESHAPE AND LINE BUFFER MODULES

Apparently, it is impossible to have unlimited hardware resources to accommodate all the pictures or video frames
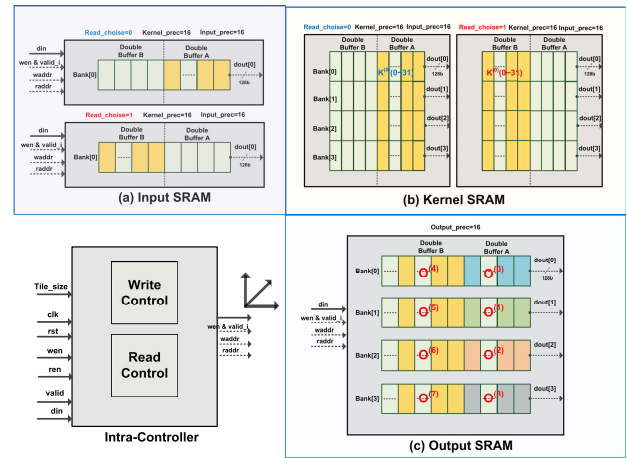

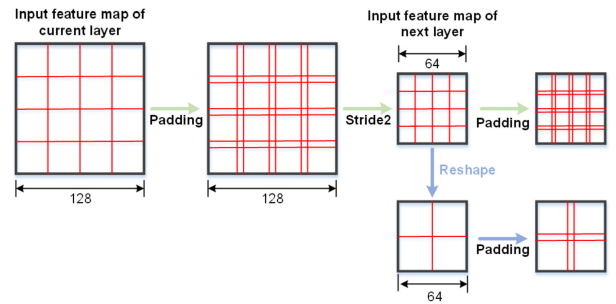**FIGURE 10.** SRAM structures of (a) Input, (b) Kernel, and (c) Output.

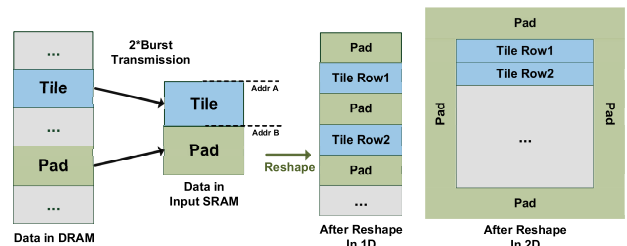**FIGURE 11.** Examples of padding given different stride steps and tiles.

FIGURE 12. Operation flow of re-organization of tile and pad.
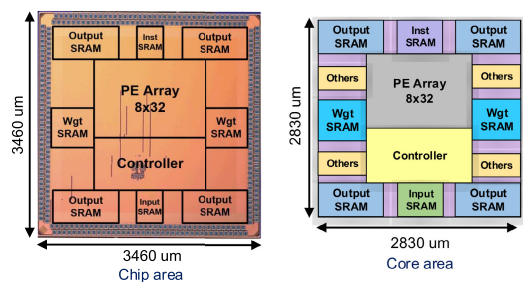

FIGURE 13. Die photo and layout of the DLA.

at the same time for any processing, particularly the on-chip memory buffers. Thus, the tile-based computation, as shown in Fig. 11, is needed, where the entire picture frame is divided into plural tiles. As the example highlights in Fig. 11, a 128 × 128 frame is divided into 16 16 × 16 tiles after stride
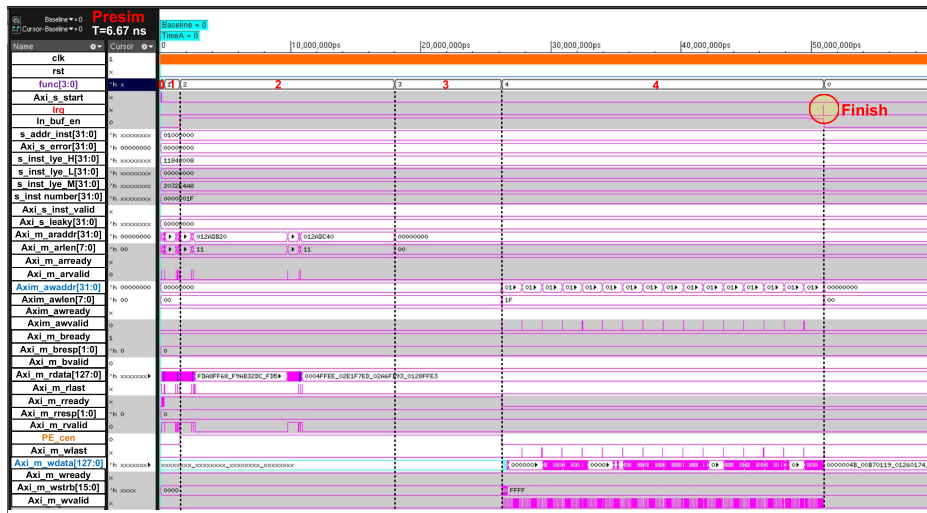
FIGURE 14. Pre-layout simulations of the DLA (clock = 150 MHz).

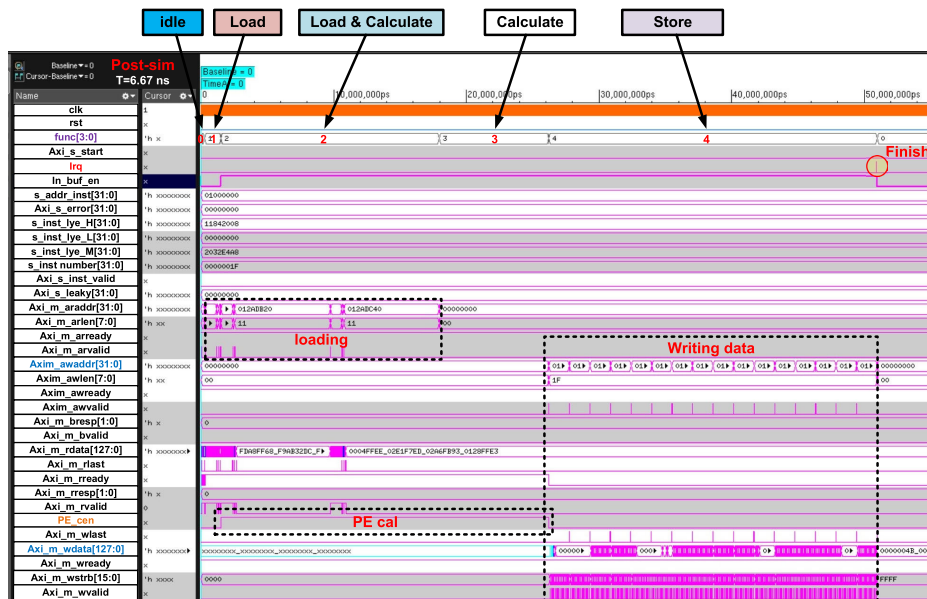**FIGURE 15.** Post-layout simulations of the DLA (clock = 150 MHz, worst corner).

2 operations. Notably, a title of 4 32 × 32 tiles will be re-assembled by a Reshape module, which will be addressed later in the text.

A Reshape module is used for the design to support tile-based calculations as explained earlier. The Reshape module re-organizes the tile-based data to support burst transmission such that the transmission of multi-tile data from one module to another is feasible, as shown in Fig. 12. Notably, a padding step is needed that re-organizes the data into 1D or 2D representation prior to the transmission.

Lastly, the line buffer is composed of 16-b registers with 128-b SRAM (1R1W), which is used to push 8 groups of 16-b data during the convolution operation. The line buffers are also used to hold the weights and data values, which are repeatedly used during convolution operations.

III. IMPLEMENTATION, CHIP MEASUREMENT, AND EXPERIMENT IN WATER

The proposed digital logic accelerator is implemented using TSMC 40-nm CMOS technology (TSMC 45 nm CMOS LOGIC General Purpose Superb (40G) ELK Cu1P10M 0.9/2.5V). Fig. 13 shows the die photo and the layout of the DLA chip, where the on-silicon size is 3460 × 3460 μm^2 including 320 I/O and power pads. Notably, two scan chains and BIST (using March algorithm) are included to enhance the DLA's reliability and testability, where the test coverage was up to 98.35%.

A. DESIGN VERIFICATION BY PRE-LAYOUT VS. POST-LAYOUT SIMULATIONS

Functional verification is required before any physical implementation. The signals and functions of the proposed DLA are summarized as follows.
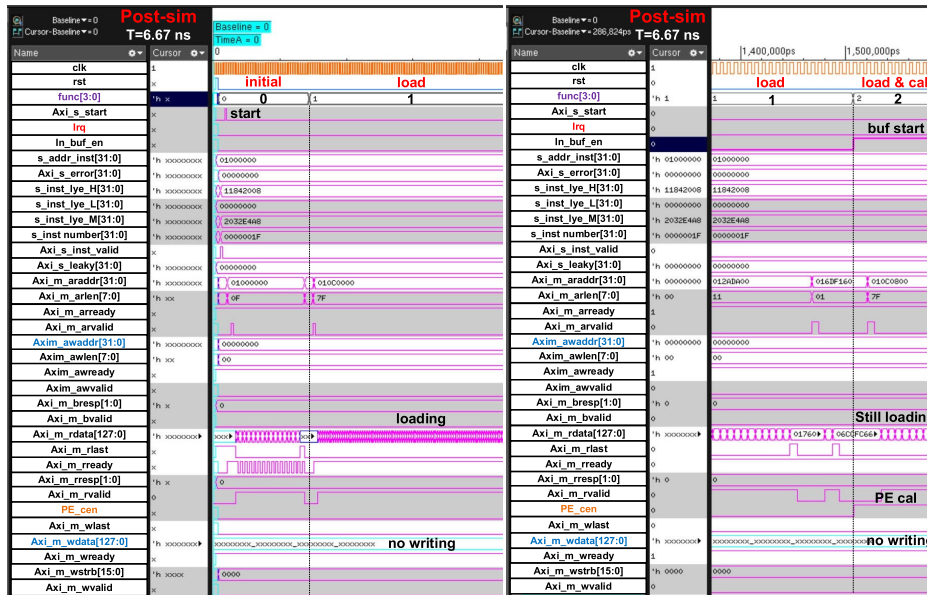
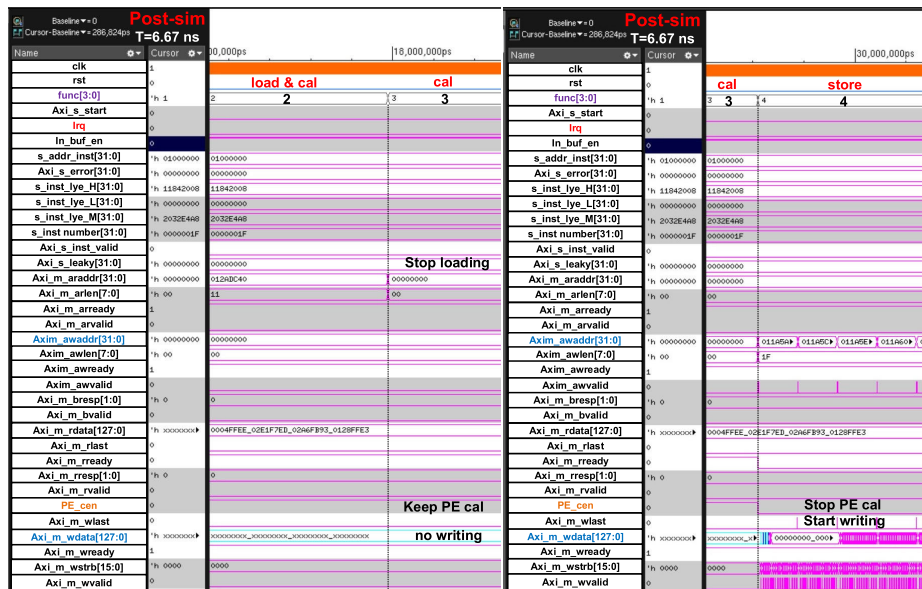**FIGURE 16.** Post-layout simulations of the DLA (Func[0], [1], [2]).

FIGURE 17. Post-layout simulations of the DLA (Func[2], [3], [4]).

- Func[0], [1], [2], [3], [4] : different phases of the controller
- PE_cen : activation signal of PE array
- irq : termination flag of the current computation

Func[0]: idle stage in which is the initialization of the system

Func[1]: load stage in which the data in DRAM are moved to on-chip buffers

Func[2]: load and calculate stage in which certain tiles are delivered to PE array, while other tiles are loaded at the same time

Func[3]: calculate stage in which no data are found in DRAM such that no load is needed and only the calculate is carried out

Func[4]: store stage in which the processed outcome is output

Fig. 14 and 15 are the pre-layout simulation and the post-layout simulation at the worst corner (namely SS), respectively. They have been fully checked to be matched when the same test-bench was used to examine the functional correctness.

To further highlight the simulation details, Fig. 16 and 17 are the magnified post-layout timing waveforms. In the left side of Fig. 16, after Reset is asserted, the DLA system is activated and Axi_s_start is triggered to command the DLA to be initialized and stayed in the standby mode. As soon as Func[0] is changed to Func[1], the data in DRAM are copied to the on-chip buffer. PE_cen and wdata are not asserted now, since there is no calculation nor output.
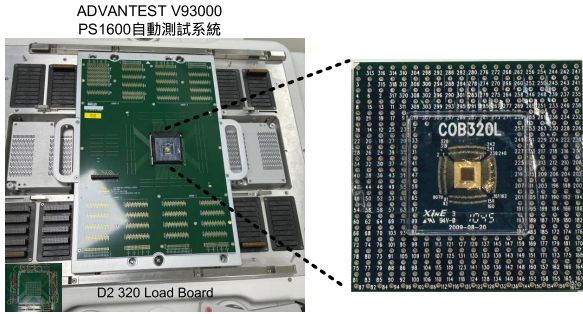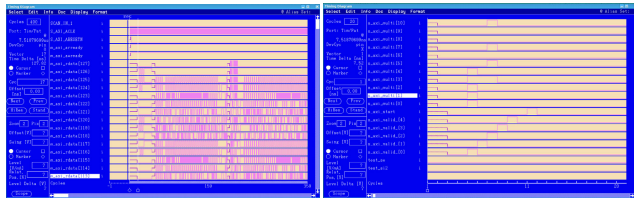
FIGURE 18. DLA chip measurement setup.

FIGURE 19. Input vectors of measurements.

Referring to the right side of Fig. 16, PE_cen is pulled high when the state is changed to Func[2] such that the PE array starts the computation. Notably, since the proposed DLA is designed with dual buffers, the next batch of tiles are read when the computation of PE array is proceeding.

The details of Func[2], [3], [4] are given in Fig. 17. The left side of the said figure shows the scenarios when Func[2] is changed to Func[3], where araddr[31:0] becomes 0 and arleng[7:0] (the length for data transfer) is also 0. At this moment, there is no new data to be fetched such that the only operation is the PE array's computation. wdata stays unknown simultaneously.

By contrast, the right side of Fig. 17 shows that transition from Func[3] to Func[4]. Besides stopping PE array operation by pulling down PE_cen, awvalid (signal to output channels), awlen (length of output data), wvalid (valid flag of data), awaddr (address to write data), and wdata (data to be output) are all activated. As soon all data are written into Output SRAM, irq is asserted to notify the entire process is done.

B. CHIP MEASUREMENT

The performance measurement of the proposed DLA chip was conducted in SOC Lab. of TSRI in Hsinchu, Taiwan, using ADVANTEST 93000, as shown in Fig. 18. Fig. 19 is the screenshot of the input vector waveform. Fig. 20 is the measured waveform to prove the state transition from Func[0] to Func[2], while Fig. 21 is those for transition from Func[2] to Func[4]. These two measured figures match the prediction given by the post-layout simulations, including initialization, load, compute and store operations.

Lastly, Fig. 22 is the end of the entire processing cycle of one picture frame. Notably, the pulse highlight in the right side of the figure indicates the end signal. Fig. 23 is the
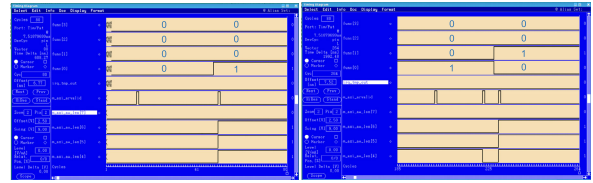

FIGURE 20. Measured waveforms for transition Func[0] to Func[2].
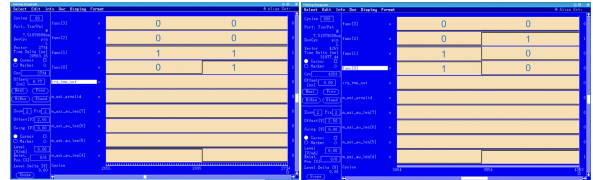
FIGURE 21. Measured waveforms for transition Func[2] to Func[4].
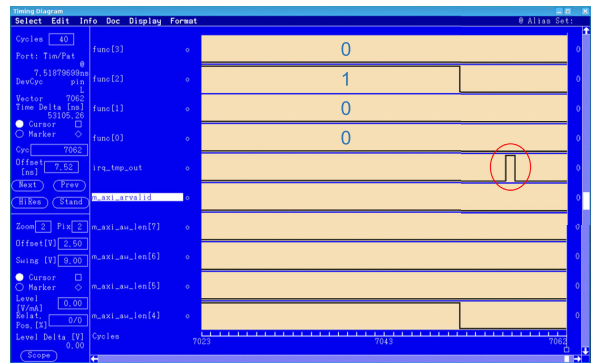
FIGURE 22. Measured waveform for transition Func[4] to the end of the current processing cycle.
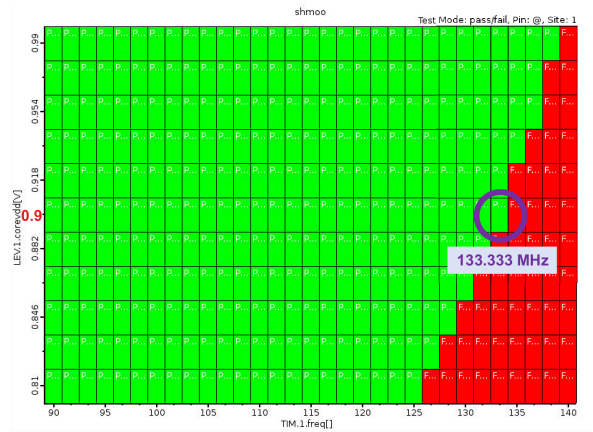
FIGURE 23. Shmoo plot of the proposed DLA.

Shmoo plot to show that when VDD = 0.9 V, the operation clock = 133.33 MHz.

C. REAL-TIME SYSTEM FUNCTION VERIFICATION

To verify the DLA functionality in real time, the best way is to make a comparison of two experiments: 1) from CPU-based software simulations (using float32 computation, assumed as the golden model), and 2) the DLA+FPGA hardware testing. An algorithm based on YOLOv3-tiny was implemented using the mentioned two approaches, which
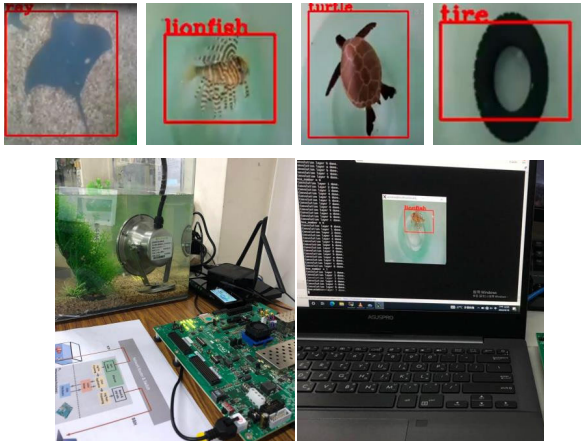
High-performance DLA experiment
for real-time recognition

FIGURE 24. Comparison of CPU-based and DLA-based experiments for underwater object recognition.

FIGURE 25. Recognition outcomes of SW-based FPGA vs. our DLA.

FIGURE 26. Absolute error of the DLA approach vs. the golden model (≤ 1.4%).
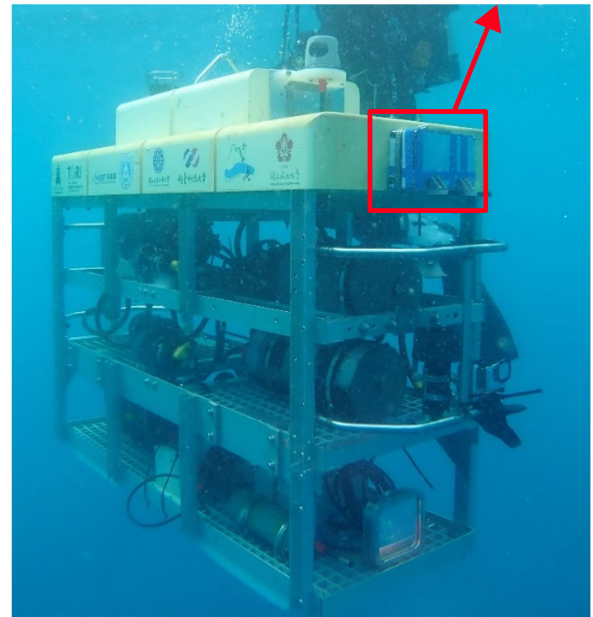
FIGURE 27. AUV equipped with an AI box containing the proposed DLA and auxiliary circuits.

are compared to estimate the absolute error caused by our DLA.

The comparison experiment was shown in Fig. 24, which shows the identical recognition results except the delay and frame rate. Fig. 25 demonstrates an apple-to-apple comparison between the software-based solution and our DLA. The absolute error was found to be less than 1.4% as shown in Fig. 26.

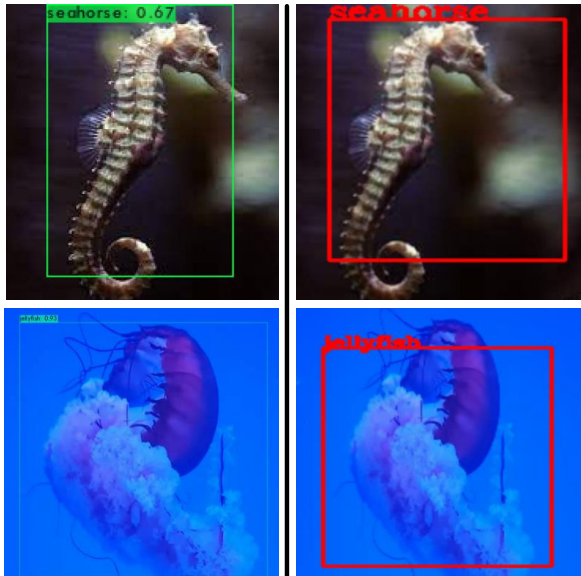### D. OPEN WATER TEST DEMONSTRATION
To physically test the proposed DLA in real underwater environment, we then conducted open water experiments. An AI box containing the proposed DLA, camera, battery-based power supply, FPGA board, and other auxiliary circuits, was installed on the front of an AUV as shown in Fig. 27. Before

the open water experiments, the AI box had been trained offline to recognize more than 20 different underwater objects, including lion fish, clown fish, shark, tire, glass bottle, turtle, diver, etc. The mAP has been trained over 90% before the experiment. All the weights and kernels were written into the FPGA so that the edge inference using the proposed DLA can be carried out independently in water. Fig. 28 shows the AUV was driven 7 meters below the water surface, where it is about 1 mile from the coast line of Little Ryukyu, an island close to Taiwan.

Besides the mentioned object recognition, the proposed DLA installed in the AI box is utilized to carry out the mission of object following in water. In our experiment, the diver is selected to be the object to be followed by AUV, since other objects in the data bank are either uncontrollable, such as shark and fish, or stationary still, such as tires and glass bottles. Fig. 29 and 30 demonstrate the diver following mission screenshots. Particularly, Fig. 30 shows the scenario where not only the AUV follows the diver, it also detects

TABLE 2. Table of Comparison with previous State-of-the-Art.

|	[13]	[20]	[21]	[22]	[23]	[24]	[25]	[26]	Ours
Year	2017	2018	2020	2020	2020	2021	2022	2023	2024
Publication	JSSC	TCAS-I	JETCAS	JSSC	GCCE	HCS	TCAS-I	TCAS-I	
Process (nm)	65	65	40	65	90	180	180	Nexys A7-100T (FPGA)	40
Verification	Meas.	Simu.	Simu.	Meas.	Simu.	Simu.	Meas.	Meas.	Meas.
Supply (V)	1.0	1.2	0.9	0.6	1.2	1.8	1.8	3.3	0.9
Area (mm^2)	16	10.6	200	2.56	14	3	53.63	50.2k LUT 240 DSP	11.97
Max. Freq. (MHz)	200	200	200	0.25	100	107	100	100	133.33
On-chip buffer (kb)	181.5	139.6	118	16	322	16	150	58.1k FFs	150
No. of MACs	168	64	128	512	72	182	256	82.53% (utilization)	256
Activation bit-width	16	16	16	8	16	32	16	8	16
Kernel bit-width	16	16	16	8	16	32	16	8	16
Performance (GOPS)	42	23.4	51.2	0.471	14.4	35.05	40.96	95.08	**54.61**
Power (mW)	278	93.4	153.94	0.0106	164.7	649	196.8	2203	**96.35**
Area eff. (GOPS/mm^2)	2.625	2.21	0.26	0.184	1.029	11.684	0.7638	N/A	**4.562**
Power eff. (TOPS/W)	0.1511	0.253	0.3326	44.434	0.087	0.054	0.2081	0.04316	**0.5668**
[1]CO_2 equivalent (kg.)	1.05	0.35	0.58	0.01	0.624	2.5	0.75	8.32	**0.365**
[2]FOM1	30.21	60.1	59.86	6.40	10.491	10.402	37.46	47.00	**68.01**
[3]FOM2	1.89	5.67	0.30	2.34	0.75	3.47	0.70	N/A	**5.68**

[1]Based on U.S. EPA greenhouse gas equivalency [27].
Computed based on continuous operation for 1 year.
[2]$FOM1 = \frac{Frequency(MHz) \times GOPS}{Normalized\ Power(mW)}$
[3]$FOM2 = \frac{FOM1}{Area(mm^2)}$
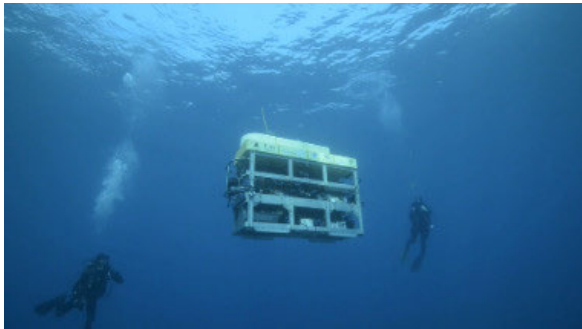
FIGURE 28. AUV with the AI box was tested in the open sea of Little Ryukyu, an island close to Taiwan.
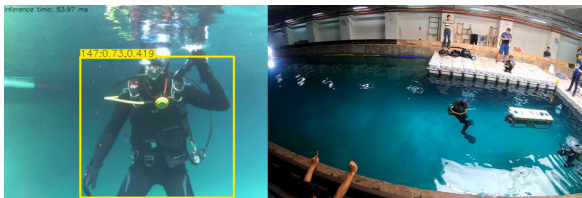
FIGURE 29. AUX with the AI box to execute diver following mission.

FIGURE 30. AUX with the AI box to execute diver following and object avoidance.

the unknown big rock in the water and cruise away to avoid possible collisions. These experiments surely prove that the proposed design not only measurable on silicon, but also usable in field applications.

E. PERFORMANCE COMPARISON AND ANALYSIS
Table 2 shows the comparison with many recent CNN/DNN hardware accelerator works reported in top journals recently. Notably, the supply voltage of our DLA is 0.9 V operating at

133.33 MHz frequency. The on-silicon measurement results of our DLA show a performance 54.61 GOPS at a power consumption of 96.35 mW. Meanwhile, TOPS/W = 0.5668, and GOPS/mm^2 = 4.562, both are the best by far if normalized with CMOS technology nodes and the operating clock frequency. It also shows that [22] has the highest TOPS/W and this is because its designs uses only 8-bit kernels thus significantly decreases the overall area and hence power of the chip.

Besides the comparison of recent DLAs on single dies, we also made a comparison with a recent work implementing YOLOv3-tiny on Nexys A7-100T FPGA [26]. Not surprisingly, though the FPGA-based solution gives a better performance in terms of GOPS, it pays very high price in

terms of power consumption such that the overall power efficiency is really poor. Two (2) FOMs (Figure-of-Merit) is used to compare the different designs, the first one uses the frequency, performance, and power while the second one added the effect of the chip area. In short, the proposed design shows an FOM1 value of 68.01 and FOM2 value of 5.68 which is the best among all DLA works in Table 2. It also shows the lowest carbon dioxide (CO_2) equivalent energy emission when used continuously for an entire year [27]. Lastly, the proposed DLA is the only one specially developed for underwater AI applications.

IV. CONCLUSIONS AND FUTURE WORKS

A low-power and high-performance DLA using 40-nm CMOS process is presented in this investigation. A new parallel architecture based on processing element with underflow and overflow detection is proposed to increase processing speed and reduce computational error. Not only the normalized area and power efficiencies of our design are better than prior DLAs, the FOM also shows that our design is the best so far even if the clock frequency is taken into account.

Future works for this investigation is to improve the processing elements to perform faster computations. An improved version of the machine learning is also under development to further reduce the computational requirements of the DLA in order to further improve the power efficiency of the design.

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