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Up To 99.6 % duty cycle digital PWM using 180-nm CMOS process

Chua-Chin Wang [a,b,*], Oliver Lexter July Alvarez Jose [c], Venkata Naveen Kolakaluri [a]

[a] Department of Electrical Engineering, National Sun Yat-Sen University, No. 70 Lian-Hai Road, Gushan District, Kaohsiung, 80424, Taiwan
[b] Institute of Undersea Technology, National Sun Yat-Sen University, No. 70 Lian-Hai Road, Gushan District, Kaohsiung, 80424, Taiwan
[c] Department of Electronics Engineering, Batangas State University - The National Engineering University, Alangilan, Batangas City, 4200, Philippines

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ABSTRACT

Prior digital pulse width modulation (DPWM) techniques are implemented with numerous D flip-flops (DFFs), which exponentially increase with the resolution and can easily affected by clock skew. This study presents a high-resolution (N = 8) DPWM design that uses a small number of DFFs (The prior architectures used the 2^N number of DFFs in their design, while in this research, the "N" resolution is not directly proportional to 2^N number of DFFs.) It uses a single clock input for synchronization to achieve high input clock frequency (f_{clkin}). The DPWM has a Non-overlapping circuit to prevent shoot-through between DPWM complementary outputs during operations. The DPWM architecture has been fabricated using UMC 180-nm CMOS technology. The DPWM's functionality and performance were validated through the measured comparisons at f_{clkin} = 100, 250, 350, and 400 MHz. It achieves a maximum duty ratio of 99.6 % and output voltage of 1.79 V with 8.913 mW power dissipation at f_{clkin} = 400 MHz. In addition, it has the highest f_{clkin} and resolution to date, which makes it superior to prior works.

1. Introduction

Power supply plays a vital role in many terminal applications such as the Internet of Things (IoT), since it involves millions of electronic devices [1]. Many IoT applications, such as those in industrial fields, smart cities, etc., require sensors to operate for an extended period without the need to change the battery [2]. A power management circuit may be utilized to meet any voltage requirements while also increasing battery efficiency [3].

Most conventional power management circuits rely primarily on analog circuits, making them susceptible to PVT (process, voltage, and temperature) variations [4]. Digital controllers mostly employ digital pulse width modulation (DPWM), which has gained popularity as an alternative to analog PWM circuitry. DPWM has no headroom constraints, making it suitable for advanced CMOS technology. However, DPWM has a bandwidth and resolution limitation, which is critical for high-accuracy applications [5]. Most DPWM techniques also use multiple clock inputs to achieve higher resolution, which is difficult to synchronize in real-time.

A DC-DC buck converter is a typical example to take advantage of the DPWM for low-power applications [6,7]. A delay line through a long chain of DFF array is utilized to generate the modulated digital pulse signal. The DPWM resolution (N) can be increased by increasing the DFF array exponentially (i.e., number of DFF = 2^N). The DPWM's higher resolution requires more clock buffers, making it more susceptible to clock skew. It also uses multiple clock inputs, which limits the bandwidth due to synchronization issues.

A prior report that also used DFFs to increase the resolution implements a matrix shift array to minimize the effect of the clock skew issue [8]. The DFFs in the matrix shift array can be reorganized to decrease the number of DFFs in a single column by increasing the number of rows and single clock input for stability. However, increasing the resolution that controls the matrix shift array to attain a lower effect of clock skew will result in a larger area.

Another DPWM employs a digital counter and VCO (voltage control oscillator) in a buck converter for duty cycle control to achieve higher efficiency [9]. Since this study does not use a long chain of DFF, the resolution can be increased without the lower effect of clock skew. The accuracy of the DPWM depends heavily on the linearity of the VCOs, making it vulnerable to PVT (process, voltage, temperature) variations [10]. It also used multiple clock inputs, which limits the DPWM bandwidth. An all-digital PWM for DC-DC converters achieved 6.25 ps resolution and 16-bit PWM resolution using a multi-phase clock signal from ADPLL (All-Digital Phase Locked Loop) [11]. The use of ADPLL as a synchronized multiple clock source accumulates a significant amount of jitter, which results in a larger PWM signal pulse width [12]. There is also a mismatch in the DPWM average step

* Corresponding author.
E-mail address: ccwang@ee.nsysu.edu.tw (C.-C. Wang).

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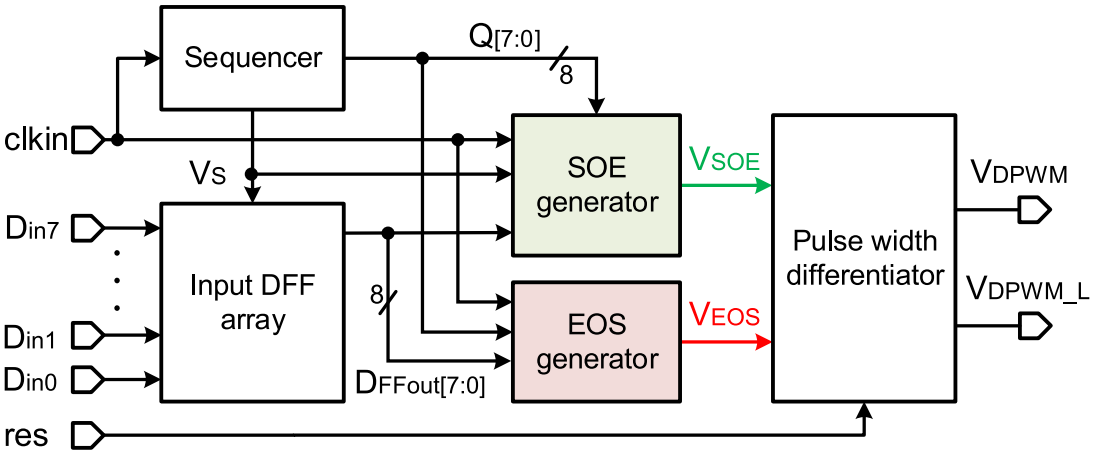

Fig. 1. Proposed DPWM block diagram.

size and standard deviation during measurement caused by the 8-phase clock signals.

A high-resolution DPWM design is presented in this work, which is preferred during high-accuracy applications. The DPWM design requires less number of DFFs at higher resolution, minimizing the effect of clock skew. It uses a single clock input; hence, no extra circuit for timing synchronization was required [13]. A Non-overlapping circuit is utilized to avoid shoot-through between DPWM's complementary outputs. The DPWM functionality and performance are validated through physical chip measurement.

2. Proposed high-resolution DPWM

Fig. 1 shows the system block diagram of the proposed high-resolution DPWM design. The DFF input array is used to synchronize the N-bit inputs. Its output is coupled to the SOE (start-of-sequence) and EOS (end-of-sequence) generators, which provide the V_{DPWM}'s start and end reference points, respectively. The Sequencer generates the input for SOE and EOS generators, which define the PWM period (T_{DPWM}) of the V_{DPWM} by counting the clkin cycles based on N resolution. Finally, the V_{SOE} and V_{EOS} signals will drive the Pulse width differentiator, which will output the modulated % duty cycle.

The working principle of the proposed DPWM technique is illustrated in Fig. 2. It is summarized as follows:

t_0-t_1: A half-clock cycle between clkin and V_S is generated, providing enough time for the logic circuit outputs to reach the stable state.

t_1-t_2: Another half-clock cycle is generated between V_S and V_{SOE}, providing enough read and write operation margins of the DFF input.

t_2-t_3: V_{SOE} goes high at the positive edge of clkin. V_{SOE} is a fixed position for all the possible combinations of input $D_{in[7:0]}$ (D flip-flop input in the DFF array block) and provides a reference to V_{DPWM} to become logic "1". For example, when $D_{in[7:0]}$ = 00000111, the V_{DPWM} is high for seven (7) clkin (equivalent decimal) and will go low at the positive edge of V_{EOS7}. Signal V_{EOS} is delayed by the number of clock cycles set by the $D_{in[7:0]}$ input, which results in an increase or decrease in the output duty cycle.

t_3-t_4: V_{DPWM} is low until the clkin completes a cycle equal to 2^N. In this case, the modulation process is completed.

2.1. Sequencer and input DFF array

Fig. 3 shows the Sequencer schematic. Its primary function is to translate input clock (clkin) pulses into N-bit binary sequences, represented by $Q_{[7:0]}$ signals, which will be the reference for the input pulse position. The DFF strings in the Sequencer are double-edge-triggered (positive edges for the present state and negative edges for the next state) to provide sufficient margin for the "read"/"write" operations, improving the DPWM reliability. The Sequencer's output V_S is generated every 2^N clock cycle and will output a logic "1" when the cycle is completed.

The Input DFF array in Fig. 1 defines the "N" resolution (N = no. of DFFs) of the proposed DPWM technique. In addition, it will synchronize the $D_{in[7:0]}$ input for the stability.

2.2. SOE generator

The SOE generator provides a reference for the modulated % duty cycle to begin to rise. Illustrated in Fig. 4 is the schematic of the SOE generator. When $D_{in[7:0]} \neq$ 00000000, a fixed position SOE signal is generated. There is no generated SOE during $D_{in[7:0]}$ = 00000000, since there must be no PWM signal under this state. To accurately determine if $D_{in[7:0]}$ is a zero value, the SOE signal is updated at the positive edge of clkin and is delayed by half a clock signal with respect to V_S.

2.3. EOS generator

The EOS generator shown in Fig. 5 outputs an EOS signal to determine the width of the proposed DPWM modulated duty cycle. EOS generator implements a small number of DFFs compared to prior DPWM techniques [6–8]. The number of DFFs (DFF_{No}) in the DPWM design with respect to the resolution is defined by Eq. (1).

$$DFF_{No} = 3 \cdot N + 4 \tag{1}$$

Referring again to Fig. 2, notice that the SOE signal is delayed by one clkin cycle from t_0. Therefore, EOS is likewise delayed by one clkin cycle so that T_{DPWM} (modulated signal period) is the same as Eq. (2).

$$T_{DPWM} = T_{clkin} \times 2^N \tag{2}$$

where T_{clkin} is the period of the input clock signal. The "on" time (T_{DPWM_on}) and maximum output duty cycle (max_{duty_cycle}) for the proposed DPWM can be calculated using Eqs. (3) and (4), respectively.

$$T_{DPWM\_on} = D_{[7:0]\_dec} \times T_{clkin} \tag{3}$$

$$max_{duty\_cycle} = \left(1 - \frac{1}{T_{clkin}}\right) \times 100\% \tag{4}$$

where $D_{[7:0]\_dec}$ is the decimal equivalent of the binary input $D_{[7:0]}$. EOS is the reference point for the modulated duty cycle to turn off.

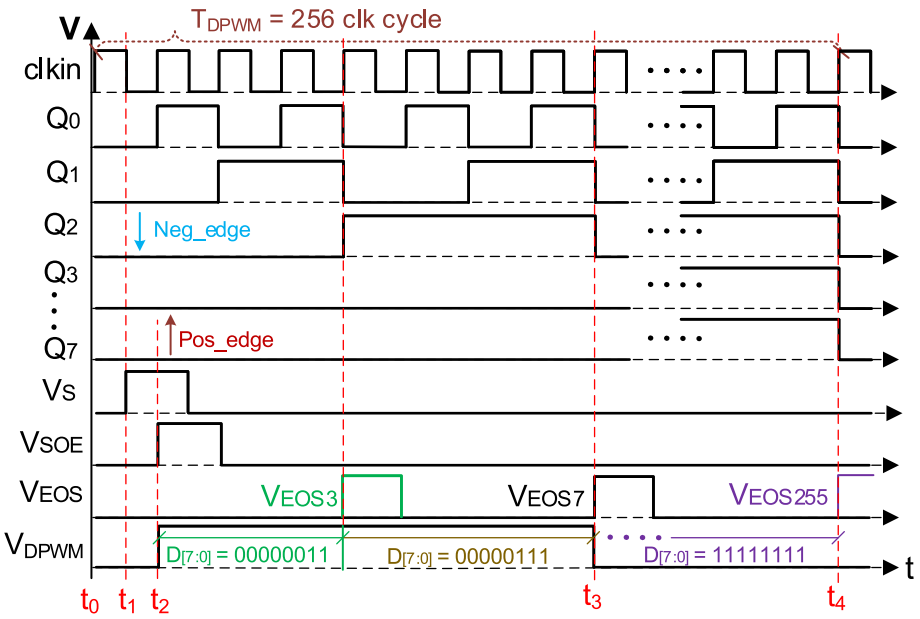

Fig. 2. Proposed DPWM timing diagram.

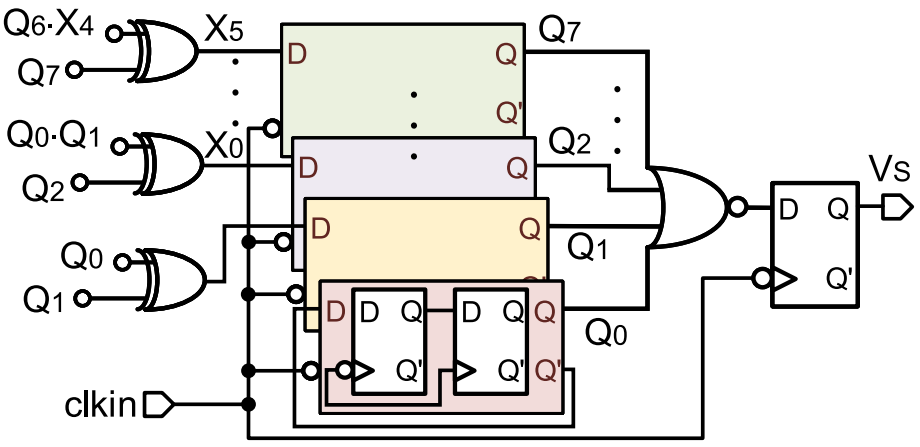

Fig. 3. Sequencer schematic.

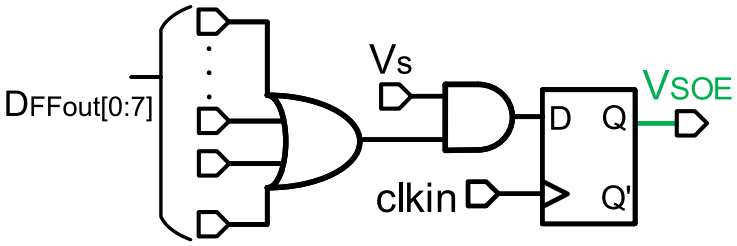

Fig. 4. SOE generator schematic.

2.4. Pulse width differentiator

The Pulse width differentiator generates the proposed DPWM complementary output signals, V_{DPWM} and V_{DPWM_L}. Fig. 6 shows the Pulse width differentiator schematic driven by SOE and EOS signals. The reset (res) input sets the SR latch to its initial state (Q = 0) and deactivated afterward. The Non-overlapping circuit reported in [14] is implemented to provide on-off timing delay between complementary DPWM outputs, eliminating shoot-through during transitions. The optimal output frequency (f_{out_ideal}) can be calculated using Eq. (5).

$$f_{out\_ideal} = \frac{f_{clkin}}{2^N} \tag{5}$$

3. Measurement and performance analysis

The die photo of the proposed DPWM technique fabricated using a UMC 180-nm CMOS technology process is illustrated in Fig. 7. The chip has a core area of 658.93 × 493.79 μm^2 with an overall chip area of 1469.08 × 1469.08 μm^2.

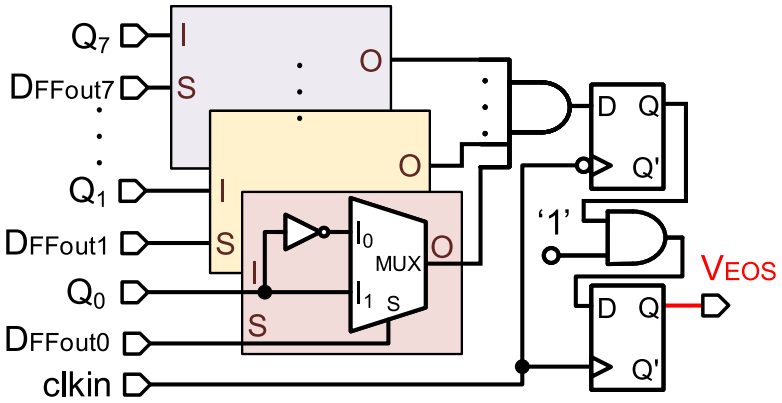

Fig. 5. EOS generator schematic.

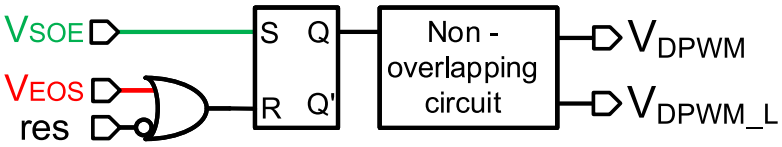

Fig. 6. Pulse width differentiator schematic.

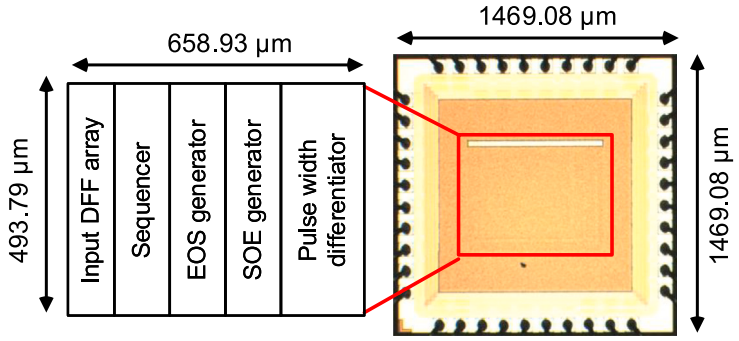

Fig. 7. Proposed DPWM design layout and die photo.

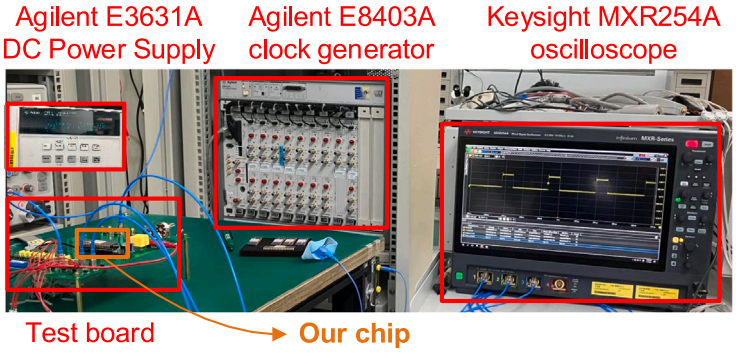

Fig. 8. Proposed DPWM measurement setup.

Fig. 8 shows the measurement setup for the proposed DPWM technique. Agilent E3631 A supplies a 1.8 V VDD, while Agilent E8403 A provides the clkin. To monitor the DPWM output waveform, Keysight MXR254 A is used.

Illustrated in Fig. 9(a), (b), (c), and (d) are the T_{DPWM}, f_{out_meas} (output frequency), and Duty ratio for f_{clkin} (clkin frequency) equal to 100, 250, 350, and 400 MHz, respectively, at $D_{in[7:0]}$ = 11 111 111, probe capacitance $C_{(Load)}$ = 30 pF, and inductive load = 0.8 µH. A 0.01% variation in the Duty ratio is observed when f_{clkin} = 250 and 400 MHz. The worst output frequency and T_{DPWM} occur at f_{clkin} = 250 MHz with 0.003 ns and 5.68 kHz highest variation, respectively. The minimal variations of the theoretical vs. measured T_{DPWM}, f_{out_meas}, and Duty ratio verify the functionality and accuracy of the proposed DPWM design.

Fig. 10(a), (b), (c), and (d) show the modulated duty cycle for $D_{in[7:0]}$ = 00000001, 00000111, 00011111, and 01111111, respectively, at clkin = 400 MHz. The target Duty cycle error of 0.2% can be observed at $D_{in[7:0]}$ = 00000111. A 0.6 MHz highest frequency variation occurs at the lowest clock input frequency, $D_{in[7:0]}$ = 00000001.

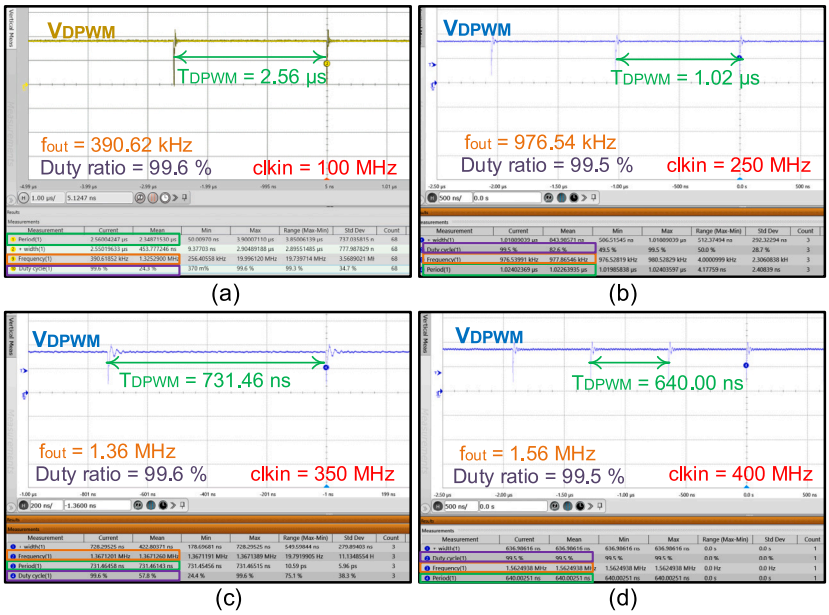

Fig. 9. Waveforms of V_{DPWM} demonstrating its T_{DPWM}, f_{out_meas}, and Duty ratio at f_{clkin} = (a) 100, (b) 250, (c) 350, and (d) 400 MHz.

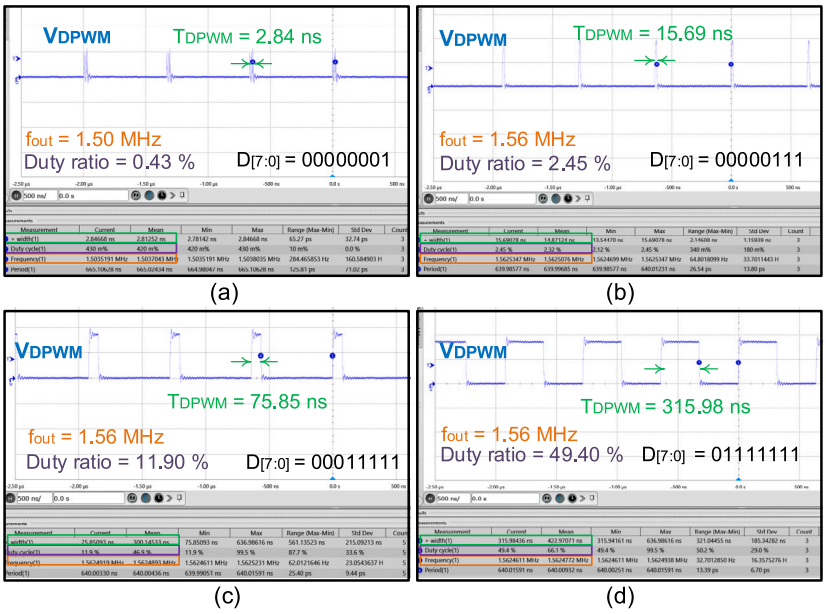

Fig. 10. Waveforms of V_{DPWM} demonstrating its T_{DPWM}, f_{out_meas}, and Duty ratio at f_{clkin} 400 MHz and $D_{in[7:0]}$ = (a) 00000001, (b) 00000111, (c) 00011111, and (d) (a) 01111111.

Tabulated in Table 1 is the Duty ratio comparison between theoretical values and those measured ones at clkin frequency = 100, 250, 350, and 400 MHz using Johnson counter input. The % error is high when input $D_{in[7:0]}$ is low. As the $D_{in[7:0]}$ increases, the error decreases and is almost negligible above $D_{in[7:0]}$ = 00000111. This is because during a lower duty ratio, the effect of propagation delay is significant, since the on-time is small.

Fig. 11 shows the eye diagram measurement of the proposed DPWM technique. It has an eye height (E_{height}) of 1.53 V and 316.52 ns width (E_{width}) for 18.991 M samples. The E_{height} is 0.63 V higher than $V_{DD}/2$ (0.9 V), which will minimize false triggering. A minimal variation of 3.49 ns between measured and ideal eye width (640 ns/2 = 320 ns) at 50% duty cycle proves that the DPWM is not affected by timing error at high clock frequency. Notably, the 18.991 M samples are not scattered, validating the effectiveness of our design.

Table 1
Theoretical values and Duty ratio comparison at various f_{clkin}.

$D_{in[7:0]}$	Duty ratio (%)				
	Ideal	100 MHz	250 MHz	350 MHz	400 MHz
00000001	0.39	0.37	0.54	0.68	0.43
00000011	1.17	1.02	2.63	0.98	1.01
00000111	2.73	2.70	2.63	2.5.0	2.45
00001111	5.85	5.83	5.70	5.56	5.59
00011111	12.10	12.10	12.00	11.90	11.90
00111111	24.60	24.60	24.50	24.40	24.40
01111111	49.60	49.60	49.50	49.40	49.40
11111111	99.60	99.60	99.50	99.60	99.50

The DPWM jitter measurement is illustrated in Fig. 12 at 50% Duty cycle and clkin = 400 MHz. It has a standard distribution curve based

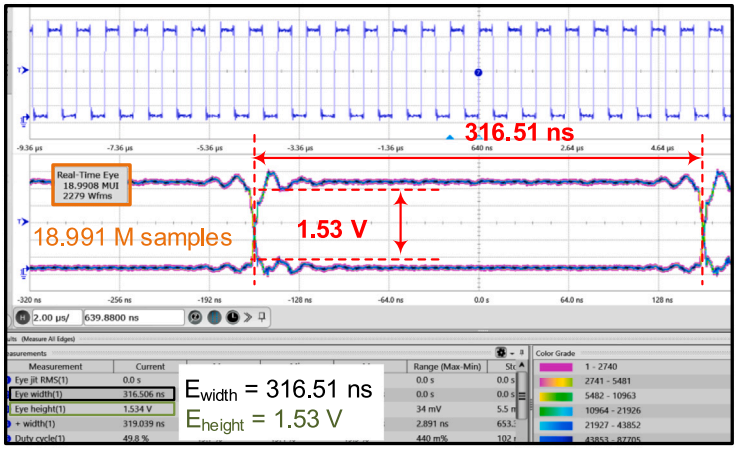

Fig. 11. Eye diagram measurement of our DPWM design.

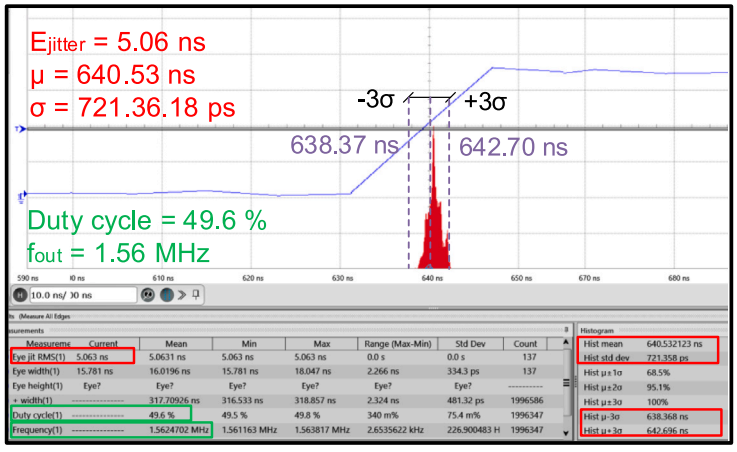

Fig. 12. Jitter measurement of our DPWM design.

Table 2
Performance comparison of DPWM design.

	[6]	[7]	[9]	[8]	This work
Year	2014	2019	2021	2024	2025
Publication	JSSC	ICEIC	AICSP	TVLSI	
Technology	40-nm	65-nm	180-nm	180-nm	180-nm
Verification	Meas.	Post-sim	Meas.	Meas.	Meas.
V_{supply}	0.6~1.1 V	0.6 V	1.3V	1.8 V	1.8 V
V_{out}	0.3 V~0.55 V	0.1~0.5 V	0.4~0.9 V	0.05~1.6 V	**0.014~1.79 V**
Output frequency (f_{out})	0.1 MHz	1 MHz	1.5~2 MHz	0.625~6.25 MHz	0.391~1.56 MHz
Resolution (bits)	6	6	5	4	**8**
No. of clk input	3	2	2	1	1
Clock frequency	6.4 MHz	64 MHz	2 MHz	100 MHz	**400 MHz**
Load	220 μH	4.7 μH	2.2 μH & 10 μF	30 pF	30 pF & 0.8 μH
Duty ratio range	0~50%	0~50%	30~70%	0~90.6%	**0~99.6** %
Core area (mm^2)	31.43	31.73	2.25	0.205	0.324
$Area_{norm}$ (chip area/$process^2$)	0.0196	0.0075	0.0694×10^{-3}	0.0063×10^{-3}	0.0100×10^{-3}
Power diss.	0.038 mW	0.180 mW	17.800 mW	3.400 mW	8.913 mW
$Power_{norm}$ (Power diss./V_{DD}^2)	31.41	500.00	10 532.54	1049.38	2528.70
FOM	3.11	14.20	9.57	5458.15	**12 604.09**

on random activities, having a considerable deviation (σ) of 721.36 ps and 640.53 ns mean (μ). The μ in the jitter measurement also projects almost the same value (640.00 ns) in Fig. 9(d).

Table 2 shows the performance comparison of prior DPWM reports and ours. Our DPWM design implemented a smaller number of DFFs compared to [6–8], exhibiting the minimal effect of clock skew with an increase in resolution. It has the highest resolution (N = 8) compared to the prior DPWM design, which is critical during high-accuracy applications. As a trade-off, it has a lower maximum output frequency of 1.56 MHz compared to [8]. The proposed DPWM also attains the highest input clock frequency of 400 MHz and voltage output range of 0.014 to 1.79 V. Our DPWM offers the highest modulated % Duty cycle equal to 99.6%, improving the line and load regulation required by many power converters. It also attains the highest FOM, which is calculated using Eq. (6).

$$\text{FOM} = \frac{\text{N} \times \text{Max.duty\%} \times \text{f}_{\text{clkin}}\ (\text{GHz})}{\text{Area}_{\text{norm}}\ (\text{mm}^2/(\text{nm})^2) \times \text{Power}_{\text{Norm}}\ (\mu/\text{V}^2)} \tag{6}$$

where $Area_{norm}$ is the normalized area and $Power_{norm}$ is the normalized power dissipation.

4. Conclusion

This paper presented a high duty cycle DPWM design fabricated using UMC 180-nm CMOS technology. The proposed DPWM utilized a small number of DFFs and was synchronized by a single clock. The architecture attains a wide range of input clock frequencies and is less affected by clock skew. The minimal variation of Duty ratio for different f_{clkin} proves the functionality of the DPWM design. Compared to prior works, it attains the highest f_{clkin} = 400 MHz and V_{out} range = 0.014~1.79 V with a maximum Duty ratio of 99.6%. Finally, the proposed DPWM can be used in high-accuracy applications, since it has the highest resolution of N = 8.

CRediT authorship contribution statement

Chua-Chin Wang: Conceptualization, Formal analysis, Interpretation of data, Writing – original draft,Writing – review & editing, Approval of the manuscript. **Oliver Lexter July Alvarez Jose:** Conceptualization, acquisition of data, Formal analysis, Interpretation of data, Writing – original draft,Writing – review & editing, Approval of the manuscript. **Venkata Naveen Kolakaluri:** Conceptualization, acquisition of data, Formal analysis, Interpretation of data, Writing – original draft,Writing – review & editing, Approval of the manuscript.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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