Journal of Circuits, Systems, and Computers
Vol. 35, No. 4 (2026) 2550423 (15 pages)
© World Scientific Publishing Company
DOI: 10.1142/S0218126625504237

World Scientific
www.worldscientific.com

A 49.23% Power Reduction Active Gate Driver with Digital Multi-level Power Gating Control

Chua-Chin Wang ¶

Institute of Integrated Circuit Design, National Sun Yat-sen University, No. 70, Lien-hai Road, Gushan, Kaohsiung 80424, Taiwan

Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung City 80424, Taiwan
ccwang@ee.nsysu.edu.tw

Pradyumna Vellanki,* Soumika Majumder,† L S S Pavan Kumar Chodisettii‡ and Venkata Naveen Kolakaluri§

Department of Electrical Engineering, National Sun Yat-sen University, No. 70, Lien-hai Road, Gushan, Kaohsiung 80424, Taiwan
**v.pradyumna93@gmail.com*
†*soumikamajumder387@gmail.com*
‡*pavanece9@gmail.com*
§*kvnaveen080@gmail.com*

Mitch Ming-Chi Chou

Academy of Innovative Semiconductor and Sustainable Manufacturing, National Cheng Kung University, Tainan 70101, Taiwan
z11308043@ncku.edu.tw

Lean Karlo Santos Tolentino

Department of Electronics Engineering, Technological University of the Philippines, Ermita, Manila 1000, Philippines
leankarlo_tolentino@tup.edu.ph

Received 2 April 2025
Accepted 30 June 2025
Published 20 August 2025

When it comes to power systems, both overall performance and efficiency are key factors in the design of the power device drivers. Using multi-level power gating logic, this study developed an active gate driver (AGD) design that is capable of driving the power transistor at different voltage levels. To lessen the amount of power that the AGD consumes, it is equipped with an effective power gating control logic. Additionally, the Four-stage Stability Control Circuit inside of the AGD makes certain that each and every power MOS device contained within the

¶Corresponding author.

buffer arrays of the Output Stage is equally utilized. For the implementation of the AGD design, the TSMC 180-nm High-voltage (HV) Bipolar-CMOS-DMOS (BCD) process was utilized. The measurement outcomes with C_{load} equal to 2 nF and an operating PWM frequency of 400 kHz validate the functionality of the AGD design. It dissipates an average of 533 mW, which is a combination of static and dynamic power. Finally, the power gating mechanism offers a power reduction of 49.23%, as determined by a comparison of two cycles with and without power gating circuit installed.

Keywords: Multi-level power gating; power device driver; four-stage stability control; power MOSFET; AGD.

1. Introduction

SiC and GaN devices are pivotal in advancing power electronics technology and enhancing power density, efficiency, and system integration.[1] The design of power semiconductor gate drivers significantly impacts their performance and efficiency, necessitating fine-tuning for optimal switching capabilities. This tuning is essential to reduce power losses during switching events and effectively suppress oscillations.[2]

A typical gate driver usually uses an open-loop control to improve SiC devices rising edge di/dt and dv/dt values.[3] A lot of passive and discrete off-the-shelf components make the design bulky. Also, the driver doesn't have any active feedback. Hence, it cannot compensate for variations in voltage and temperature. With regard to efficient adaptive gate drivers, the utilization of microcontrollers and field-programmable gate arrays (FPGAs) has been extensively documented.[4,5] However, adapting these models to suit distinct power devices while acknowledging the absence of real-time output data is crucial. These devices, comprising multiple integrated circuits, tend to have more significant form factors, necessitating high-cost data processors for handling computationally intensive tasks. Monitoring the gate voltage (V_g) of SiC or GaN devices is a core function of a dynamic gate driver chip during switching transients. Its main objective is to generate an optimized dynamic gate resistance (R_g) pattern.[6] However, implementing this optimized timing configuration for the gate driver chip using an FPGA amplifies area, complexity, and expense requirements. Meanwhile, a resistive gate driver (RGD) circuit effectively manages surge voltage, surge current, and switching losses by manipulating the switching waveform through R_g.[7] However, its capacity to adjust waveforms remains limited. Meanwhile, AGDs have proven effective in reducing electromagnetic interference (EMI) and improving power efficiency across various power semiconductor devices.[8] An AGD design utilizing a window comparator circuit was reported with huge power consumption.[9] A recent study on AGD design reported achieving only a 15% power reduction.[10]

A multi-level power gating logic-controlled driver is proposed in this investigation to precisely drive a 10-V power transistor device. It was successfully implemented utilizing 180-nm High-voltage (HV) Bipolar-CMOS-DMOS (BCD) technology, overcoming area limitations that often accompany AGDs employing both microcontroller and FPGA components. Furthermore, the power gating technique

integrated into the driver effectively reduces power dissipation caused by the operation of the Output Stage.

2. Active Gate Driver with Digital Multi-level Power Gating Control

The proposed active gate driver (AGD) with digital multi-level power gating control logic block diagram is shown in Fig. 1. It consists of the following blocks: Multi-level Power Gating Control Logic Circuit, Four-stage Stability Control Circuit, Transition Delay Generator, PMOS Control Pre-driver, NMOS Control Pre-driver, Voltage Level Shifter, Phase Synchronizer, and Output Stage.

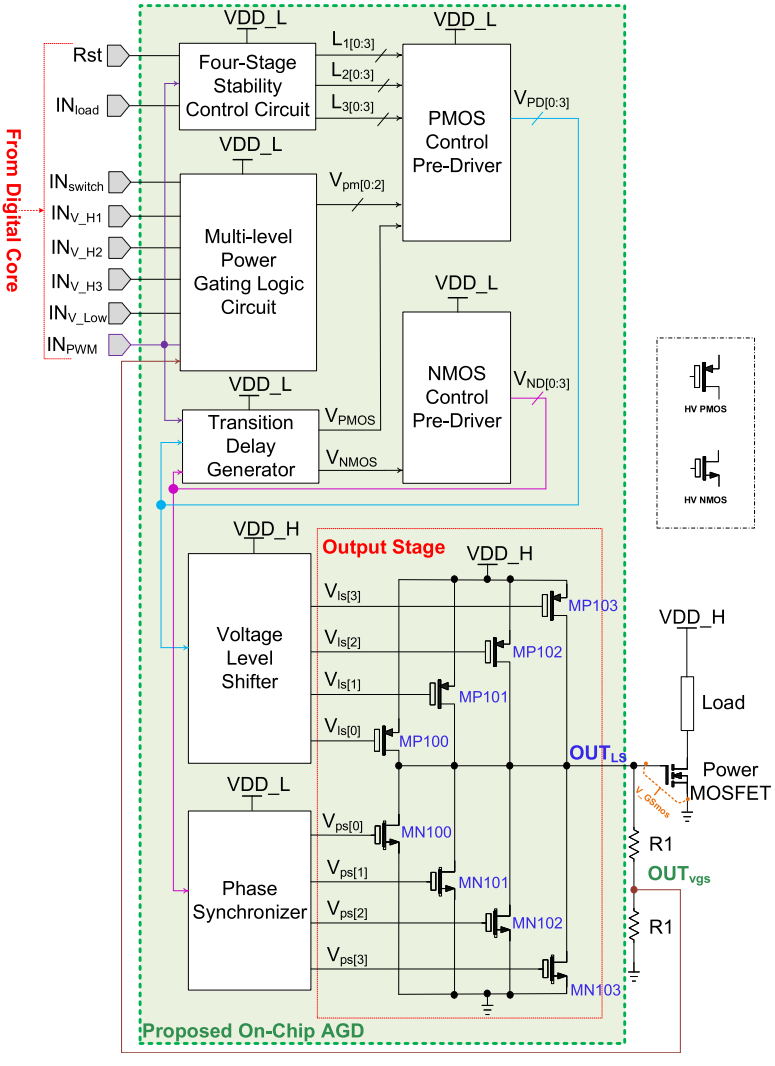


Fig. 1. Block diagram of the proposed AGD with multi-level power gating logic.

The Transition Delay Generator resolves the IN_{PWM} signal from the Digital Core into two nonoverlapping signals, V_{PMOS} and V_{NMOS}. One of its inputs, $V_{PD[0:3]}$, is influenced by the Four-stage Stability Control Circuit, which plays a critical role in maintaining uniform operation among the HV MOS devices in the Output Stage. The Four-stage Stability Control Circuit consists of programmable shift registers and ensures each PMOS in the Output Stage is activated evenly to prevent mismatches. It operates by assigning time-slotted positions for the activation of each PMOS based on IN_{PWM}, which is also used to control transition timing.

The Transition Delay Generator adjusts the delay between V_{PMOS} and V_{NMOS} based on the switching state of the PMOS and NMOS transistors in the Output Stage. The delay between the nonoverlapping signals is also known as dead time. This dead time is necessary for the reliable operation of the PMOS and NMOS transistors in the Output Stage. Due to the design limitation of the PMOS in the T18HVG2 process, the PMOS gate can only handle a V_{GS} difference of 5 V. Since the V_GSmos signal swing to drive the external Power MOSFET needs to be 10 V due to the power MOS requirements, the gate signal needs a Voltage Level Shifter to shift from the 0–5 V range to the 5–10 V range. The Voltage Level Shifter generates a propagation delay in PMOS gate signals due to the level shift process. The Phase Synchronizer matches for this propagation delay by adding additional delay to the NMOS gate signals. The Phase Synchronizer employs a sequence of inverters to counterbalance the delay produced by the Output Stage.[11] The supply voltages are VDD_H = 10 V and VDD_L = 5 V in this investigation. Transistors implemented in all the blocks except the Level Shifter and the Output Stage are 5-V, low-voltage MOS devices.

The Output Stage of the proposed AGD comprises 4-PMOS and 4-NMOS arrays, producing current in four cases. Its PMOS (MP100, MP101, MP102, and MP103) and NMOS (MN100, MN101, MN102, and MN103) devices are HV devices. Notably, $V_{ls[0:3]}$ can be adjusted by the Voltage Level Shifter for its proper driving from 0–5 V to 5–10 V.[12]

The Multi-level Power Gating Logic Circuit uses the output signal OUT_{vgs} as a feedback signal. It is detected by multiple levels, namely IN_{V_H1}, IN_{V_H2}, and IN_{V_H3}. When OUT_{vgs} is less than IN_{V_LOW}, the signal is reset.

2.1. *Multi-level power gating: Concept and realization*

The power gating signals are generated from the Multi-level Power Gating Logic Circuit. It detects OUT_{vgs} at various levels, e.g., when $OUT_{vgs} \geq 0.8$ VDD_L, $OUT_{vgs} \geq 0.6$ VDD_L, and $OUT_{vgs} \geq 0.4$ VDD_L. It resets the signal when $OUT_{vgs} \leq 0.2$ VDD_L. Four PMOS devices of Output Stage can share an equal load of current; each PMOS can contribute 25% of it. It is widely known the way to charge and discharge a capacitor in an RC circuit. The transition event of the PMOS in Output Stage can be recognized using the same RC concept. The complimentary values of $\%V_{max}$ and $\%I_{max}$ are referring to Table 1, an example is that when OUT_{vgs} reaches

Table 1. $\%V_{\max}$ and $\%I_{\max}$ at Different Time Constants in RC circuit.

Time constant $(R_g \cdot C_g)$	$\%V_{\max}$	$\%I_{\max}$
5.0	99.3	0.79
4.0	98.2	1.80
3.0	95.5	5.00
2.0	86.5	13.5
1.0	63.2	36.8
0.7	50.3	49.7
0.5	39.3	60.7

40% of VDD_L, the maximum $I_{\max}$ required is 60.7%. Based on the RC model concept, we can conclude that shutting off the PMOS devices in the Output Stage will allow us to bring down the overall power consumption of the proposed driver.

Figure 2 shows the timing diagram of power gating analysis in one of the four PMOS levels. During turn-on, OUT_{vgs} starts to rise when IN_{PWM} is high while $V_{\text{PD}[0:3]}$ is low. Notably, as OUT_{vgs} is increasing, $V_{\text{PD}[1]}$, $V_{\text{PD}[2]}$, and $V_{\text{PD}[3]}$ go high at T_{11}, T_{12}, and T_{13} intervals. However, as OUT_{vgs} is increasing, the overall power $(P_{\text{VDD_L+VDD_H}})$ decreases until such time that IN_{PWM} becomes low and OUT_{vgs} reaches 100% of VDD_L. This makes $V_{\text{PD}[0:3]}$ to go high, making $P_{\text{VDD_L+VDD_H}}$ equal to 0.

The Multi-level Power Gating Logic Circuit is shown in Fig. 3, consists of four hysteresis comparators and three latch detectors for three levels. The hysteresis comparators (C1–C4) shown in Fig. 3 are modified versions of the basic design.[13] These comparators are optimized to achieve low static power dissipation while maintaining a high slew rate. These comparators compare four different input voltage levels ranging from 0 to 5 V with the feedback output voltage, OUT_{vgs}. The schematic diagram of the hysteresis comparator is depicted in Fig. 4. The V_{pow} signal from the Power Gating Circuit acts as an enable input for the comparators.

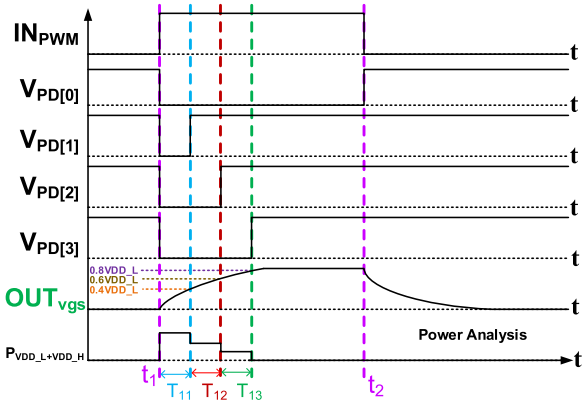


Fig. 2. Timing diagram of the power gating analysis in one of the four PMOS levels.

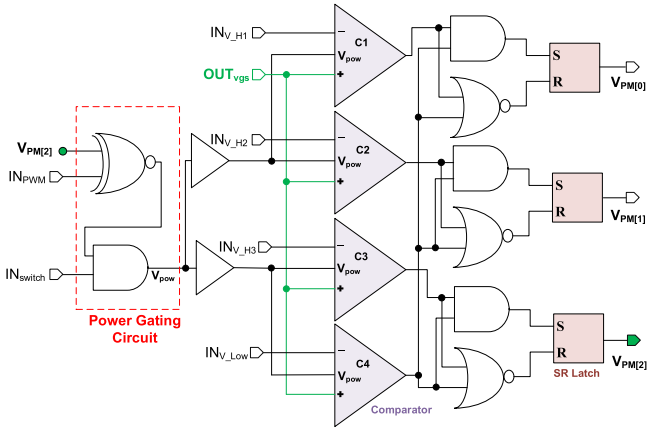


Fig. 3. Multi-level Power Gating Logic Circuit.

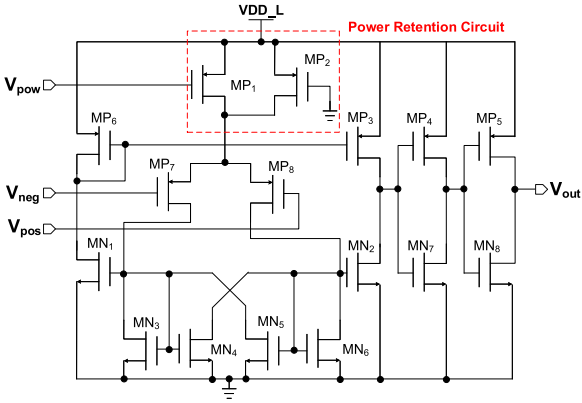


Fig. 4. Schematic of the hysteresis comparator.

The output of the comparator goes logic high when the voltage at the positive terminal exceeds that at the negative terminal, and vice versa.

Each latch detector works for each case, which consists of two voltage references. When the OUT_{vgs} signal goes higher than the two other voltage references, the latch turns ON. Moreover, the latch turns OFF when the OUT_{vgs} signal goes below the other voltage references. This block generates the control signals required for the power gating.

Each latch detector corresponds to a different voltage level. Three different external voltage inputs, IN_{V_H1}, IN_{V_H2}, and IN_{V_H3} generate the three different voltage levels for power gating in the four PMOS of the Output Stage. The minimum voltage input, IN_{V_Low}, which resets the whole driver, is 0.2 VDD_L. The different voltage levels for IN_{V_H1}, IN_{V_H2}, and IN_{V_H3} used in this proposed driver are 0.4 VDD_L, 0.6 VDD_L, and 0.8 VDD_L, respectively. These voltage levels are chosen to

enable efficient and stepwise power gating, allowing different portions of the circuit to be progressively turned off, reducing power consumption while still maintaining functionality where needed. As $\mathrm{OUT_{vgs}}$ increases, the maximum current ($I_{\max}$) requirement decreases, allowing for more transistors (PMOS) to be powered down without affecting the ability of the circuit to meet performance demands. When $\mathrm{OUT_{vgs}}$ reaches 40% of VDD_L, the $I_{\max}$ required is approximately 60% of $I_{\max}$. Similarly, when $\mathrm{OUT_{vgs}}$ reaches 80% of VDD_L, only 20% of $I_{\max}$ is needed, allowing more aggressive power gating.

2.2. *Four-stage stability control circuit*

This block as shown in Fig. 5 consists of three programmable parallel-in parallel-out (PIPO) shift registers. $\mathrm{IN_{PWM}}$ signal works as a clock in the shift registers that generate different positions for each PMOS in the Output Stage to be turned ON. This makes sure that each MOS is equally used and no mismatch issue occurs. The Load pin ($\mathrm{IN_{LOAD}}$) loads the sequence. The Rst signal resets the block. $L_{1[0:3]}$ gives the positions of four PMOS for one level.

2.3. *Transition delay time generator*

The Transition Delay Generator is responsible for generating the interval of time, known as dead time, which is needed between the transitions of the Output Stage. It is based on the feedback-controlled split-path CMOS buffer.[14] The system identifies the buffer array with the slowest rise time/fall time. Upon identifying the buffer with

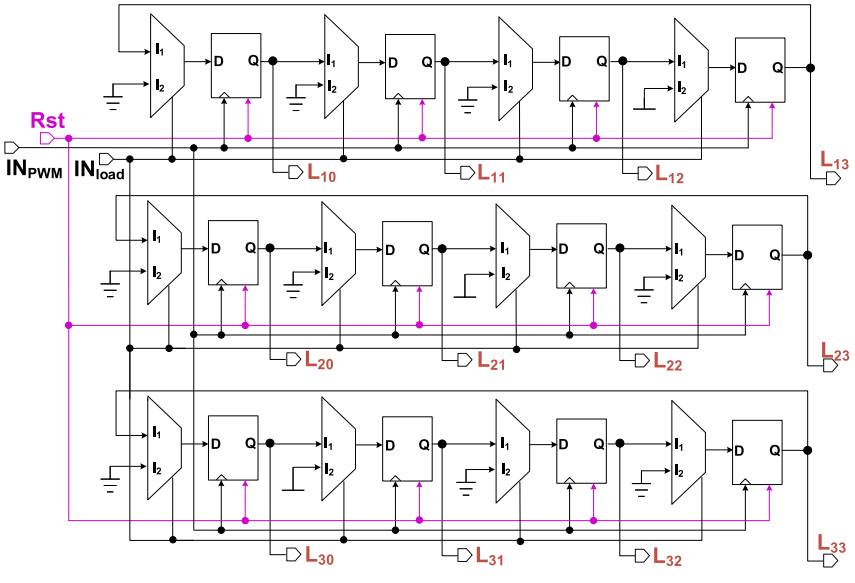


Fig. 5. Four-stage stability control circuit.

the slowest speed, the CMOS Schmitt trigger counteracts this by generating an additional delay for the remaining buffers so that the short-circuit currents are prevented.

2.4. *PMOS control pre-driver and NMOS control pre-driver*

As shown in Fig. 6, the Pre-driver circuit makes decisions on which MOS in the Output Stage to turn on compared with the output of the Multi-level Power Gating Logic Circuit and the output of Four-stage Stability Control Circuit. It can be better understood in terms of matrix format where rows indicate the levels and columns indicate the positions of the MOS to be turned on, e.g., [0001], [0010], [0100]. The following equation gives the logic implementation:

$$V_{\mathrm{PD}[0:3]} = (L_{1[0:3]} \cdot V_{\mathrm{PM0}}) + (L_{2[0:3]} \cdot V_{\mathrm{PM1}}) + (L_{3[0:3]} \cdot V_{\mathrm{PM2}}) + V_{\mathrm{PMOS}}. \quad (1)$$

This logic finally activates the power gating in the gate driver. Notably, NMOS control Pre-driver is identical to that for PMOS counterpart.

Referring to the timing diagram as shown in Fig. 7, when $\mathrm{IN}_{\mathrm{PWM}}$ is high and $V_{\mathrm{PD}[0]}$ is low, then MP100 will be ON. $\Delta t_{\mathrm{VPD0_low}}$ denotes the ON time of MP100. Moreover,

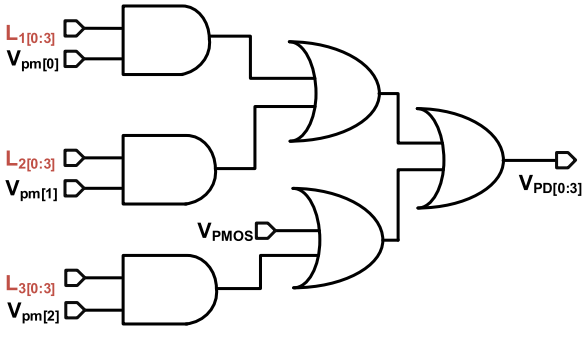


Fig. 6. Pre-driver circuit for PMOS transistors.

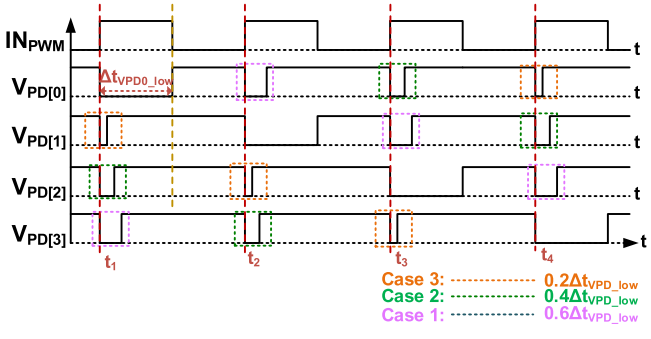


Fig. 7. Timing diagram of the PMOS Pre-driver Outputs for the AGD.

Table 2. Various cases at the output.

Output case	ON transistor	Time period	$\%I_{max}$
Case 1	MP100, MP101, MP102	T_{11}	0.75
Case 2	MP100, MP101	T_{12}	0.50
Case 3	MP100	T_{13}	0.25

the following cases considering the condition of the PMOS Pre-driver Outputs are stated as follows:

(1) Case 1: As one PMOS (MP103) is turned off and three PMOS (MP100, MP101, MP102) are turned on when $V_{PD[0:2]}$ is high, it generates 75% of the I_{max}, greater than 60.7%.
(2) Case 2: When OUT_{vgs} reaches 60% of VDD_L, the maximum I_{max} required is 40%. At this time, since $V_{PD[0:1]}$ is high, two PMOS (MP100 and MP101) are turned on. They generate 50% of the I_{max}, which is greater than 40%.
(3) Case 3: When OUT_{vgs} reaches 80% of VDD_L, the maximum I_{max} required is 20%. Since only $V_{PD[0]}$ is high, one PMOS (MP100) is turned on. It generates 25% of the I_{max}, greater than the required 20%.

Table 2 summarizes the above operations.

3. Simulations and Measurement Analysis

TSMC 180-nm HV BCD process was used to realize the proposed AGD. Figure 8 shows the die photo and floorplan of the proposed AGD. The core and chip area of the AGD are $4.5 \times 0.63\,mm^2$ and $4.9 \times 1.05\,mm^2$, respectively.

Figure 9 shows the measurement setup. The two different voltage inputs (VDD_L = 5 V and VDD_H = 10 V) are supplied to the fabricated chip using a DC

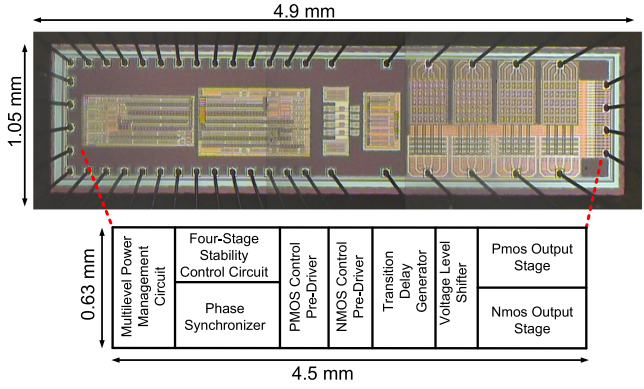


Fig. 8. Die photo and floorplan of the proposed AGD.

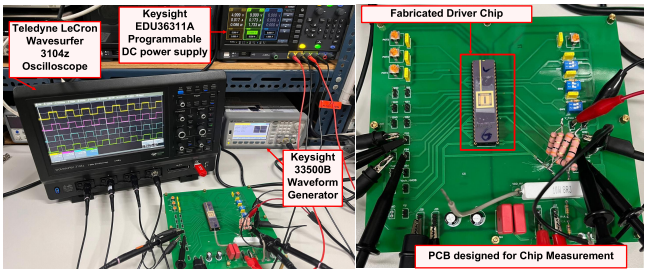


Fig. 9. Measurement environment of the chip.

power supply (Keysight EDU36311A). A waveform generator (Keysight 33500B) produces the required 400 kHz IN_{PWM} input frequency to drive the proposed driver. The oscilloscope (Teledyne LeCroy WaveSurfer 3104z), labeled in the measurement setup image, visually displays the output waveforms of the fabricated chip. The Power MOSFET used on the PCB for measurements is the IMW65R107M1H SiC MOSFET from Infineon.

The timing diagram of the proposed AGD depicted in Fig. 2 is verified in the post-layout simulations, shown in Fig. 10 and in measurement as shown in Figs. 11 and 12. It also illustrates various trigger levels and their corresponding control signals,

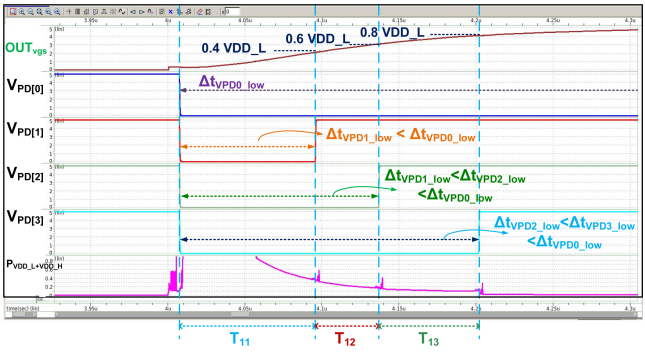


Fig. 10. Power Gating analysis in post-layout simulations.

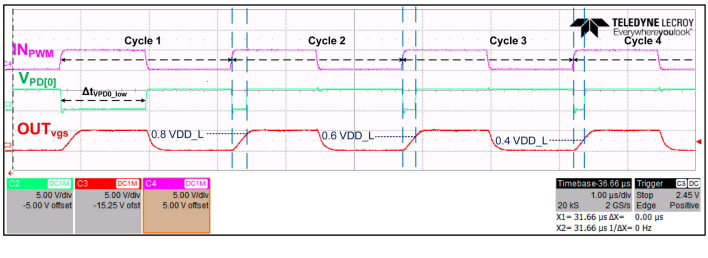


Fig. 11. Power Gating analysis in measurement for four cycles of IN_{PWM}.

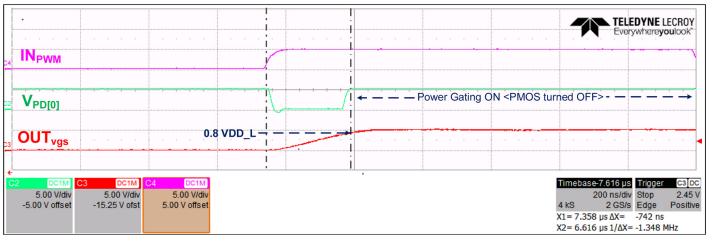


Fig. 12. Power Gating analysis in measurement for one cycle of $\mathrm{IN_{PWM}}$.

notably $V_{\mathrm{PD}[0:3]}$, output signals from the Pre-driver block. Figure 10 also shows a correlation between the voltage trigger level and the on-time of the PMOS control signal. The timing intervals T_{11}, T_{12}, and T_{13} serve as the starting points for the various PMOS. As the voltage level rises in the $\mathrm{OUT_{vgs}}$ signal, so does the number of PMOS turned off, resulting in lower static power consumption, as shown in the post-layout simulation between intervals T_{11} and T_{13}.

The measurement shown in Fig. 13 demonstrates when a 5 V input signal $\mathrm{IN_{PWM}}$ applied to the chip produced an output signal $\mathrm{OUT_{LS}}$ achieving 10 V. Figure 14 shows the four output signals from the Pre-driver block, $V_{\mathrm{PD}[0:3]}$, when the Power Gating is disabled, showing the four PMOS transistors turning on and off in sync with the reference input signal. Figure 15 shows the measurement results of $V_{\mathrm{PD}[0:3]}$ when Power Gating is enabled. In the enable state, the power consumption is

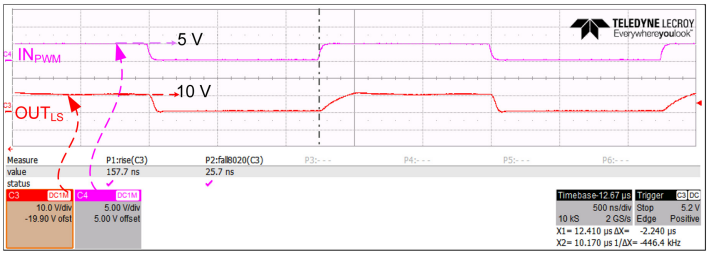


Fig. 13. AGD 10 V output ($\mathrm{OUT_{LS}}$) with 5 V input ($\mathrm{IN_{PWM}}$).

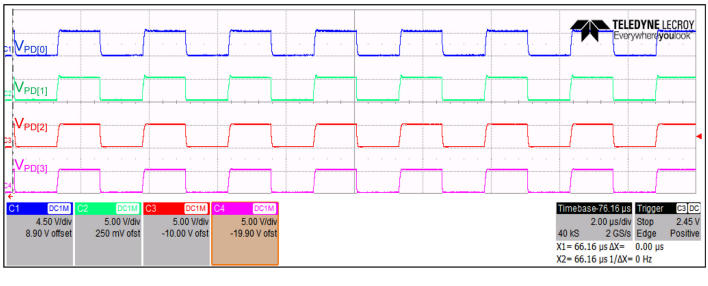


Fig. 14. PMOS control signals without power gating.

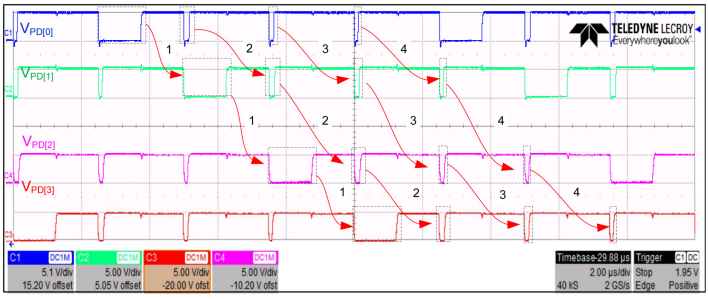


Fig. 15. PMOS control signals with power gating.

533 mW. These images also verify the effective operation of the proposed Four-stage Stability Control Circuit and Pre-driver block within the driver architecture. The transition sequence is illustrated using the numbers 1, 2, 3, and 4 to enhance the visualization of the verification process. The label "1" indicates that the ON time of the PMOS matches the ON time of the $\mathrm{IN_{PWM}}$ signal. Labels "2", "3", and "4" show that the ON time gradually decreases according to the requirements of the $\mathrm{OUT_{vgs}}$ signal to be activated. This sequence also demonstrates that each PMOS turns on at different points depending on the voltage level of VDD_L, as mentioned in the timing diagrams in Figs. 2 and 7.

During the post-layout simulations, our design was evaluated across all PVT corners using an $\mathrm{IN_{PWM}}$ frequency of 0.5 MHz and a load capacitance of 2 nF. At the worst-case corner, i.e., [FF, 1.1 × (VDDH, VDDL), 0°C], the reduction in overall power dissipation is 42.21%. At this corner, the Rise time (t_{rise}) was 261 ns, and Fall time (t_{fall}) was 234 ns.

In measurements, when the proposed AGD drives the IMW65R107M1H SiC MOSFET from Infineon with an $\mathrm{IN_{PWM}}$ frequency of 0.4 MHz and 2 nF as load capacitance, the average power dissipation $P_{\mathrm{dis_total}}$, i.e., combined static and dynamic power, is 533 mW with Power Gating. However, it is 1.05 W without Power Gating. Hence, 517 mW or 49.23% of overall power dissipation is reduced. Figure 16 shows the measured values of t_{rise} and t_{fall} as 197.8 ns and 94.2 ns, respectively. The high t_{rise} is due to the use of a Voltage Level Shifter in the proposed driver, which shifts the control signals ($V_{\mathrm{PD[0:3]}}$) from the 0–5 V range to the 5–10 V range ($V_{\mathrm{ls[0:3]}}$)

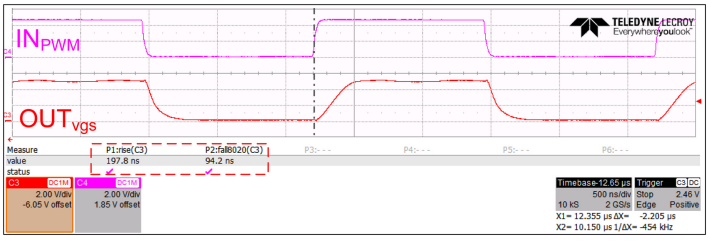


Fig. 16. Rise time and Fall time measurements for an $\mathrm{IN_{PWM}}$ of 400 kHz.

Table 3. Performance comparison.

	15	4	6	9	This work
Year	2018	2019	2022	2023	2024
Publication	JSSC	TPE	ISPSD	MWSCAS	
Technology (nm)	180 BCD	CPLD	180 BCD + FPGA	180 T18HVG2	180 BCD
Driver type	Passive	Active	Active	Active	Active
Verification	Meas.	Meas.	Meas.	Post Sim.	Meas.
V_{DD} (V)	15	20 and −5	1.8, 3.3 and 20	12	5 and 10
f_{PWM_in} (MHz)	1	9.2	0.1	0.5	0.4
t_{rise} (ns)	5.6 at 5 V	N.A.	N.A.	153 at 12 V	197.8 at 10 V
t_{fall} (ns)	N.A.	N.A.	N.A.	187 at 12 V	94.2 at 10 V
C_{load} (nF)	2.7	N.A.	2	2	2
Chip area (mm^2)	4.9 × 2.3	N.A.	2.5 × 2.5	4.515 × 3.26	4.9 × 1.05
P_{dis_total}	N.A.	N.A.	79.51 mW[a]	32,700 mW	533 mW

[a]Power consumption of FPGA is excluded.

to drive the external Power MOSFET. This level shifting introduces propagation delay and signal degradation, significantly affecting the PMOS rising edge and transition speed. On the other hand, the t_{fall} is significantly faster because the NMOS pull-down path does not involve level shifting and benefits from direct, faster discharging of the load capacitor.

The reduction in IN_{PWM} frequency during measurements is due to the limitations of Four-stage Stability Control Circuit. At higher clock frequencies, the shorter time intervals between clock edges reduce the time available for signal transitions. Because of a weak power line in the circuit, the output lines L_{13}, L_{23}, and L_{33} were not driving the PMOS transistor (MP103) in the Output Stage properly, preventing it from responding effectively under these conditions. To mitigate this issue, the IN_{PWM} frequency shall be reduced.

Table 3 summarizes the performance comparison of the recent power MOS driver designs. Referring to Table 3, 4.9 × 1.05 mm^2 is the total core area of the proposed design, which is relatively smaller than previous works.[6,9,15] The power dissipation of the previously reported design was 79.51 mW, but this excludes the power consumption of external FPGA and operates at low PWM frequency.[6] Compared to designs requiring external FPGA control (e.g., Ref. 6), our approach reduces overall system complexity by eliminating the need for additional components.

4. Conclusion

An AGD single-chip design for driving power transistors implemented using the TSMC 180-nm HV BCD process is presented in this paper. It incorporates Multi-level Power Gating Logic and a Four-stage Stability Control Circuit. It is validated through measurement outcomes, demonstrating an average power dissipation of 533 mW at 400 kHz PWM frequency. The AGD with the power gating system achieves a notable power reduction of 49.23%, highlighting its efficacy in

enhancing the efficiency of the driver. In the future, to enhance design performance at higher frequencies, the Power Retention Circuit of the hysteresis comparator can be optimized to deliver high slew rate currents, thereby enabling faster transitions of comparator. Additionally, the Four-stage Stability Control Circuit can be improved by replacing the D-flip flop with a Master-slave D-flip flop. This modification could provide better read and write margins, ensuring accurate data retrieval and generating output data on the subsequent clock edge. These enhancements would contribute to improved system stability and greater robustness against noise.

Acknowledgments

The EDA tool employed by TSRI in NARLabs is widely acknowledged for its excellence. NSTC of Taiwan partially funded this study under grants NSTC 112-2218-E-110-009-, NSTC 112-2221-E-110-063-MY3, NSTC 112-2923-E-006-003-MY3 and NSTC 113-2923-E-110-001-.

ORCID

Chua-Chin Wang https://orcid.org/0000-0002-2426-2879
Pradyumna Vellanki https://orcid.org/0009-0000-0768-188X
L S S Pavan Kumar Chodisettii https://orcid.org/0009-0009-7310-8323
Lean Karlo Santos Tolentino https://orcid.org/0000-0002-8014-8229

References

1. J. G. Kassakian and T. M. Jahns, Evolving and emerging applications of power electronics in systems, *IEEE J. Emerg. Sel. Topics Power Electron.* **1** (2013) 47–58.
2. C.-C. Wang, O. L. J. A. Jose, P.-K. Su, L. K. S. Tolentino, R. G. B. Sangalang, J. S. Velasco and T.-J. Lee, An adaptive constant current and voltage mode P&O-based Maximum Power Point Tracking controller IC using 0.5-μm HV CMOS, *Microelectronics J.* **118** (2021) 1–12.
3. Y. Han, H. Lu, Y. Li and J. Chai, Open-loop gate control for optimizing the turn-ON transition of SiC MOSFETs, *IEEE J. Emerg. Sel. Topics Power Electron.* **7** (2019) 1126–1136.
4. Y. Yang, Y. Wen and Y. Gao, A novel active gate driver for improving switching performance of high-power SiC MOSFET modules, *IEEE Trans. Power Electron.* **34** (2019) 7775–7787.
5. S. Zhao, X. Zhao, A. Dearien, Y. Wu, Y. Zhao and H. A. Mantooth, An intelligent versatile model-based trajectory-optimized active gate driver for silicon carbide devices, *IEEE J. Emerg. Sel. Topics Power Electron.* **8** (2020) 429–441.
6. W. T. Cui, W. J. Zhang, J. Y. Liang, H. Nishio, H. Sumida, H. Nakajima, Y.-T. Hsieh, H.-H. Tsai, Y.-Z. Juang, W.-K. Yeh and W. T. Ng, A dynamic gate driver IC with automated pattern optimization for SiC power MOSFETs, *Proc. 2022 IEEE 34th Int. Symp. Power Semiconductor Devices and ICs (ISPSD)* (IEEE, 2022), pp. 33–36.
7. Y. Noge, M. Shoyama and M. Deng, Active gate driver for high power SiC-MOSFET module with source current feedback and P-D controller, *Proc. 2021 IEEE 12th Energy Conversion Congr. Expo. — Asia (ECCE-Asia)* (IEEE, 2021), pp. 1350–1353.

8. D. Liu, H. C. P. Dymond, J. Wang, B. H. Stark and S. J. Hollis, Building blocks for future dual-channel GaN gate drivers: Arbitrary waveform driver, bootstrap voltage supply, and level shifter, *Proc. 2019 31st Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, Shanghai, China, May 2019, pp. 79–82.
9. O. L. J. A. Jose, J.-M. Kuo, V. N. Kolakaluri and C.-C. Wang, SiC MOSFET high side gate driver design using HV CMOS process, *Proc. 2023 IEEE 66th Int. Midwest Symp. Circuits and Systems (MWSCAS)* (IEEE, 2023), pp. 45–49.
10. P. Vellanki, V. N. Kolakaluri, Y.-C. Chang, L. S. S. P. K. Chodisetti, M. M.-C. Chou and C.-C. Wang, Active gate driver design using differential timing-based miller detector for power MOSFET, *Proc. 2024 IEEE Asia Pacific Conf. Circuits and Systems (APCCAS)*, Taipei, Taiwan, November 2024, pp. 744–748.
11. K.-H. Cheng, W.-B. Yang and H.-Y. Huang, The charge-transfer feedback-controlled split-path CMOS buffer, *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.* **46** (1999) 346–348.
12. B. Yuan, L.-Q. Xiao, B.-Y. Wang and J. Ying, High-speed dynamic level shifter for high-side bootstrapped gate driver in high-voltage buck regulators, *IEEE Trans. Circuits Syst. II: Express Briefs* **68** (2021) 3083–3087.
13. C. F. Lee and P. K. T. Mok, A monolithic current-mode CMOS DC–DC converter with on-chip current-sensing technique, *IEEE J. Solid-State Circuits* **39** (2004) 3–14.
14. H.-Y. Huang and Y.-H. Chu, Feedback-controlled split-path CMOS buffer, *Proc. 1996 IEEE Int. Symp. Circuits and Systems (ISCAS)* (IEEE, 1996), pp. 300–303.
15. A. Seidel and B. Wicht, Integrated gate drivers based on high-voltage energy storing for GaN transistors, *IEEE J. Solid-State Circuits* **53** (2018) 3446–3454.