A 24.9% Power Reduction Active Gate Driver With Power Gating and Current Modulation for Power MOSFETs

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***Abstract*—The configuration of an active gate driver (AGD) plays a crucial role in determining the performance and efficiency of power semiconductor devices. This research introduces a novel AGD that accurately detects the Miller plateau during turn-on and turn-off transitions using a a Differential timing-based Miller detector. Additionally, a power gating mechanism is implemented to deactivate N-1 PMOS devices in the Output stage, effectively minimizing power loss. To further enhance efficiency, a newly designed current modulation circuit is integrated, reducing overall power consumption. The AGD is fabricated using TSMC T18HVG2 process, and comprehensive measurements validate its functionality at an operating frequency of 500 kHz. Experimental results show that the average total power dissipation with power gating is 568 mW. Moreover, the combined power gating mechanism and current modulation circuit achieve a significant 24.9% reduction in static power dissipation.**

***Index Terms*—Miller region, AGD, power gating, power MOSFET, current modulator, power reduction**

I. Introduction

Power electronics refers to circuits that convert or process energy. The power electronic system comprises semiconductor devices like Insulated-Gate Bipolar Transistor (IGBT), Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), etc [1]. The design of these devices' gate drivers, on the other hand, has a considerable impact on the performance and efficiency of these power devices. It is vital to optimize the design of the gate driver to obtain optimal switching performance while simultaneously minimizing switching losses and suppressing oscillations [2].

Gate drive circuits can be classified into two types, namely passive gate drive circuits (PGD) and active gate drive circuits (AGD). The PGD use a gate resistor to control the MOSFET switching parameters. In PGDs, the gate resistance value is designed to reduce the transient noise (EMI) without giving up too much in terms of switching losses (power loss), resulting in a sub-par performance of the switch. Active gate drive circuits are able to optimize the switch parameters without sacrificing the others [3], [4]. AGD can be implemented in open-loop or closed-loop configurations. In open-loop configuration, the gate voltage or the gate resistance value is modulated based on pre-determined data bank values. Usually, the data-bank values are acquired from the datasheet of the power semiconductor switch or experimental results. Even though they are effective at optimizing the switching performance of the power semiconductor device, they do not compensate for real-time fluctuations caused by external factors like temperature or supply voltage variations. Closed-loop active gate drive circuits overcome this shortcoming using real-time feedback from the power semiconductor switch parameters [3], [4].

The Miller plateau in power MOSFETs represents a phase during switching when the gate-source voltage remains constant, corresponding to the charging or discharging of the drain-gate capacitance [5]. Several methods have been developed to mitigate the adverse effects of the Miller plateau.

A resistance modulation-based active gate drive circuit was discussed in [6]. This circuit that is designed to reduce surge voltage, surge current, and switching losses. This AGD varies the gate resistance to alter the switch performance. The digital nature of the circuit makes it more reliable. However, the circuit is an open loop and does not have feedback. Hence, the AGD cannot compensate nor calibrate for the real-time temperature and voltage fluctuations.

Cui *et al.* presented a dynamic resistance-based AGD, which adopts a closed-loop approach, unlike the prior work [7]. The circuits adjust the driving resistance dynamically during turn-on and turn-off transitions. Also, it updates the resistance pattern after every switch transition cycle. The control signal is generated with the help of a programmable device, namely FPGA. However, the external FPGA used in the system makes it bulky and expensive to produce.

We already introduced a 2-level Miller detector based AGD previously, which is verified through post-layout simulations and suffers with redundant static power dissipation [8].

This work presents an AGD design that makes use of Differential timing-based Miller detector (DTMD) to identify the Miller plateau before and after power MOSFET are turned on and off, respectively. When the V_GSmos and V_DSmos of the power transistor are taken into consideration, the Miller plateau is detected, which results in an improvement in the detection accuracy. Through the use of the novel power gating mechanism combined with current modulation circuit, the driver was able to limit the amount of power dissipation that was caused by the Level Shifter.

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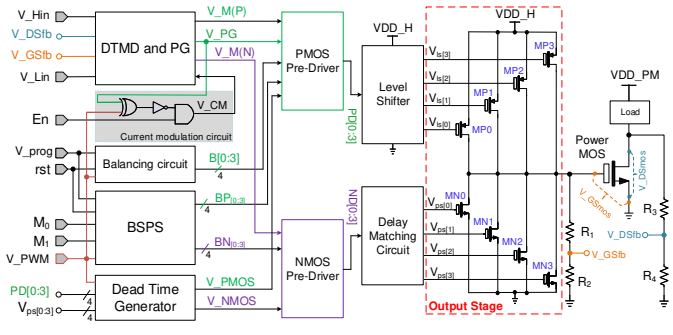

Fig. 1. Proposed AGD block diagram

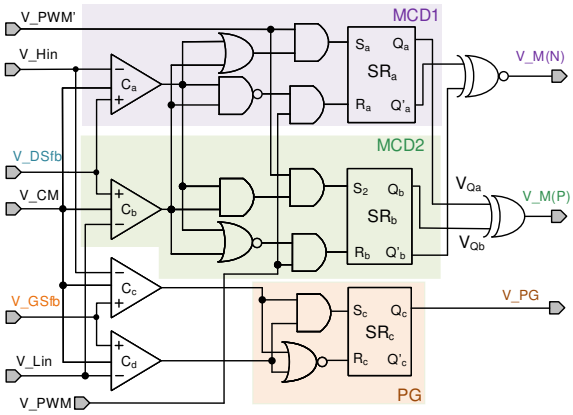

Fig. 2. Schematic of the DTMD

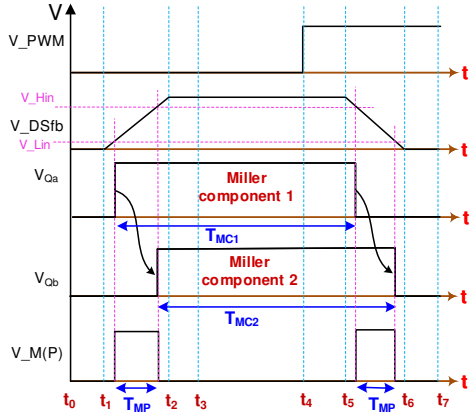

Fig. 3. Timing diagram for Miller component detection

II. Proposed Active Gate Drive Circuit

Figure 1 depicts the functional block diagram of the proposed AGD. Our novel contributions includes a DTMD, power-gating circuit (PG), and Current modulation circuit (CM). The remaining circuits like Balancing Circuit, Dead Time Generator, Buffer strength profile selector (BSPS), PMOS/NMOS Pre-Driver, Delay Matching Circuit, Level Shifter, and Output Stage all are sourced from our previous work [8].

The Dead Time Generator resolves the V_PWM signal from the controller into two non-overlapping signals, V_PMOS and V_NMOS. The circuitry adjusts the delay between V_PMOS and V_NMOS based on the switching state of the PMOS and NMOS transistors in the Output Stage. The delay between the non-overlapping signals is also known as dead time. This dead time is necessary for the reliable operation of the PMOS and NMOS transistors in the Output Stage. Due to the design limitation of the PMOS in the T18HVG2 process, the PMOS gate can only handle a V_{GS} difference of 5 V. Since the V_GSmos signal swing needs to be 10 V due to the power MOS requirements, the gate signal needs a Level Shifter Circuit to shift from the 0–5 V range to the 5–10 V range. The Level Shifter generates a propagation delay in PMOS gate signals due the level shift process. The Delay Matching Circuit matches for this propagation delay by adding additional delay to the NMOS gate signals.

The BSPS determines the number of PMOS and NMOS that turn-off during the Miller period. The number of PMOS and NMOS devices is determined by the Mode Input M_1 M_0. Turning-off the PMOS/NMOS in the Output Stage can cause mismatch between the individual MOS in the Output Stage. The Balancing Circuit tries to mitigate the mismatch between the individual MOS in the PMOS/NMOS in the Output Stage by turning-off different MOS in every V_PWM cycle.

The DTMD identifies the Miller region in the V_GSmos signal with the help of scaled-down Power MOS parameters V_GSfb and V_DSfb. The PG Circuit reduces redundant power dissipation in the Level Shifter. When V_GSmos reaches over 0.9 V_{DD}, the PG Circuit shuts-off (N-1) PMOS in the Output Buffer to reduce power dissipation. The PMOS and NMOS Pre-Driver circuits determine the individual MOS states in the Output Stage, respectively. The PMOS and NMOS Pre-Driver circuits generate signals V_PD[0:3] and V_ND[0:3] based on the inputs from other circuits like the DTMD, PG, Balancing Circuit, BSPS, and Dead Time Generator. The Output Stage generate the power MOS gate drive signal V_GSmos.

A. Differential timing-based Miller detector (DTMD)

Fig. 2 illustrates the DTMD, which implements an innovative technique to precisely identify minor fluctuations in the Miller time period T_{MP}. T_{MP} is characterized as the phase shift between two Miller component signals, V_{Qa} and V_{Qb}, which originate from Miller component detectors MCD1 and MCD2, respectively. These detectors incorporate a comparator pair, C_a and C_b, to monitor transitions in the V_DSfb signal, generating a signal whose pulse width is determined by the voltage differential between the reference levels V_Hin and VL_in. For MCD1, the OR and NAND logic gates regulate the S_a and R_a inputs of the SR_a latch. Additionally, a pair of AND gates facilitates the interleaving process of S_a and R_a, ensuring the SR_a latch does not enter an indeterminate state. This interleaving mechanism is achieved by supplying V_PWM and its inverse V_PWM' to the AND gates. As depicted in Fig. 3, the V_{Qa} signal transitions to a high state when the power MOS feedback signal V_DSfb surpasses the reference voltage VL_in. An analogous operation occurs in MCD2 with the key distinction that V_{Qb} is activated when the V_DSfb signal exceeds both V_Hin and VL_in, and deactivated when it falls below these reference levels.

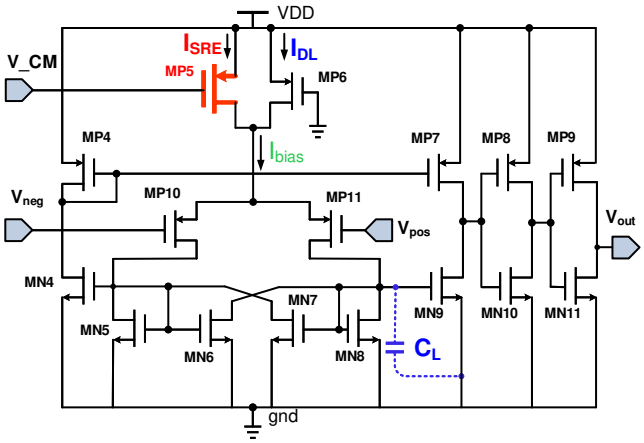

Fig. 4. Modified comparator with V_{CM} control [9], [10]

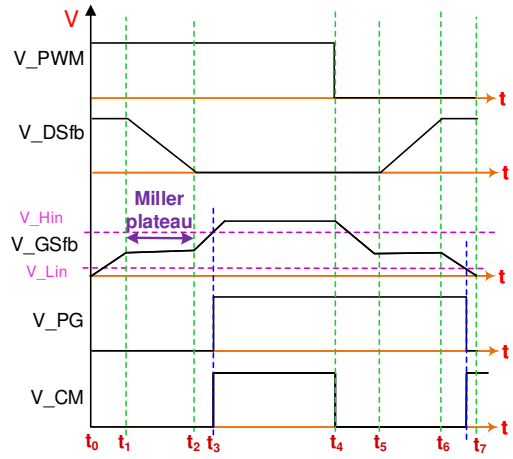

Fig. 5. Current modulation circuit's timing diagram

B. Power gating (PG)

As the name suggests, the Power gating circuit in Figure 2 generates the power gating signal V_PG to reduce redundant static power dissipation in the AGD by shutting off N-1 PMOS devices in the Output Buffer. Based on the output of the comparator pair, C_c and C_d, the SR_c latch produces the V_PG signal through the NOR and AND logic gates. If $\text{V\_GSfb} > (\text{V\_Hin} = 0.8 \times \text{VDD})$, then SR_c latch will be set. If $\text{V\_GSfb} < (\text{V\_Hin} = 0.2 \times \text{VDD})$, then SR_c latch will be reset.

C. Current modulation (CM)

The AGD presented incorporates a novel Current modulation circuit aimed at minimizing the redundant static power that is dissipated by the comparators (C_a, C_b, C_c and C_d). The schematic of these comparators is shown in Fig. 4, specifically designed to reduce static power dissipation without compromising the high slew rate. As indicated in Eqn. (1), the slew rate of the comparator is directly proportional to the bias current [11]. Consequently, to enhance the slew rates, it is necessary to utilize larger bias currents in the design process. The trade-off for this strategy is the rise in static power dissipation. To counteract this effect, the current modulation

TABLE I
BSPS SEQUENCE DATA FOR THE PMOS/NMOS IN OUTPUT STAGE

	$BP_{[0:3]}$, $BN_{[0:3]}$			
Mode	Cycle 1	Cycle 2	Cycle 3	Cycle 4
0	0000, 1111	0000, 1111	0000, 1111	0000, 1111
1	1000, 0111	0100, 1011	0010, 1101	0001, 1110
2	1100, 0011	0110, 1001	0011, 1100	1001, 0110
3	1110, 0001	0111, 1000	1011, 0100	1101, 0010

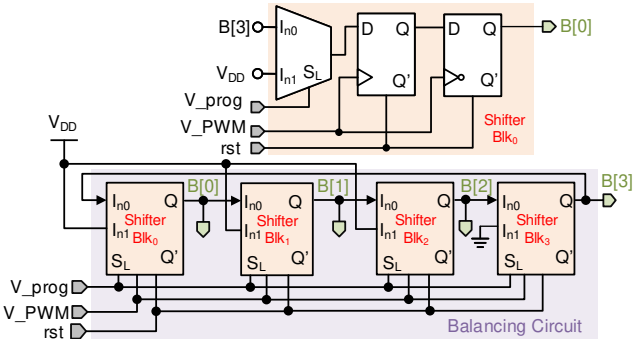

Fig. 6. Balancing circuit schematic

circuit effectively regulates the bias current when there are no transitions occurring in the power MOS waveforms, helping to reduce excess power dissipation.

$$\text{slew rate} = \frac{I_{bias}}{C_L} \tag{1}$$

$$\text{V\_CM} = \overline{(\text{V\_PWM} \oplus \text{V\_PG})} \cdot \text{En} \tag{2}$$

The V_CM signal is produced based on the logic expression shown in Eqn. (2). The XOR gate identifies the transition between V_GS fb and V_PG, marking the occurrence of the Miller plateau. As depicted in Fig. 5, this plateau appears twice in the timing diagram, specifically between the intervals t1-t2 and t5-t6. The V_CM signal is activated only when both V_PG and V_PWM are in the same state, indicating a reduction in the comparator bias current to I_{DL}, with I_{SRE} being turned off via MP5. Given that there are no transitions in the V_DSfb signals, the comparators within the detectors are only required to retain their previous states. The reduced current observed during the t3-t4 period in Fig. 5 leads to a decrease in average power dissipation for the proposed AGD.

D. Balancing circuit

The Balancing Circuit shown in Figure 6 is needed to reduce the impact of mismatches that might occur in the Buffer blocks due to the utilization of the Power Gating Circuit. Since the Power Gating Circuit shuts off N-1 PMOS devices in the Output Buffer, if the same PMOS device is turned off earlier for over several cycles, it leads to a mismatch because some MOS are less utilized than others. This circuit employs V_PWM as the clock signal to generate distinct switch selection sequences for each cycle. This circuit is made up of programmable parallel-in-parallel-out (PIPO) shifter blocks (denoted by Shifter Blk). In the design, the initial load sequence stored in the register during the load phase is hard-wired as B[0:3]=1110.

TABLE II
PERFORMANCE COMPARISON

	[12]	[13]	[14]	[7]	[15]	[16]	This work
Year	2017	2018	2019	2022	2023	2023	2025
Publication	ECCE	JSSC	TPE	ISPSD	MWSCAS	TCAS I	
Technology (nm)	180 HVCMOS	180 BCD	CPLD	180 BCD + FPGA	180 BCD	180 BCD	T18HVG2 (180)
Driver type	Active	Passive	Active	Active	Active	Active	Active
Verification	Meas.	Meas.	Meas.	Meas.	Post Sim.	Meas.	Meas.
VDD (V)	-4 & 15	15	20 & -5	1.8, 3.3 & 20	12	5, -5, 15, 600	5 & 10
f_{V_PWM} (MHz)	0.1	1	9.2	0.1	0.5	N.A.	0.5
t_{rise} (ns)	140 at 15 V	5.6 at 5 V	N.A.	N.A.	153 at 12 V	200	260 at 10 V
t_{fall} (ns)	N.A.	N.A.	N.A.	N.A.	187	250	257 at 10 V
Chip area (mm^2)	5.00	4.9 x 2.3	N.A.	2.5 x 2.5	4.515 x 3.26	4.16	5.26 × 1.05
P_{dis_total}	N.A.	N.A.	N.A.	79.51 mW*	32.7 W	N.A.	568 mW

*Power consumption of FPGA is excluded

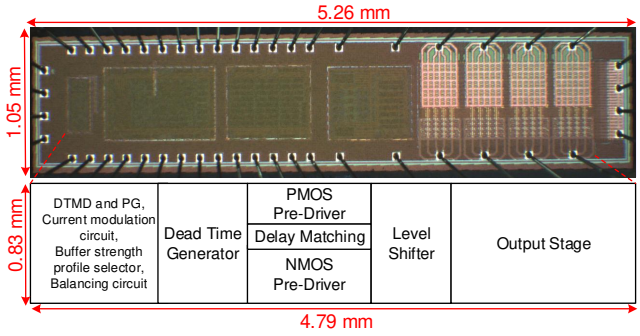

Fig. 7. Die photo and layout of the proposed AGD

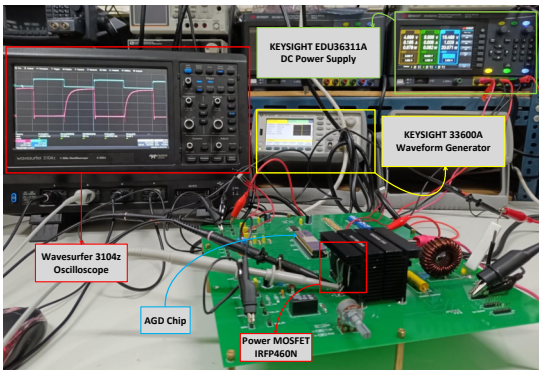

Fig. 8. Measurement setup of the proposed AGD

E. Buffer strength profile selector (BSPS)

The BSPS makes certain that the Level-Shifted PMOS array and Delay Compensated NMOS array in Output Buffer have the appropriate driving currents when the Miller plateau is in effect. A Balancing circuit and a mode decoder are included in the BSPS circuit [8]. The list of sequence data for the buffer arrays is summarized in Table I.

III. MEASUREMENT AND ANALYSIS

The proposed AGD's floorplan, and die photo that was designed and realized utilizing the T18HVG2 process are shown in Fig. 7. The total chip size measures 5.26×1.05 mm^2, while the core area measures 4.79×0.83 mm^2.

Fig. 8 shows the actual measurement setup for the proposed AGD. The Waveform Generator generates V_PWM at 500 kHz frequency, while the DC Power Supply provides clean voltage supply for VDD, VDD_H and VDD_PM. The gate and source pins of the Power MOSFET IRFP460N was coupled

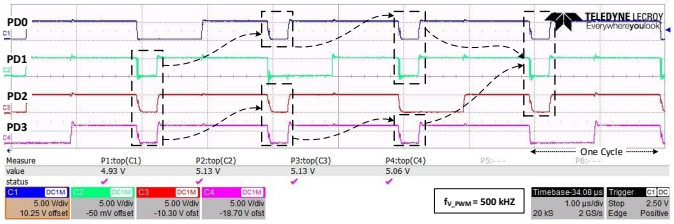

Fig. 9. In Mode 3, the waveforms of PMOS Pre-Driver

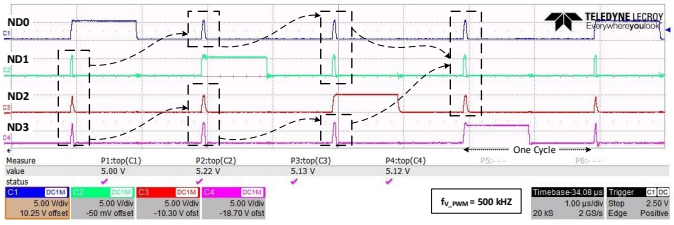

Fig. 10. In Mode 3, the waveforms of NMOS Pre-Driver

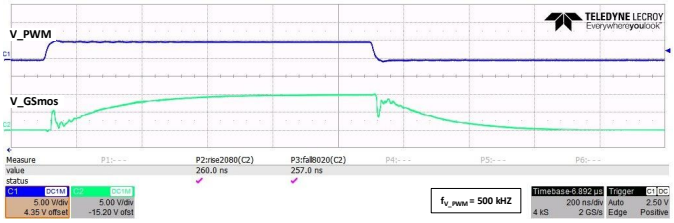

Fig. 11. Generated V_GSmos signal corresponds to a V_PWM input

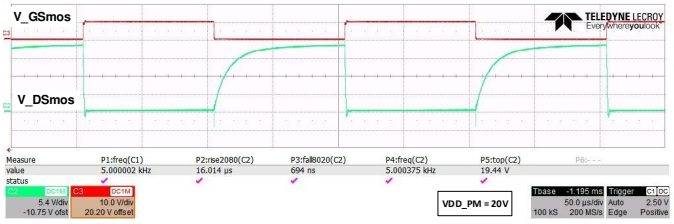

Fig. 12. Generated V_DSmos signal corresponds to V_GSmos

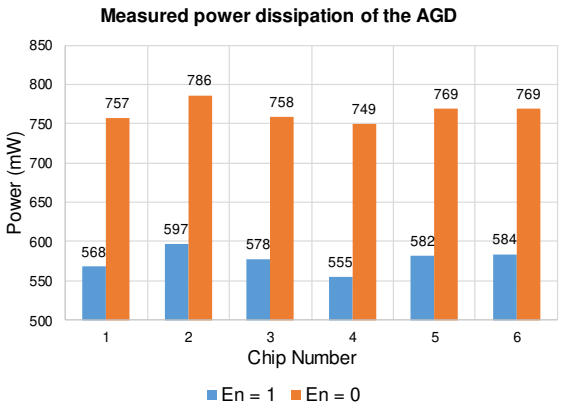

Fig. 13. Graph for the power dissipation of the proposed AGD chip with and without power gating at V_PWM=500 kHz, VDD=5 V, VDD_H=10 V

into the AGD's V_GSfb pin to validate the Miller plateau detection. An inductor (50 μH) was used as the load in the double pulse test.

The timing diagrams of measured PMOS and NMOS Pre-Driver output signals (PD[0:3] and ND[0:3]) are shown in Fig. 9 and 10, respectively at M_1M_0=11 (Mode 3), and En=1 (V_CM enable is on). For enhanced visibility, the shifting sequence is highlighted.

The measurement result shown in Fig. 11, demonstrates when a 5 V, 500 kHz input signal (V_PWM) is applied to the chip, it generates a 10 V V_GSmos signal at En=1 (V_CM enable is on) to drive the Power MOSFET IRFP460N. For a VDD_PM of 20 V, the measurement result in Fig. 12 illustrates the V_GSmos vs V_DSmos characteristics of the Power MOSFET IRFP460N. Fig. 13 shows the measured power dissipation (P_dis) for the 6 AGD chips. It can be observed that, the proposed AGD achieves a 23.7%∼25.9% power reduction when En=1 (V_CM enable is on)

The comparison of the prior works for power transistor drivers is summarized in Table II. The proposed AGD is designed in a compact area (5.26 $\times$ 1.05 mm^2), which is 50.9% and 11.6% smaller than the core areas of [13] and [7], respectively. The proposed AGD design implements all the necessary circuits on a single die, unlike [7], which uses FPGAs to operate. Lastly, the t_{rise} and t_{fall} values for this occurrence are 260 ns and 257 ns, respectively. Though the measured t_{rise} is slower compared to some ultra-fast designs [13], which reports a 5.6 ns, those prior results are based on low-capacitance GaN systems with significantly smaller gate charge (Q_g). In contrast, our design targets SiC MOSFETs which inherently possess a much larger Q_g.

IV. Conclusion

A power-effective AGD design on silicon for power transistors is realized using the T18HVG2 process. Its differential timing-based Miller detector with power-gating method is capable of properly identifying the Miller plateau by using the V_GSmos and V_DSmos of the Power MOSFET. The AGD with the power gating system achieves a notable power reduction of 24.9%, highlighting its efficacy in enhancing the driver's efficiency.

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