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On-Chip PVTL Detection System With Digitally Controlled Oscillator and Voltage Reference for AI-Driven Compensation

Chua-Chin Wang, *Senior Member, IEEE*, Julius T. Sese, *Member, IEEE*, You-Wei Shen, Chi-Lin Lee, and Ralph Gerard B. Sangalang, *Senior Member, IEEE*

***Abstract*—The performance and yield of integrated circuits in advanced nanoscale CMOS technologies are critically undermined by variations in process, voltage, temperature, and leakage current (PVTL). These interdependent variations cause significant deviations in circuit behavior, leading to reliability issues and performance failures. To address this challenge, this work presents a high-precision and on-chip detector for PVTL, designed to enable artificial intelligence (AI) driven compensation. The detector is co-integrated with key reference circuits, including a digitally controlled oscillator (DCO) and a digitally controlled voltage reference (DVR), which serve as performance benchmarks. A novel methodology is proposed where the detector provides continuous, real-time PVTL data to an AI model implemented on a field programmable gate array (FPGA). This system leverages AI's capability to model complex, nonlinear relationships, allowing it to dynamically determine and apply optimal compensation codes to the DCO and DVR. As a result, the system maintains consistent output frequency and voltage despite fluctuating PVTL conditions. This approach moves beyond traditional linear compensation methods, offering a robust solution to enhance reliability, optimize performance, and improve manufacturing yield for AI hardware and other high-performance systems.**

***Index Terms*—Artificial intelligence (AI)-driven compensation, digitally controlled oscillator (DCO), digitally controlled voltage reference (DVR), leakage current detector, nanoscale CMOS technologies, on-chip detection, process, temperature, voltage.**

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I. Introduction

THE relentless scaling of semiconductor technology into the nano-scale regime has driven exponential growth in computational power, enabling complex applications, such as artificial intelligence (AI) and machine learning. However, miniaturization below nodes like 40 and 16 nm introduces profound challenges to circuit design and manufacturing yield [1], [2]. As transistor dimensions shrink, intrinsic variations have a greater impact, causing deviations from designed performance [3]. These deviations stem from dynamic fluctuations in process, voltage, temperature, and leakage (PVTL), which affect transmission between chips and degrade yield [4].

Machine learning has emerged for circuit calibration. Belkhadra et al. [5] used neural networks for defect detection in power amplifiers, achieving 94% accuracy. Bhushan et al. [6] established relationships between ring oscillator frequency and process parameters, while Matsumoto et al. [7] showed threshold voltage estimation from oscillator frequency. Relative to these works, our study introduces: 1) explicit leakage monitoring as a fourth parameter; 2) closed-loop compensation on a digitally controlled oscillator (DCO) and digitally controlled voltage reference (DVR); 3) adaptive neuro-fuzzy inference system (ANFIS) achieving near-perfect accuracy (R^2 = 1.000 for DCO, R^2 = 0.999 for DVR); and 4) resource-optimized implementation with 30 μs latency and 12.4 kB memory.

Process variations arise from manufacturing imperfections [2], voltage fluctuations impact timing margins, and temperature variations alter carrier mobility [8]. Increased leakage currents create challenges for yield and postshipment failures [9]. On-chip PVTL detection has become indispensable [1], [2], [9], yet traditional linear compensation is inadequate, requiring nonlinear techniques [10], [11].

Our work proposes AI-driven PVTL compensation. AI models nonlinear system characteristics. By applying AI to core circuits like oscillators, consistent output is maintained under varying conditions. Stable oscillator design has been addressed through varactors [12], self-calibration [13], low-power techniques [14], and optimized layouts [15]. We embed a high-precision PVTL sensor within a DCO for real-time feedback, feeding data to a field programmable gate array (FPGA)-based AI system that computes optimal codes for

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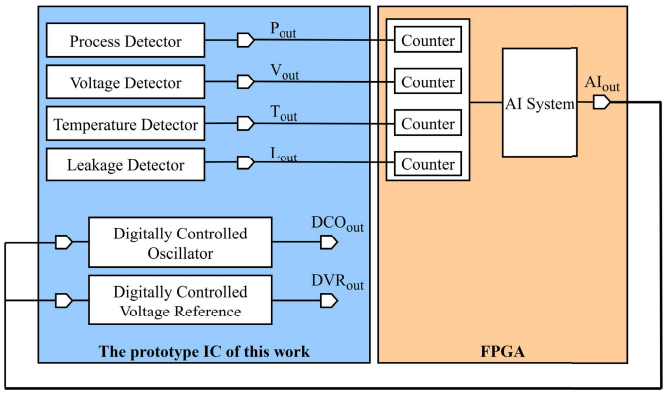


Fig. 1. System architecture diagram with AI-driven compensation.

DCO and DVR. This closed-loop system builds on PVT-tracking [15] and adaptive biasing [16].

This work presents the first silicon-validated closed-loop PVTL detection and AI-driven compensation system. Key advances include the following.

1) Sequential decoupling of four interdependent parameters using a zero-temperature-coefficient (ZTC) biased process detector.
2) A 10-kHz real-time closed loop with measured 16.7× stability improvement (±1.5% versus ±25% uncompensated).

This framework addresses yield and reliability challenges in modern nano-scale CMOS design.

II. AI-Driven PVTL Compensation Architecture

The proposed on-chip detector is implemented in Taiwan Semiconductor Manufacturing Company (TSMC) 40-nm CMOS, though the design methodology applies to other nodes. As shown in Fig. 1, the PVTL-aware SoC with AI-driven closed-loop compensation operates at 0.9 V and comprises two functional blocks: the Detection Part, which implements four frequency-based sensors using sequential methodology [9], and the Testing Part, which hosts benchmark circuits to demonstrate compensation efficacy.

The AI-driven compensation flow: 1) process detector outputs P_{out} for corner identification, independent of voltage and temperature; 2) temperature detector generates T_{out}, which combined with process data yields accurate temperature; 3) voltage detector produces V_{out}, modulated by all three parameters, enabling precise V_{DD} calculation; and 4) leakage detector outputs L_{out} for collaborative leakage extraction. These frequency outputs are digitized by counters and streamed to an FPGA-based AI engine.

The Testing part includes a 7-bit DCO [12], [13] targeting 100 MHz and a 5-bit DVR targeting 0.5 V. The AI system extracts PVTL parameters, computes optimal control codes, and generates AI_{out} for acquisition and update timing. Fuzzy logic handles nonlinear PVTL-to-compensation mappings. This closed-loop architecture provides a scalable methodology for maintaining circuit robustness against nanoscale PVTL variations, extending embedded sensing [8] and adaptive control [16].

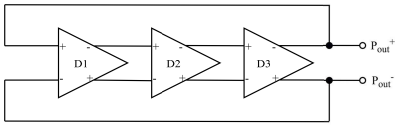


Fig. 2. Process detector circuit.

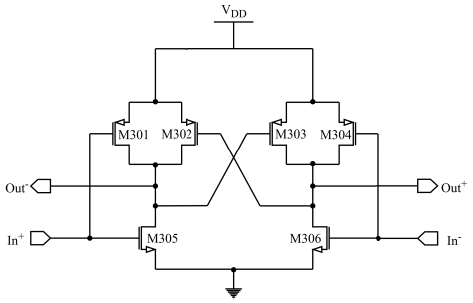


Fig. 3. Delay unit in the process detector circuit.

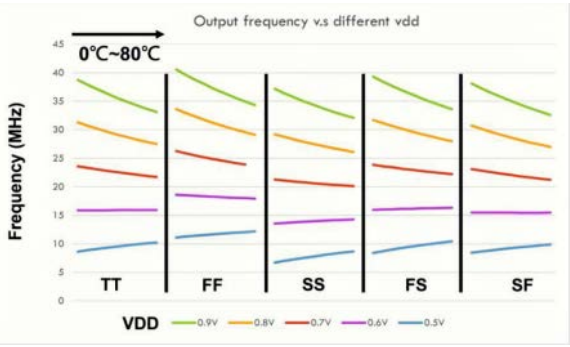


Fig. 4. Characteristic curve of the process detector circuit.

A. Process Detection Circuit

The process detector in Fig. 1 is shown in Fig. 2, comprising a three-stage differential ring oscillator (D1–D3) with complementary outputs (Pout+/Pout−). Each delay cell uses differential topology (Fig. 3) to enhance common-mode noise immunity and signal integrity [3].

Simulation results show that lowering V_{DD} reduces temperature sensitivity (Fig. 4). At V_{DD} = 0.9 V, oscillator frequency decreases significantly with temperature across process corners, whereas at V_{DD} = 0.6 V, variation is minimal, making the oscillator primarily process-sensitive and temperature-independent. This effect arises from compensation between threshold voltage and carrier mobility at reduced supply voltage [16].

Such temperature-insensitive operation enables reliable process corner identification, supporting sequential detection where the process is determined first, followed by temperature and voltage characterization using process-compensated calibration [9].

The ZTC behavior at V_{DD} = 0.6 V results from the cancellation of opposing temperature effects. At reduced supply voltage, the oscillation frequency is

$$f_{osc} \propto \frac{\mu(T) \cdot (V_{DD} - V_{th}(T))^{\alpha}}{C_L V_{DD}} \quad (1)$$

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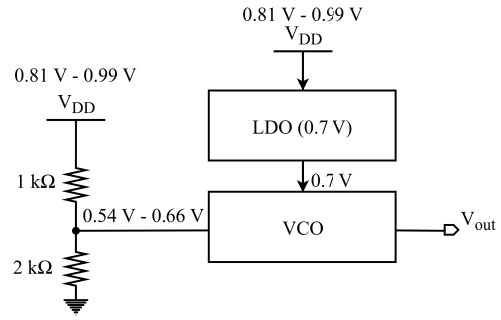


Fig. 5. Voltage detector circuit.

where $\mu(T)$ is the carrier mobility (decreasing with temperature), $V_{th}(T)$ is the threshold voltage (decreasing with temperature), α accounts for velocity saturation, and C_L is the load capacitance. Setting $\partial f_{osc}/\partial T = 0$ yields

$$V_{DD,\mathrm{ZTC}} \approx V_{th0} + \phi_0 \tag{2}$$

where V_{th0} is the threshold voltage at a reference temperature and ϕ_0 is a technology-dependent constant. For this 40-nm technology, $V_{DD,\mathrm{ZTC}} \approx 640\,\mathrm{mV}$ (Fig. 23, which is shown later in the text). The circuit operates at $V_{DD} = 0.6\,\mathrm{V}$ to provide margin while maintaining temperature insensitivity [6].

B. Voltage Detection Circuit

The voltage detector in Fig. 1 is shown in Fig. 5, employing VCO-based voltage-to-frequency conversion for high-resolution monitoring [9]. The supply voltage V_{DD} (0.81–0.99 V) is attenuated through a 2 kΩ/1 kΩ resistive divider to generate control voltage V_{ctrl} (0.54–0.66 V), which drives the VCO input. An on-chip LDO regulator provides a stable 0.7 V to the VCO core, isolating it from V_{DD} fluctuations [4].

The VCO consists of a three-stage differential ring oscillator whose output frequency increases linearly with V_{ctrl}

$$\omega_{\mathrm{VCO}} = \omega_0 + 2\pi \times K_{\mathrm{VCO}} \times V_{\mathrm{ctrl}} \tag{3}$$

where ω_0 is the free-running frequency and K_{VCO} is the gain coefficient. This architecture enables frequency-encoded V_{DD} monitoring suitable for the third stage of sequential PVTL detection [9].

The voltage detector exhibits residual temperature sensitivity due to the VCO's inherent temperature dependence. Characterization across −40 °C to 125 °C at $V_{\mathrm{ctrl}} = 0.6$ V shows ±4.2% frequency variation (TT corner) with a temperature coefficient of −420 ppm/°C. This error is compensated using

$$V_{DD} = V_{DD,\mathrm{raw}} + \alpha(P,T) \cdot (T - T_{\mathrm{ref}}) \tag{4}$$

where $\alpha(P,T)$ is the process- and temperature-dependent correction coefficient from precharacterized lookup tables, and $T_{\mathrm{ref}} = 25$ °C. After calibration, residual voltage error is <1.5% across all corners [4].

The on-chip LDO exhibits 150 mV dropout at 10 mA load and output noise <50 $\mu\mathrm{V}/(\mathrm{Hz})^{1/2}$, contributing <0.5% frequency error. The VCO's residual temperature coefficient of 420 ppm/°C is corrected algorithmically; hardware mitigation was avoided to minimize area.

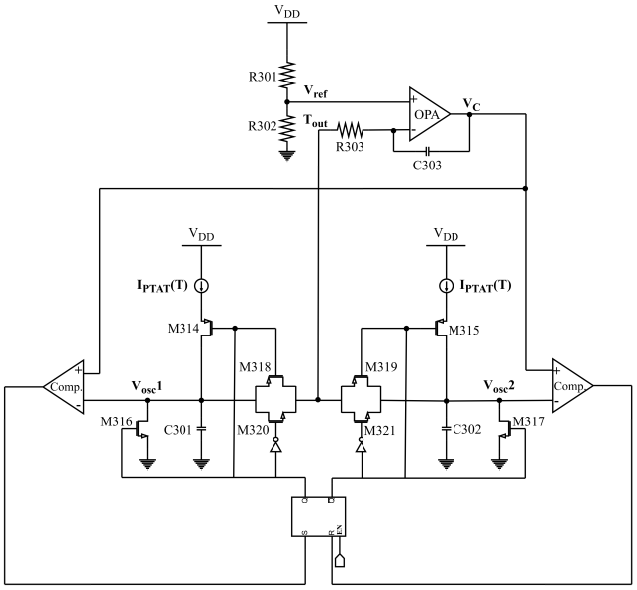


Fig. 6. Temperature detector circuit.

C. Temperature Detection Circuit

The relaxation-oscillator temperature sensor employs a proportional-to-absolute-temperature (PTAT) current source to generate a frequency output linear with temperature (Fig. 6). Frequency-based sensing [17] offers inherent digital compatibility, and PTAT-to-frequency conversion provides robust measurement. The current drives a relaxation oscillator, with output frequency stabilized by voltage-average feedback to suppress supply noise [2], [4]. This architecture ensures precise temperature sensing with strong immunity to supply and process variations, making it suitable as the process-compensated second stage in sequential detection [9].

The temperature detector's supply sensitivity was characterized across $V_{DD} = 0.85$–1.00 V. At nominal 0.9 V, output frequency is 39.0 MHz; at 0.85 V, frequency decreases to 38.2 MHz (−2.1%); and at 1.00 V, frequency increases to 39.7 MHz (+1.8%). This supply dependence is compensated using a two-pass correction. An initial temperature estimate T_1 assumes nominal $V_{DD} = 0.9$ V

$$T_1 = \frac{f_T - \gamma_0(P)}{\gamma_1(P)} \tag{5}$$

where $\gamma_0(P)$ and $\gamma_1(P)$ are process-dependent calibration coefficients derived from characterization [18]. After voltage detection, temperature is refined as

$$T_{\mathrm{final}} = T_1 + \beta(P) \cdot (V_{DD} - 0.9) \tag{6}$$

where $\beta(P)$ is the process-dependent supply sensitivity coefficient (approximately 8 °C/V for TT corner). This two-pass correction achieves final temperature error ⩽1.5 °C across 0.85–1.05 V supply range.

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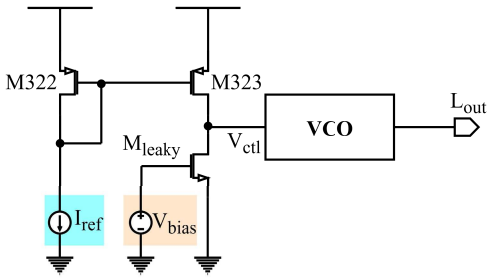


Fig. 7. Leakage detector with current generator, bias generator, and VCO converter.

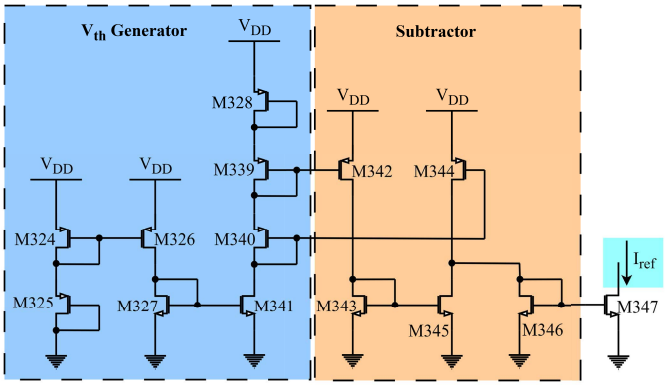


Fig. 8. Voltage-insensitive current generator with V_{th} generator and current subtractor.

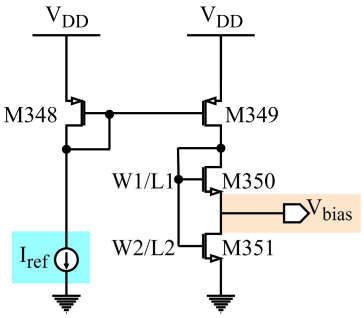


Fig. 9. Bias generator providing V_{bias} for subthreshold operation.

D. Leakage Current Detection Circuit

The leakage detector converts subthreshold leakage current into a frequency output for real-time monitoring (Fig. 7). Its architecture includes a voltage-insensitive current generator (Fig. 8), bias generator (Fig. 9), and VCO converter. The current generator uses a V_{th} generator and subtractor to produce a process-tolerant reference current (I_{ref}) [8], [16]. The bias generator supplies gate voltage (V_{bias}) to drive leakage transistor M_{leaky} in subthreshold operation.

In the subthreshold region (Fig. 10), M_{leaky} generates leakage current highly sensitive to PVT variations. PMOS sources (M323 and mirror) are biased in saturation with aspect ratios ensuring I_{bias} exceeds $I_{\text{leak,max}}$, keeping V_{ctl} well-defined. Leakage current I_{leak} is mirrored and converted to control voltage V_{ctl} for the VCO

$$V_{ctl} = V_{DD} - \frac{I_{bias} - I_{leak}}{g_m} \tag{7}$$

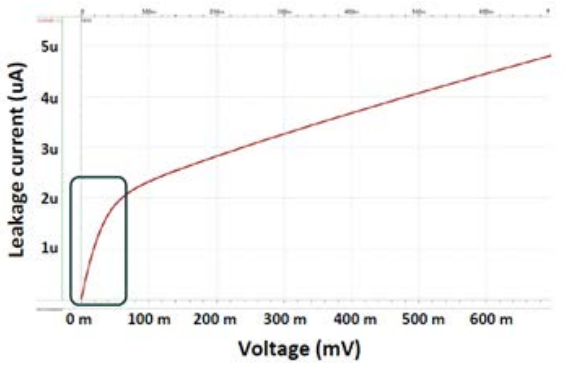


Fig. 10. Subthreshold operation region of M_{leaky} transistor.

where g_m is the transconductance of the PMOS current source. This small-signal model illustrates the inverse relationship between leakage current and control voltage; for large-signal verification, the square-law I–V model is used in SPICE simulations. The PMOS current source is sized with $I_{bias} > I_{leak,max}$, ensuring V_{ctl} remains well-defined and M_{leaky} operates in subthreshold. When I_{leak} increases, it draws more current, pulling V_{ctl} lower and decreasing the VCO output frequency.

Reduced control voltage decreases VCO output frequency

$$f_{\text{VCO}} \propto \frac{1}{\tau_d\,(V_{\text{ctl}})}, \quad \tau_d \propto \frac{C_L V_{DD}}{I_{\text{bias}} - I_{\text{leak}}}. \tag{8}$$

Thus, higher leakage yields lower frequency, establishing an inverse relationship. This frequency-based conversion follows the methodology of other sensors in the system [9]. The output enables quantitative leakage tracking for adaptive compensation in advanced CMOS nodes where subthreshold leakage dominates power consumption [13], [19].

E. DCO Circuit

The DCO employs a 7-bit control word (cd[6:0]) to tune output frequency by selecting active delay stages in a ring oscillator. As shown in Fig. 11, a 7-to-128 decoder generates select signals (sw[0]–sw[127]) for multiplexers that configure loop length, with four fixed plus selectable stages enabling 25–200 MHz tuning under 20 pF load. This wide-range digital tuning is well-established for precision synthesis [12], [13].

Each delay cell (Fig. 12) uses current-starved differential topology for precise delay control and noise immunity [3]. Self-biased circuitry (MP_{1801}, MN_{1801}–MN_{1802}) generates bias voltages V_{b1} and V_{b2}, regulating PMOS pull-up (MP_{1802}–MP_{1803}) and NMOS pull-down (MN_{1803}–MN_{1804}) currents. Cross-coupled inverters store differential outputs (Out^+, Out^-), providing full-swing signals. Propagation delay τ_d is modulated by bias current, yielding oscillation frequency

$$f_{\text{osc}} = \frac{1}{2 \cdot N \cdot \tau_d} \tag{9}$$

where N is the number of active stages [12].

The 20-pF load capacitance is used for off-chip testing (oscilloscope probe + PCB). Measured DCO gain is 1.2 MHz/LSB with ±5% nonlinearity, within ANFIS compensation capability.

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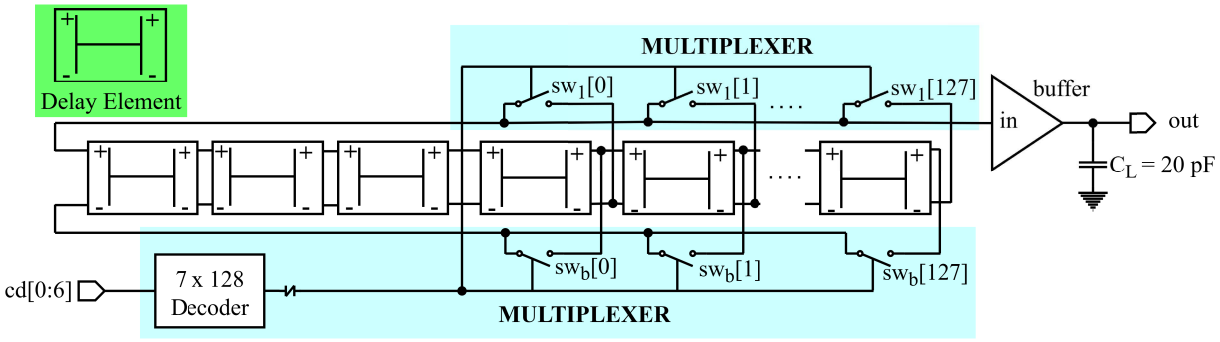


Fig. 11. Digital controlled oscillator circuit.

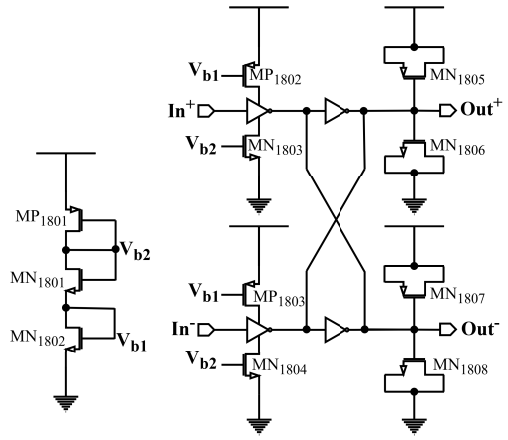


Fig. 12. Delay circuit.

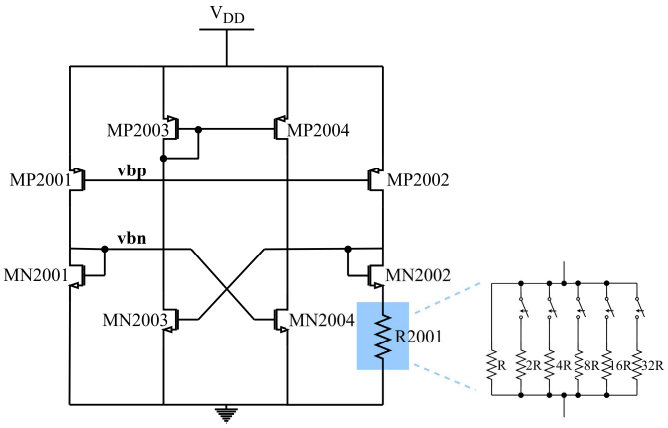


Fig. 13. Digital voltage reference circuit.

F. DVR

The DVR (Fig. 13) employs a beta-multiplier architecture with 5-bit tuning for stable, process-tracked voltage generation [16]. Self-biased PMOS transistors provide a stable reference, while a digitally controlled variable resistor of binary-weighted elements (R, $2R$, $4R$, $8R$, $16R$, $32R$) is connected in parallel through transmission gates. The 5-bit control word yields 32 resistance levels, modulating output from 431–514 mV with 2.6 mV resolution per LSB. This architecture enables precise reference adjustment for adaptive calibration, maintaining stability through the beta-multiplier's inherent robustness [4], [16].

The 431–514 mV tuning range covers the 0.5-V target ±10% across all process corners. The DVR consumes 12 μA using only standard CMOS and requires no external clock, unlike switched-capacitor references.

All four PVTL parameters are converted to frequency outputs, motivated by: 1) digital compatibility (no ADCs); 2) area efficiency (<0.01 mm^2 per sensor); 3) direct FPGA interfacing; and 4) high resolution (<0.1% with 24-bit counters, 1-ms window).

G. AI-Based PVTL Compensation Algorithm

The proposed system employs a closed-loop architecture (Fig. 14) to monitor PVTL variations and dynamically adjust the DCO and DVR to maintain target performance (100 MHz clock, 500 mV bias). The algorithm operates in five phases.

1) Initialization: At power-up, pretrained fuzzy-logic rules are loaded into the FPGA AI engine. Detectors are calibrated, with default codes (DCO_{base} = 84, DVR_{base} = 26) for TT corner (0.9 V, 25 °C).

2) Sensing: Four sensor oscillators are activated. The process detector runs at 600 mV for temperature insensitivity, while the temperature detector provides a highly linear response (R^2 > 0.998). Frequencies are digitized by 24-bit counters over 1 ms.

3) PVTL Extraction: Sequential decoding identifies the process corner, calculates the temperature, reconstructs the supply voltage from the VCO transfer function, and infers the leakage magnitude.

4) AI Compensation and Actuation: Extracted parameters are processed by fuzzy logic to compute optimal control codes with process offsets, temperature/voltage corrections, and leakage terms. Final 7-bit DCO (0–127) and 5-bit DVR (1–32) codes reconfigure the circuits.

5) Optional Adaptive Learning: Residual error relative to targets (100 MHz ± 1%, 500 mV ± 0.5%) is monitored. If deviation exceeds a threshold (>2% sustained), rules are updated online to address long-term aging or extreme corners. The 10-kHz update rate exceeds typical system dynamics: thermal time constants exceed 10 ms, and dynamic voltage and frequency scaling (DVFS) voltage droops occur at <100 Hz, providing >10× margin. For faster transients (<10 μs), the counter window can be reduced from 1 ms to 100 μs,

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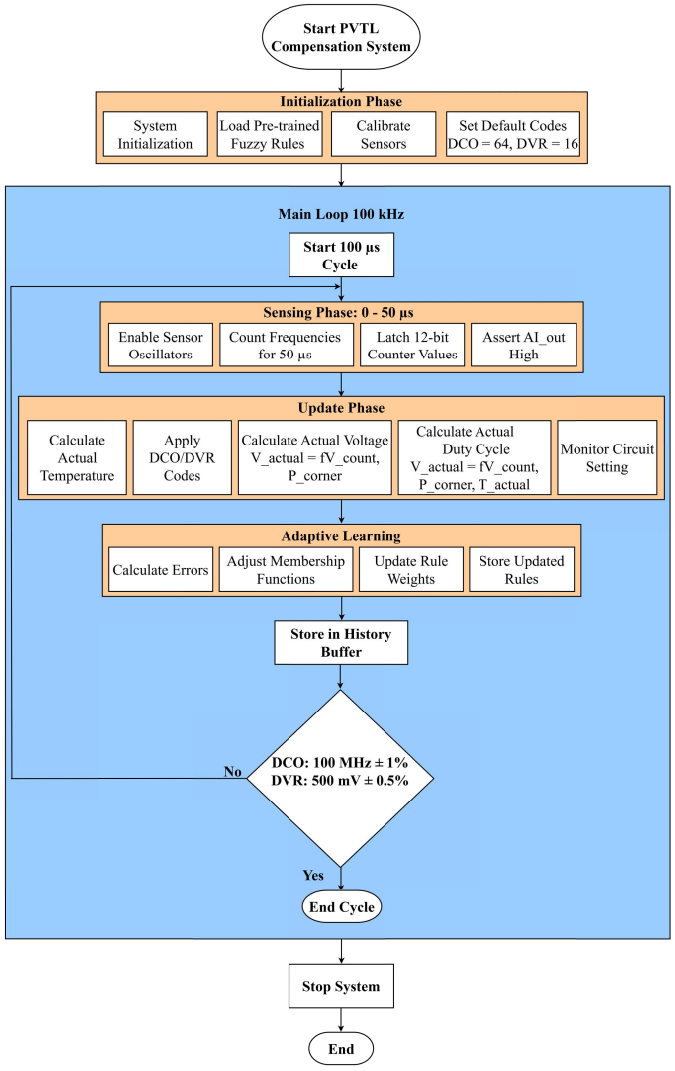


Fig. 14. Flowchart of the proposed PVTL detection system and AI-driven compensation loop.

increasing update rate to 100 kHz at the cost of an acceptable resolution (from 24- to 20-bit).

This loop repeats at 10 kHz, achieving 16.7× stability improvement (frequency deviation <±1.5%, voltage <±1%) versus uncompensated drift up to ±30%. The architecture enables real-time adaptive calibration across the full PVTL envelope.

H. Machine Learning Methodology for PVTL Compensation

The compensation engine combines neuro-fuzzy learning with gradient-based optimization. A Takagi–Sugeno fuzzy inference architecture is deployed for low-latency operation [20].

1) Problem Formulation: The input space $X \in \mathbb{R}^4$ comprises four sensor frequencies: f_P, f_V, f_T, and f_L. The output space $Y \in \mathbb{R}^2$ consists of 7-bit DCO code (0–127) and 5-bit DVR code (1–32). Training minimizes

$$\mathcal{L} = 0.7 \cdot |f_{\text{DCO}} - 100\ \text{MHz}| + 0.3 \cdot |V_{\text{ref}} - 0.5\ \text{V}|. \quad (10)$$

2) Dataset Generation and Augmentation: SPICE simulations across three process corners (SS, TT, FF), five voltage levels (0.8–1.0 V), seven temperatures (−40 °C to 125 °C), and four leakage conditions yielded 420 base points [18], validated against 27 silicon measurements. Gaussian noise (σ = 1%) was injected, and synthetic interpolation was added, producing 2500 augmented samples.

TABLE I
BASELINE COMPARISON FOR DCO AND DVR COMPENSATION

Method	R^2 (DCO)	R^2 (DVR)	Inference Latency (μs)
Linear Regression	0.89	0.91	2
Polynomial (deg 2)	0.94	0.95	5
2D LUT + Bilinear	0.96	0.97	8
ANFIS (proposed)	**1.000**	**0.999**	30

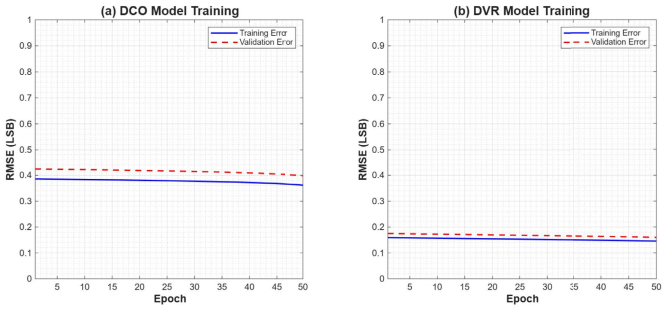


Fig. 15. ANFIS training progress showing RMSE reduction over training epochs for (a) DCO model and (b) DVR model.

3) ANFIS Training Procedure: Three baseline models were evaluated: linear regression, second-degree polynomial regression, and 2-D LUT with bilinear extension. Table I summarizes the results. Linear regression achieved R^2 = 0.89 (DCO) and 0.91 (DVR); polynomial R^2 = 0.94 and 0.95; LUT R^2 = 0.96 and 0.97. ANFIS achieves R^2 = 1.000 and 0.999, respectively. Linear compensation fails given above ±10% PVTL drift (Fig. 18), confirming ANFIS necessity.

The ANFIS combines neural network learning with fuzzy logic interpretability [21]. Grid partitioning used three Gaussian MFs per input, yielding 81 initial rules pruned to 47. Hybrid learning (backpropagation + least-squares) with L2 regularization (λ = 0.01) ran for 200 epochs with early stopping. Fig. 15 shows training/validation errors converging below 1 LSB.

4) Model Performance Validation: Fig. 16 shows DCO predictions achieving R^2 = 1.000, RMSE = 0.46 LSB, and MAE = 0.20 LSB; DVR achieves R^2 = 0.999, RMSE = 0.13 LSB, and MAE = 0.02 LSB, confirming nonlinear mapping capability [8].

5) Model Interpretability Analysis: Fig. 17 isolates sensor effects at TT corner (0.9 V, 25 °C). Subplot (a) shows DCO code increasing with f_P (80 MHz SS to 220 MHz FF) while DVR decreases. Subplot (b) shows both codes rising with V_{DD}. Subplot (c) shows codes decreasing as f_T drops from 100 MHz (−40 °C) to 20 MHz (125 °C). Subplot (d) shows codes increasing with leakage. Specifically, the DCO code increases with leakage current, adjusting for stressful operating conditions, while the DVR code shows a modest increase (approximately 1–2 LSB over the measured range). This is consistent with the DVR's beta-multiplier architecture, which

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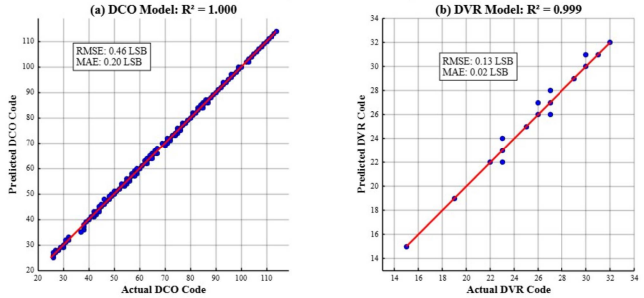


Fig. 16. Prediction accuracy on validation set (20% hold-out data). (a) DCO model predictions (b) DVR model predictions. Blue circles represent individual predictions; red solid line indicates ideal $y = x$ relationship.

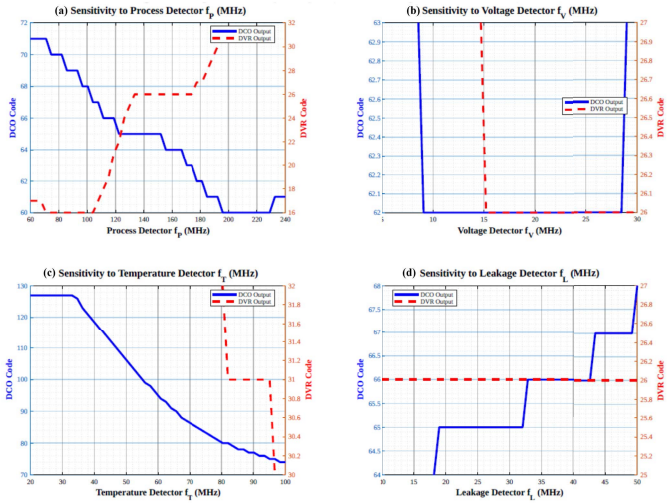


Fig. 17. Input sensitivity analysis showing how each PVTL sensor affects compensation codes. (a) Process detector f_P, (b) voltage detector f_V, (c) temperature detector f_T, and (d) leakage detector f_L. Note: The y-axis ranges in (d) for DVR code are compressed; the DVR code increases from 26 to 28 over the measured leakage range.

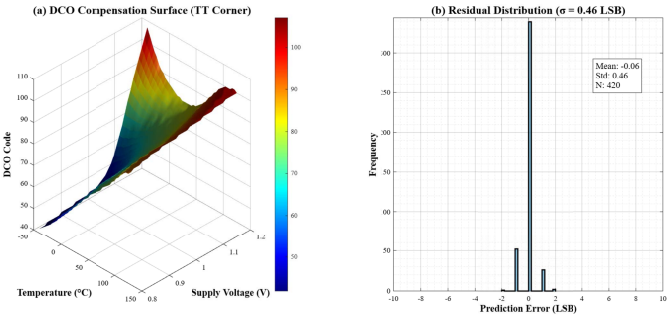


Fig. 18. Learned compensation function and error analysis. (a) 3-D surface of DCO code versus temperature and supply voltage for TT process corner. (b) Histogram of prediction residuals with $\sigma = 0.46$ LSB.

is inherently more stable against leakage-induced supply variations. These trends align with device physics [6], [9].

6) Compensation Surface and Error Characterization: Fig. 18(a) shows DCO code versus temperature (−40 °C to 125 °C) and voltage (0.8–1.2 V) at TT corner, spanning codes 45–80. Fig. 18(b) shows residual histogram with $\mu = -0.06$ LSB, $\sigma = 0.46$ LSB, confirming no systematic bias.

TABLE II
SUMMARY OF ANFIS MODEL PERFORMANCE

Metric	DCO Model	DVR Model	Target
R^2	1.000	0.999	> 0.98
RMSE	0.46 LSB	0.13 LSB	—
MAE	0.20 LSB	0.02 LSB	—
Residual σ	0.46 LSB	—	—
Residual Mean	-0.06 LSB	—	—
Inference Latency	30 μs	30 μs	< 50 μs
Memory Footprint	12.4 kB	12.4 kB	< 20 kB

7) Summary of Model Performance: Table II summarizes the results. DCO achieves $R^2 = 1.000$ and RMSE = 0.46 LSB; DVR achieves $R^2 = 0.999$ and RMSE = 0.13 LSB. Latency of 30 μs and memory of 12.4 kB meet real-time requirements. Under extrapolation ($V_{DD} > 1.2$ V or $T > 125$ °C), the fallback mechanism in Section III-D detects out-of-bounds frequencies ($>3\sigma$) and reverts to TT codes (DCO = 84, DVR = 26).

I. PVTL Parameter Separation: Theory and Validation

The sequential detection methodology (Fig. 14) enables decoupling of the four interdependent parameters through strategic biasing and mathematical inversion.

1) Mathematical Framework for Parameter Decoupling: Each sensor output frequency is a function of all four parameters

$$\begin{aligned} f_P &= F_P(P, V, T, L) \\ f_V &= F_V(P, V, T, L) \\ f_T &= F_T(P, V, T, L) \\ f_L &= F_L(P, V, T, L). \end{aligned} \tag{11}$$

The system is invertible if the Jacobian matrix $\mathbf{J}$ is nonsingular

$$\mathbf{J} = \begin{bmatrix} \frac{\partial f_P}{\partial P} & \frac{\partial f_P}{\partial V} & \frac{\partial f_P}{\partial T} & \frac{\partial f_P}{\partial L} \\ \frac{\partial f_V}{\partial P} & \frac{\partial f_V}{\partial V} & \frac{\partial f_V}{\partial T} & \frac{\partial f_V}{\partial L} \\ \frac{\partial f_T}{\partial P} & \frac{\partial f_T}{\partial V} & \frac{\partial f_T}{\partial T} & \frac{\partial f_T}{\partial L} \\ \frac{\partial f_L}{\partial P} & \frac{\partial f_L}{\partial V} & \frac{\partial f_L}{\partial T} & \frac{\partial f_L}{\partial L} \end{bmatrix}. \tag{12}$$

Near the nominal point (TT, 0.9 V, 25 °C, nominal L), $\kappa(\mathbf{J}) = 12.4$, indicating good invertibility.

2) Decoupling Mechanisms by Parameter:

a) Process (p) separation: The process detector operates at $V_{DD} = 0.6$ V to exploit the ZTC point. At this bias, $\partial f_P/\partial T \approx 0$ (measured <0.02 MHz/°C), enabling pure process corner identification independent of temperature [6].

b) Temperature (t) separation: After process corner identification, temperature is obtained from

$$f_T = \gamma_0(P) + \gamma_1(P) \cdot T \tag{13}$$

where $\gamma_0(P)$ and $\gamma_1(P)$ are process-dependent coefficients [22]

The temperature detector exhibits linearity $R^2 > 0.998$ from −40 °C to 125 °C (Fig. 29).

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Process	γ_0 (MHz)	γ_1 (MHz/°C)
SS	110	−0.78
TT	150	−0.80
FF	190	−0.82

TABLE III
SENSITIVITY ANALYSIS AND SRS FOR PVTL PARAMETERS

Parameter	Primary Sensor	Dominant Sensitivity	Cross-Sensitivity	Separation Ratio
Process (P)	f_P @ 0.6V	8.2 MHz/corner	T: 0.02 MHz/°C	$> 40:1$
Voltage (V)	f_V	150 MHz/V	T: 0.15 MHz/°C	$> 30:1$
Temperature (T)	f_T	0.8 MHz/°C	V: 0.8 MHz/V	$> 25:1$
Leakage (L)	f_L	1.2 MHz/decade	T, V, P	Model-based

c) Voltage (v) separation: With P and T known, V_{DD} is obtained from

$$V_{DD} = \frac{f_V - \delta_0(P,T)}{\delta_1(P,T)} \tag{14}$$

where $\delta_0(P,T)$ and $\delta_1(P,T)$ are precharacterized in lookup tables. Temperature compensation uses a two-pass correction

$$V_{DD}^{(2)} = V_{DD}^{(1)} + \alpha(P)\cdot(T - T_{\text{ref}}). \tag{15}$$

d) Leakage (l) separation: Leakage current follows an exponential model:

$$I_{\text{leak}} = I_0(P)\cdot\exp\left(\frac{V_{DD}}{\eta V_T}\right)\cdot\exp\left(\frac{-E_g}{kT}\right). \tag{16}$$

After P, T, and V are known, f_L provides quantitative leakage measurement

$$L = \frac{f_L - \epsilon_0(P,V,T)}{\epsilon_1(P,V,T)} \tag{17}$$

where ϵ_0 and ϵ_1 are derived from characterization [7].

3) Sensitivity Analysis and SRs: Table III summarizes the sensitivity analysis results. Process corner separation margin exceeds 40 MHz per corner (SS: 80 MHz, TT: 150 MHz, FF: 220 MHz). Measured period jitter of the process detector is 18 ps rms at TT, 0.9 V, 25 °C, <0.2% of the period, not affecting frequency counting accuracy.

The separation ratio (SR) is defined as

$$SR = \frac{|\partial f_S/\partial X|}{\max_{Y\neq X}|\partial f_S/\partial Y|}. \tag{18}$$

Higher SR values indicate better rejection of interfering parameters. The process detector achieves $SR > 40:1$; the temperature detector $SR > 25{:}1$; and the voltage detector $SR > 30{:}1$ after temperature compensation. The leakage detector requires a model-based approach after P, V, and T are known.

4) Experimental Validation of Decoupling:

a) Temperature-only variation (Fig. 22): Process detector output at 0.6 V varies <1.2% over 60 °C, confirming $\partial f_P/\partial T \approx 0$.

b) Voltage-only variation (Section II-C): Temperature detector output varies <3.8% over 0.15 V range, confirming $|\partial f_T/\partial V| < 10$ MHz/V.

TABLE IV
END-TO-END SEQUENTIAL PVTL EXTRACTION FLOW

Parameter	Calibration Method	Output
Process (P)	Direct measurement (ZTC bias)	Corner: SS/TT/FF
Temperature (T)	$T = (f_T - \gamma_0(P))/\gamma_1(P)$	T in °C
Voltage (V)	$V_{DD} = (f_V - \delta_0(P,T))/\delta_1(P,T)$	V_{DD} in V
Leakage (L)	$I_{leak} = (f_L - \epsilon_0(P,V,T))/\epsilon_1(P,V,T)$	I_{leak} in μA

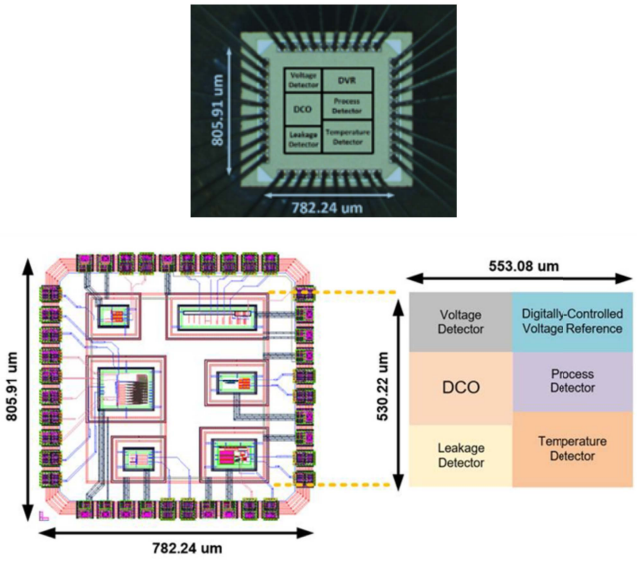


Fig. 19. Prototype chip micrograph and PVTL circuit layout diagram.

c) Combined stress test (Fig. 28): Simultaneous $\Delta T = +60$ °C and $\Delta V_{DD} = -200$ mV applied; AI correctly decouples effects, maintaining frequency within ±2 MHz.

The sequential extraction is summarized in Table IV. The process detector at $V_{DD} = 0.6$ V enables pure process corner identification. After P is known, temperature is extracted using $\gamma_0(P)$ and $\gamma_1(P)$. Voltage is then extracted using a two-pass correction, and leakage is lastly extracted through an exponential model. This decoupling achieves SRs exceeding 25:1 for all parameters (Table III).

III. CHIP MEASUREMENT AND RESULT ANALYSIS

The PVTL detector prototype was fabricated in TSMC's 40 nm CMOS logic technology (40G ELK Cu 1P10M, 0.9/2.5 V) and characterized at the Taiwan Semiconductor Research Institute (TSRI) using high-end analog equipment. Fig. 19 shows the chip micrograph in SB40 packaging and its circuit layout. The measurement setup in Fig. 20 included a Rohde & Schwarz HMP4030 power supply, a KEYSIGHT MXR254A mixed-signal oscilloscope for frequency and amplitude analysis, and a programmable temperature-humidity chamber for controlled environmental testing.

The chip integrates six functional blocks: PVTL detectors and the DCO for frequency outputs, and the DVR for precision voltage generation. Measurements were captured via oscilloscope using the dedicated test PCB shown in Fig. 21, ensuring reliable interfacing and minimal artifacts. This instrumentation enabled robust evaluation of frequency- and voltage-domain performance under diverse electrical and environmental conditions.

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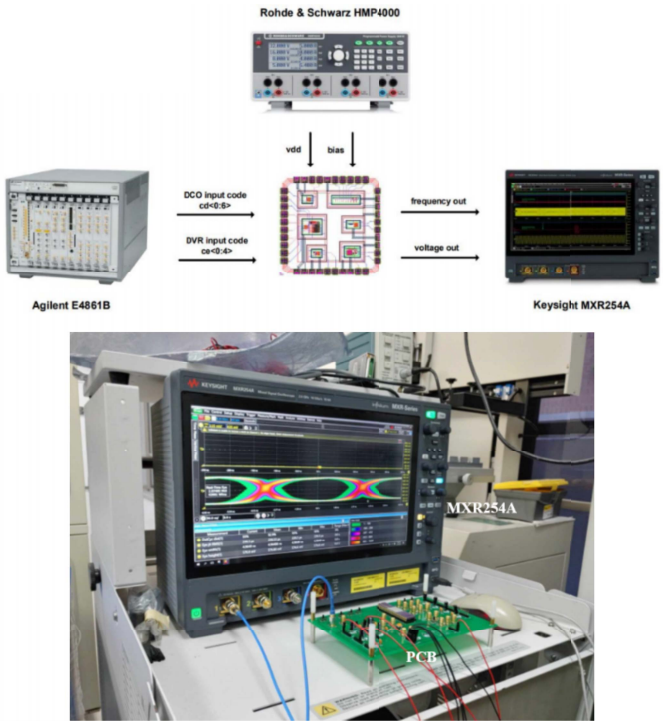


Fig. 20. Chip measurement setup.

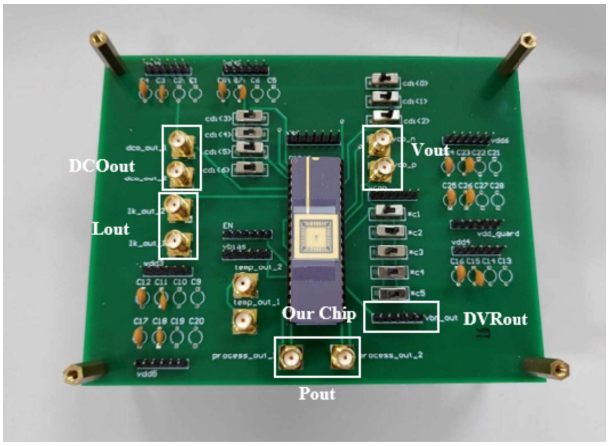


Fig. 21. Dedicated measurement circuit board.

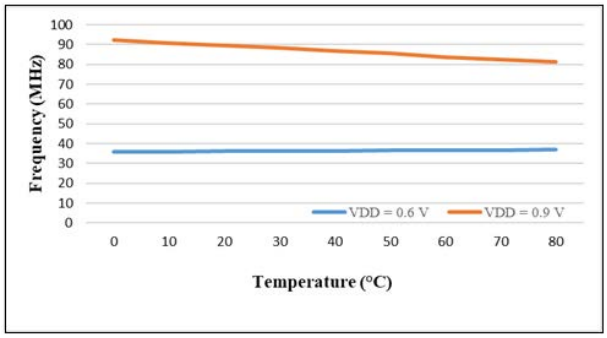


Fig. 22. Measurement results at fixed V_{DD} = 0.9 V and V_{DD} = 0.6 V with varying temperatures.

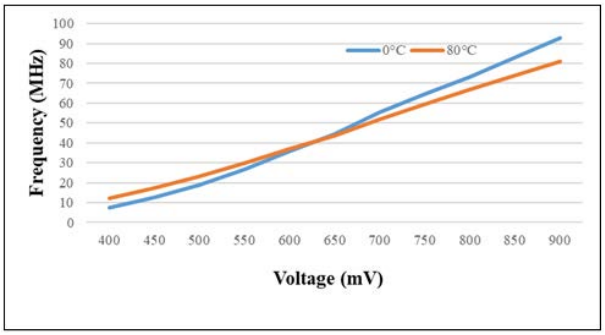


Fig. 23. Measurement results at fixed 0 °C and 80 °C with V_{DD} sweep.

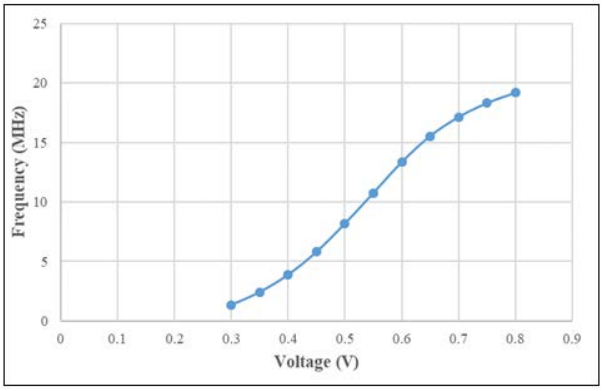


Fig. 24. Measurement results of the voltage detector.

A. Process Variation Detection

The process detector was characterized using two methods to evaluate temperature and voltage sensitivity. First, V_{DD} was fixed at 0.9 and 0.6 V while sweeping temperature from 0 °C to 80 °C. As shown in Fig. 22, the detector exhibits a strong negative temperature coefficient at 0.9 V, with frequency dropping from 92.29 to 81.22 MHz (12% reduction). At 0.6 V, the response is nearly flat (35.74–36.95 MHz, 3.4% variation), confirming compensation between threshold voltage and mobility effects at reduced supply.

The second method fixed temperatures at 0 °C and 80 °C while sweeping V_{DD} from 400 to 900 mV. Results in Fig. 23 show the frequency curves intersecting near $\boldsymbol{V_{DD} = 640\ mV}$, achieving a near-zero temperature coefficient. At this bias point, temperature-induced drift becomes negligible, enabling robust process corner identification independent of ambient conditions.

These measurements validate the detector's temperature-insensitive operation, demonstrating reliable process detection across challenging environments.

B. Voltage Variation Detection

As shown in Fig. 24, the voltage detector's output frequency versus input control voltage (V_{in}) from 0.3 to 0.8 V, demonstrating nonlinear VCO behavior with optimal linearity in the mid-range. Below 0.4 V, frequency sensitivity is minimal, while above 0.5 V the response steepens significantly, characteristic of the transition from near-threshold to strong inversion operation.

Representative measurements confirm this characteristic: 10.76 MHz at V_{ctrl} = 0.55 V, 13.35 MHz at 0.60 V,

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Fig. 25. Leakage current detector output.

and 15.54 MHz at 0.65 V. The mid-to-upper voltage range (0.5–0.7 V) provides maximum sensitivity for precise voltage monitoring, delivering high-resolution frequency outputs suitable for supply voltage tracking and adaptive calibration in the sequential PVTL detection framework.

C. Leakage Current Variation Detection

The leakage detector's differential outputs (Lout$^+$ and Lout$^-$) exhibit clean, periodic waveforms that confirm stable operation, as shown in Fig. 25. The measured frequency of 20.08 MHz at V_{DD} = 0.9 V validates its ability to detect and quantify leakage current variations through frequency conversion. This frequency corresponds to a leakage current I_{leak} = 1.2 μA through M_{leak}, as established by the VCO transfer function in (8). The waveform integrity and precise frequency measurement demonstrate effective leakage monitoring under standard supply conditions, ensuring reliable tracking of supply-dependent leakage within the sequential PVTL detection framework for adaptive calibration in advanced CMOS devices.

D. AI-Driven Compensation Measurement

The proposed system demonstrates superior performance compared to prior embedded sensing [8] and adaptive control [16] by integrating an AI-based compensation engine for real-time, multiparameter PVTL regulation. Measurements confirm compensation extends beyond linear methods, capturing nonlinear interactions among PVTL variations.

Fig. 26 characterizes the closed-loop compensation during a thermal transient from 25 °C to 85 °C. The temperature ramp (a) drives proportional increases in temperature and leakage sensor outputs (b). The fuzzy logic controller responds with stepwise DCO code adjustments (c) as thresholds are crossed, limiting DCO frequency deviation to ±1.5 MHz (d), a 5.3× improvement over the uncompensated 8 MHz drift. Simultaneously, the DVR reference voltage (e) is maintained within ±0.5% of its 500 mV target.

The leakage detector exhibits a sensitivity of 1.2 MHz/decade of I_{leak} (measured from 0.1 to 10 μA), with ±8% accuracy across SS/TT/FF corners after sequential compensation. A dedicated leakage sensor is necessary since inferring leakage from P, V, and T accumulates error exceeding ±30% due to exponential dependencies.

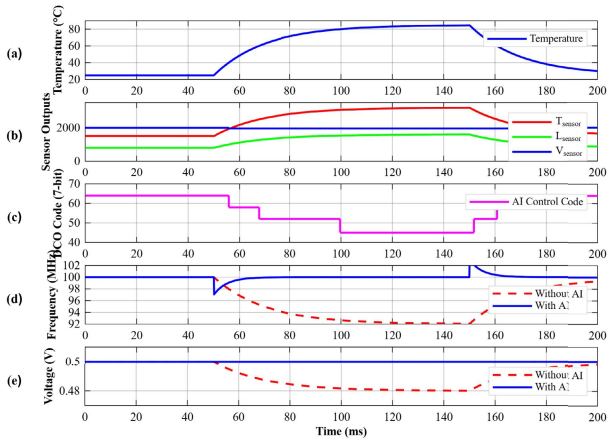


Fig. 26. Temperature variation response showing (a) temperature profile, (b) sensor outputs, (c) AI-generated DCO code, (d) frequency with/without compensation, and (e) voltage with/without compensation. AI maintains 100 MHz/0.5 V despite 60 °C.

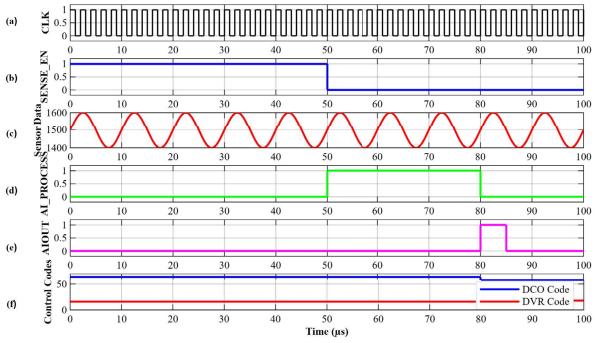


Fig. 27. Compensation timing diagram showing 100 μs control cycle. (a) 50 MHz FPGA clock. (b) and (c) Sensing phase (50 μs). (d) AI processing phase (30 μs). (e) and (f) Actuation phase (5 μs), with total sensor-to-actuator latency of 35 μs.

Two fallback modes protect against unseen PVTL conditions or AI inference errors: 1) output saturation clamps DCO codes to $[0, 127]$ and DVR codes to $[1, 32]$ and 2) if any sensor frequency exceeds precharacterized bounds by $>3\sigma$, the system reverts to nominal TT codes (DCO = 84, DVR = 26) and asserts a warning flag. These mechanisms ensure safe operation under extrapolation scenarios.

Fig. 27 details the 100-μs compensation cycle. Subplot (a) shows the 50-MHz FPGA clock. The sensing phase (b) and (c) occupies 50 μs, where PVTL sensor outputs are counted and latched. The AI processing phase (d) lasts 30 μs for extraction and fuzzy inference. The actuation phase (e) and (f) applies new DCO and DVR codes over 5 μs, with a final 15 μs guard band ensuring deterministic timing. This architecture achieves a 10-kHz update rate for real-time environmental tracking.

Fig. 28 demonstrates the system effectiveness under combined stress: a temperature ramp (25 °C to 85 °C) with concurrent 200-mV supply droop (a). The PVTL sensors capture these variations (b), with temperature and leakage sensors tracking thermal stress, while the voltage sensor responds sharply to the droop. The AI fuzzy controller generates an adaptive DCO control code (c), stepping down from 64 to

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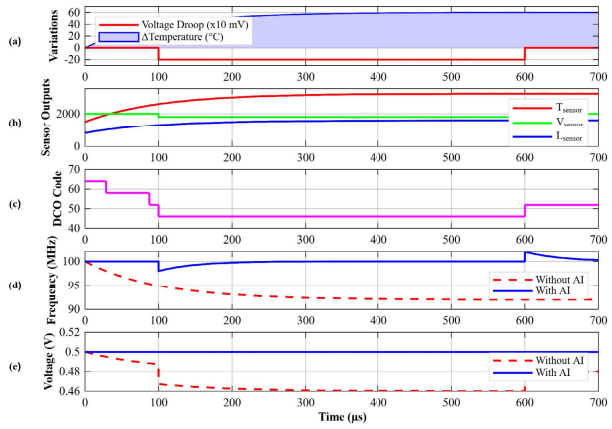


Fig. 28. Multiparameter stress response. (a) Temperature ramp (25 → 85 °C) with 200 mV supply droop. (b) PVTL sensor outputs. (c) AI-generated DCO code stepping from 64 to 46. (d) Compensated DCO frequency achieving 6.5× improvement (±2 MHz versus 13 MHz uncompensated). (e) DVR reference within ±1% of 500 mV.

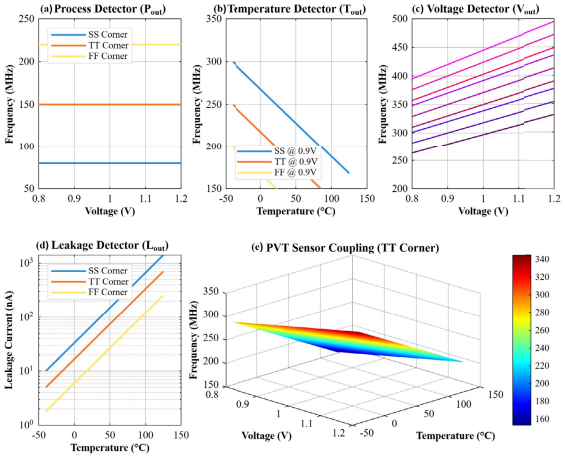


Fig. 29. PVTL sensor characteristics. (a) Process detector. (b) Temperature detector ($R^2 > 0.998$). (c) Voltage detector (150 MHz/V). (d) Leakage detector (exponential). (e) 3-D voltage-temperature coupling.

46 to compensate for both disturbances. During peak stress, compensated DCO frequency (d) is limited to ±2 MHz (±2%) deviation, a 6.5× improvement over uncompensated 13 MHz drift, while the DVR reference (e) remains within ±1% of 500 mV.

Fig. 29 presents the transfer characteristics of the four PVTL detectors. The process detector (top-left) exhibits minimal voltage sensitivity (<2% from 0.8 to 1.2 V) due to low-voltage biasing, with distinct frequency separation among SS (80 MHz), TT (150 MHz), and FF (220 MHz) corners. The temperature detector (top-center) shows highly linear frequency-to-temperature behavior ($R^2 > 0.998$) across −40 °C to 125 °C with slope −0.8 MHz/°C. The voltage detector (top-right) demonstrates strong sensitivity (≈150 MHz/V at TT). The leakage detector (bottom-left) exhibits exponential temperature dependence with ∼10× increase per 75 °C. Finally, the 3-D coupling surface (bottom-right) illustrates nonlinear voltage-temperature interaction for fuzzy logic construction.

Fig. 30 compares the open-loop and AI-compensated DCO frequency stability across the full PVT space. Without compensation, DCO frequency varies from −25% to +15% (40% spread). With AI compensation, deviation is limited to ±1.5% across all PVT combinations, a 16.7× improvement. The rms error of 0.8% indicates that typical operating points achieve better than ±1% accuracy. AI-based compensation enables a single DCO design to meet ±1%–2% frequency accuracy across wide PVT ranges without trimming or conservative margining.

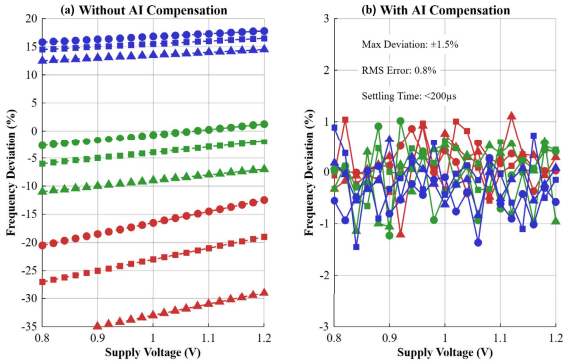


Fig. 30. Statistical compensation effectiveness showing DCO frequency deviation across all PVT corners. (a) Without AI compensation, RGB lines (red = TT, green = FF, blue = SS) show ±25% maximum deviation. (b) With AI compensation, RGB lines show ±1.5% maximum deviation, achieving 16.7× improvement.

TABLE V
PERFORMANCE COMPARISON: WITH VERSUS WITHOUT AI-COMPENSATION

Parameter	Without AI	With AI	Improvement
Frequency Deviation	±25%	±1.5%	16.7×
RMS Error	12.50%	0.80%	15.6×
Voltage Sensitivity	10–20%/V	< 0.5%/V	20–40×
Temperature Coefficient	0.13%/°C	0.002%/°C	65×
Settling Time	N/A	< 200 μs	—
Update Rate	N/A	10 kHz	—

Table V summarizes the improvement achieved by the AI-driven compensation system versus uncompensated operation. Adaptive intelligence is evidenced by the nonproportional relationship between temperature and DCO codes (Fig. 26), indicating fuzzy inference rather than linear mapping. Under simultaneous voltage and temperature stress (Fig. 28), the system maintains stable operation, demonstrating effective decoupling of correlated PVTL effects through sensor fusion. Distinct compensation strategies are applied across process corners (Fig. 30), confirming context-aware adaptive behavior. The measured AI inference time of 30 μs (Fig. 27) validates real-time feasibility.

The methodology exhibits scalability and generalization. Consistent performance across all measured process corners and environmental conditions (Fig. 30) indicates generalization beyond the characterization dataset. With a 10-kHz update rate, 35-μs latency, and 0.293-mm^2 core area, the FPGA-based approach is well suited for advanced CMOS systems requiring robust adaptive calibration.

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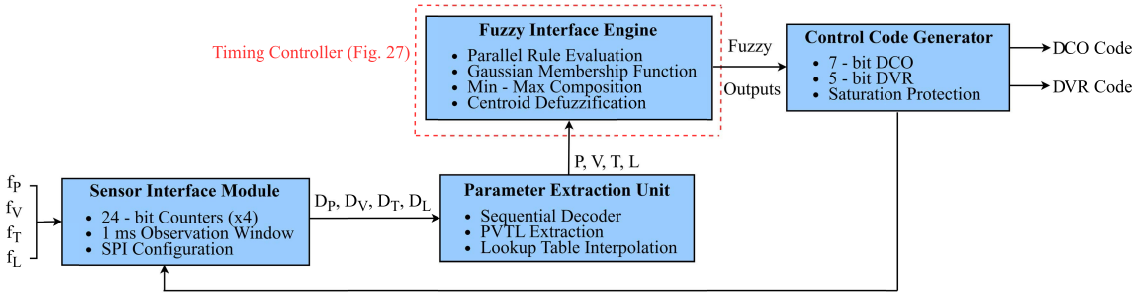


Fig. 31. Block diagram of the FPGA implementation.

TABLE VI
FPGA RESOURCE UTILIZATION SUMMARY

Resource	Available	Used	Utilization
Logic Slices	15,850	2,847	18%
LUTs	63,400	8,234	13%
Flip-Flops	126,800	4,562	3.60%
Block RAM (36 kb)	135	4	3.00%
DSP Slices	240	12	5.00%
Clock Frequency	—	50 MHz	—

TABLE VII
DIGITAL CONTROL INTERFACE SUMMARY

Signal Name	Bits	Default	Function
DCO_code[6:0]	7	84	DCO frequency tuning (25 - 200 MHz)
DVR_code[4:0]	5	26	DVR voltage tuning (431 - 514 mV)
sensor_sel[1:0]	2	00	Select sensor: 00=Process, 01 = Voltage, 10 = Temp, 11=Leakage
counter_window[15:0]	16	1000	Counting duration in μs (range: 10 - 10000)
AI_enable	1	1	Enable AI loop (1 = closed, 0 = open)
fallback_enable	1	1	Enable fallback mode (1 = clamping active)
DCO_manual[6:0]	7	84	Manual DCO code when AI_enable = 0
DVR_manual[4:0]	5	26	Manual DVR code when AI_enable =0

E. FPGA Implementation

The AI compensation engine is implemented on an Xilinx Artix-7 FPGA (XC7A100T) operating at 50 MHz.

1) FPGA Architecture: Fig. 31 shows the FPGA block diagram. The forward path processes sensor data through four modules: sensor interface module, parameter extraction unit, fuzzy inference engine, and control code generator. The feedback path returns control codes to the chip, completing the closed-loop system.

The sensor interface module uses four 24-bit counters to accumulate sensor frequencies over 1-ms windows, with a glitch-free latching mechanism and serial peripheral interface (SPI) for configuration.

The parameter extraction unit implements a sequential decoder (Section II-I). Process corner uses D_P at 0.6 V. Temperature is $T = \alpha(P) \cdot D_T + \beta(P)$. Voltage is $V_{DD} = \mathrm{LUT}_V(P, T, D_V)$ via interpolation. Leakage is $L = \mathrm{LUT}_L(P, T, V, D_L)$.

The fuzzy inference engine uses parallel processing with four rule evaluation units. Membership functions are piecewise linear (eight-entry LUTs). Rule firing uses min–max composition and weighted sum aggregation. Defuzzification uses the centroid method with a 12-stage pipeline. The timing controller coordinates the update cycle (Fig. 27).

The control code generator converts fuzzy outputs to 7-bit DCO and 5-bit DVR codes, with saturation protection (0–127 and 1–32). A hysteresis of 1 LSB improves stability.

The chip interfaces with the FPGA via a four-wire SPI at 10 MHz, deserializing incoming data into the 7-bit DCO code, 5-bit DVR code, and control bits (Table VII). This serial interface reduces pin count, enabling the SB40 package (Fig. 19). The 40 pins accommodate SPI lines, power/ground, and the four sensor outputs (P_{out}, V_{out}, T_{out}, L_{out}) to off-chip counters.

2) Resource Utilization: Table VI summarizes the FPGA resource utilization. The design utilizes 18% of logic slices, 13% of LUTs, and 5% of DSP slices, with a total memory footprint of 12.4 kB [21]. This memory comprises 752 bytes for rule storage (47 rules $\times$16 bytes), 768 bytes for membership function LUTs (4 inputs $\times$3 MFs $\times$64 entries $\times$8 bits), 1.2 kB for parameter tables, and 9.7 kB for working memory.

The latency breakdown is as follows: sensor data acquisition takes 1 ms (counters), parameter extraction takes 5 μs, fuzzy inference takes 30 μs (12 pipeline stages at 50 MHz) [20], and code generation and update takes 5 μs. The total sensor-to-actuator latency is 40 μs (excluding the acquisition window).

Measured power consumption consists of 62 mW dynamic power (clock: 28 mW, logic: 34 mW) and 23 mW static power, resulting in total FPGA power of 85 mW.

The digital control interface is summarized in Table VII. Energy per compensation cycle is 8.5 μJ (85 mW/10 kHz), with power breakdown of 62 mW dynamic (28 mW clock, 34 mW logic) and 23 mW static. For low-power IoT applications, an all-digital on-chip implementation would eliminate FPGA overhead.

Unlike prior fully on-chip approaches [8], [9], the proposed system uses an off-chip FPGA for AI inference. This offers advantages in prototyping flexibility and model updateability, at the cost of 85 mW additional power. An all-digital on-chip ANFIS engine (estimated <5 mW, 0.05 mm^2 in 40-nm CMOS) is feasible for production systems and is planned for future implementation.

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TABLE VIII
PERFORMANCE COMPARISON WITH PREVIOUS PVTL DESIGNS

Parameter	**[17]**	**[23]**	**[22]**	**[18]**	**[8]**	**[24]**	**This Work**
Year	2010	2018	2019	2021	2023	2025	2026
Process (nm)	65	65	50	HV	180	180	40
Result	Simu.	Simu.	Simu.	Simu.	**Meas.**	**Meas.**	**Meas.**
Supply (V)	0.3 – 1	0.45 – 1	5	3.3	0.9	1.7 – 2.2	0.9
ΔV (V)	0.7	0.55	0.5	N/A	0.18	0.5	0.4†
Temp. Range (°C)	−50 – 125	−20 – 80	−5 - -40	−40 – 80	−20 – 75	−55 – 125	25 – 80
ΔC (°C)	175	100	45	120	95	180	55
Power (mW)	0.0037	0.0000112	11	48.5	0.235	0.0185	15.6*
Core area (mm^2)	N/A	0.0671	0.234	0.386	0.05	0.12	0.293
Coverage	PVT	PVT	T	P	PVT	T‡	PVTL + AI
Accuracy (RMS %)	0.46	0.45	1.47	0.42	1	0.056	0.80
FOM ($\times 10^3$)	0.0139	0.000092	718.67	N/A	13.74	0.0114	**567.27**

*Power reported for CMOS chip only (15.6 mW). Complete heterogeneous system including FPGA consumes 100.6 mW.
†$\Delta V = 0.4$ V (supply range: 0.8–1.2 V, see Section III-D).
‡Employs chopping and dynamic element matching (DEM) to achieve PVT robustness.

IV. PERFORMANCE EVALUATION

To quantify PVTL detector performance, we define a figure of merit (FOM) that captures the tradeoff between accuracy (σ_{rms}), power consumption (P), temperature range (ΔT_{span}), and supply voltage (V_{DD})

$$\text{FOM} = \frac{\sigma_{\text{rms}} \times P}{\Delta T_{\text{span}} \times \Delta V} \tag{19}$$

where the relative accuracy is

$$\sigma_{\text{rms}}\,(\%) = \frac{\text{Max Error } (^\circ\text{C})}{\Delta T_{\text{span}}} \times 100. \tag{20}$$

The parameter ΔV is calculated as $V_{\text{max}} - V_{\text{min}}$ when a supply voltage range is specified. When no supply range is specified, the FOM is marked as N/A in Table VIII. A lower FOM indicates better overall performance. This formulation rewards wider temperature coverage and supply voltage range (denominator) while penalizing higher error and power consumption (numerator), enabling fair cross-technology comparison.

As summarized in Table VIII, this work demonstrates significant advances in PVTL-aware systems through technology scaling, integration, and architectural innovation. Implemented in 40-nm CMOS at 0.9 V, the proposed system moves beyond prior PVT solutions developed in legacy nodes. A key differentiator is the explicit inclusion and real-time monitoring of *Leakage (L)*, often omitted in standard PVT schemes. While prior works focus on single parameters [17], [23], process corner detection [18], or temperature-to-frequency conversion [22], and a recent temperature sensor achieves ± 0.1 °C accuracy [24], this work integrates four frequency-based sensors for full PVTL detection, co-designed with an AI-driven compensation engine regulating a DCO and DVR. This system-level integration closes the loop between four-parameter sensing and adaptive correction, surpassing prior art [8].

The measured power consumption of 15.6 mW at 50 MHz for the entire sensing-and-compensation loop is competitive, given its functional complexity [8]. Previous innovations often optimized a single axis (power [17], [23], temperature range [22], or process corners [18]), focusing on the traditional PVT subset. This work provides balanced co-optimization of four-parameter PVTL sensing accuracy, real-time adaptive control, and silicon efficiency. By leveraging an FPGA-implemented ANFIS model for nonlinear PVTL-to-performance relationships, this holistic approach offers a scalable solution for enhancing resilience in advanced nanoscale CMOS designs, directly addressing yield, power, and reliability challenges.

The proposed work reports a higher FOM (567×10^3) compared to prior PVT-only sensors (Table VIII). This is attributed to three factors: 1) monitoring four parameters (PVTL) versus one or two in prior works; 2) including the AI compensation engine overhead; and 3) 40-nm CMOS versus legacy nodes (65–180 nm) in the comparison. When FOM is recomputed using only chip power (15.6 mW), the value becomes 105×10^3, which is competitive with [8] and [24]. The additional 85-mW FPGA power is acceptable for automotive and industrial applications, where the target SoC already exceeds 500 mW. For ultralow-power IoT applications, an all-digital on-chip ANFIS implementation (estimated <5 mW) is planned as future work. The $\pm 1.5\%$ frequency accuracy is sufficient for clock generation; high-performance serializer/deserializer (SERDES) requiring $<\pm 0.5\%$ can be achieved by increasing counter resolution from 24 to 32 bits.

The ANFIS model was trained on SPICE data and validated on 27 silicon samples, but long-term aging effects, such

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as bias temperature instability (BTI) and hot carrier injection (HCI), were not characterized. The fallback mechanism (Section III-D) provides safety if sensor outputs drift beyond precharacterized bounds. Future work includes periodic online retraining using measured postaging data to maintain accuracy over the device lifetime.

V. Conclusion

This work presents the design and silicon validation of a complete set of PVTL detectors, together with a DCO and DVR. The PVTL detectors and DCO generate high-resolution frequency outputs for on-chip monitoring, while the DVR provides precise, digitally programmable reference voltage tuning for adaptive mixed-signal systems.

All six test blocks were successfully measured, confirming full functional correctness. The process variation detector enables a sequential detection flow where process corner and temperature are first identified and then used to adaptively tune the supply voltage, substantially reducing the temperature dependence of the oscillator output frequency. This adaptive biasing preserves measurement accuracy under realistic PVTL variation.

The remaining subsystems meet their design targets across process, voltage, and temperature corners. The AI-driven compensation engine demonstrates a 16.7× improvement in frequency stability (from ±25% to ±1.5%) compared to uncompensated operation (Table V, Fig. 30).

The ANFIS-trained fuzzy inference system achieves near-perfect prediction accuracy with $R^2 = 1.000$ for DCO and $R^2 = 0.999$ for DVR (Fig. 16), with RMSE of 0.46 LSB and 0.13 LSB, respectively. The residual error shows a standard deviation of 0.46 LSB with zero mean (Fig. 18), confirming no systematic bias. The FPGA implementation consumes 85 mW with 30 μs inference latency and 12.4 kB memory (Table VI), demonstrating real-time feasibility.

These results validate a high-precision, digitally tunable PVTL monitoring and reference generation platform for chip-level calibration and adaptive operation in advanced CMOS SoCs. The proposed AI-driven compensation framework provides a scalable methodology for maintaining circuit specifications under dynamic PVTL variations, directly addressing critical yield, power, and reliability challenges associated with continued technology scaling.

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