A 3-MHz All-NMOS Adaptive Active Gate Driver With Dual-Buffer Architecture and Detection-Free CSIV Spike Suppression for SiC MOSFETs

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***Abstract*—This paper presents the on-chip all-NMOS adaptive active gate driver (ANA-AGD) for high-speed, high-voltage SiC MOSFET applications. A dual-floating dual-buffer architecture enables inherent suppression of Common Source Inductance Voltage (CSIV)-induced oscillations without auxiliary sensing circuits. By forming two floating source-buffer paths with distinct frequency responses, the architecture generates a transient voltage difference in response to high-frequency CSIV components, enabling implicit spike discrimination without explicit sensing circuits. An active float bridge (AFB) is introduced to ensure reliable signal transmission across floating domains, preventing signal distortion and device overstress under high-voltage operation. In addition, an adaptive drive strength (ADS) structure dynamically regulates the gate-driving current through a frequency-dependent mechanism, limiting excessive current during fast transients while enhancing drive capability during the Miller plateau region. The proposed driver is fabricated using TSMC 0.18 μm CMOS HV BCD (T18HVG2) process. Measurements validate operation from 1 kHz to 3 MHz while driving a 1.2-kV SiC MOSFET. The proposed driver achieves a rise time below 25 ns at 500 kHz and an average power consumption of 58 mW. Compared to a widely-used commercial gate driver, the overshoot rate is significantly reduced from 47.3% to 1.4%, confirming effective suppression of CSIV-induced oscillations. These results demonstrate that the proposed ANA-AGD provides a compact, power-efficient, and high-speed solution for robust SiC MOSFET gate driving without requiring explicit sensing circuitry.**

***Index Terms*—All-NMOS, ANA-AGD, SiC MOSFET, floating systems, Boost-Damp Buffer, active float bridge, CSIV, drive-strength.**

I. Introduction

THE increasing global demand for high-efficiency power conversion systems has driven continuous innovation in power semiconductor technologies. In particular, the emergence of third-generation wide-bandgap (WBG) semiconductors, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), has transformed modern power electronics [1], [2]. SiC MOSFETs, in particular, exhibit key advantages including higher critical breakdown voltage, lower on-resistance, faster switching speed, and superior high-temperature performance compared with conventional silicon-based devices. These features make SiC power devices particularly suitable for high-voltage, high-frequency, and high-temperature applications such as electric vehicles (EV), renewable energy conversion, and industrial motor drives [3], [4].

Although the intrinsic material properties of SiC enable high-speed operation, they also introduce serious circuit-level challenges. Owing to their extremely fast switching transitions, SiC MOSFETs are highly susceptible to parasitic effects, especially the Common Source Inductance Voltage (CSIV) spike, which arises from the parasitic inductance between the power device and its gate driver (GD) [5], [6]. These high di/dt and dv/dt transients lead to oscillations, voltage overshoots, and electromagnetic interference (EMI), degrading system efficiency, increasing switching losses, and compromising device reliability [7], [8], [9]. Moreover, the CSIV spike can induce false turn-on or gate ringing, which may result in catastrophic device failure if not properly controlled. Therefore, designing a gate driver capable of fast and stable switching while suppressing oscillation and voltage stress has become a critical focus in SiC power systems.

Traditional power discrete gate drivers typically use an open-loop control with bulky passive components, lacking active feedback and the ability to adapt to voltage and temperature variations [10]. While some active gate drivers (AGDs) integrate a feedback through external programmable devices (e.g., FPGAs, microcontrollers), this approach increases system size, cost, and power consumption, and requires reprogramming for different power devices [11], [12]. Most AGDs

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employ a complementary PMOS–NMOS output stage, which provides robust functionality and stable operation. However, the relatively low hole mobility of PMOS—approximately one-third that of NMOS—imposes a fundamental limitation on the switching speed and drive strength of the output stage. This limitation becomes critical when driving SiC MOSFETs that require fast gate charge and discharge transitions to fully exploit their high-speed characteristics. Furthermore, the conventional PMOS–NMOS topology struggles to manage parasitic oscillations effectively, as the asymmetric drive capability between pull-up and pull-down paths causes imbalanced switching transients [9], [13], [14], [15], [16], [17], [18].

To mitigate these problems, researchers have proposed several strategies. Some gate driver designs adopt multi-level gate control or negative voltage generation schemes to shape the gate voltage waveform, thereby reducing overshoot and oscillation. For example, a gate driver implemented using an internal inductor and charge pump to achieve three-level voltage control, which enhances switching speed but increases circuit complexity and power consumption [19]. Hung et al. presented a high CMTI GaN-on-SOI driver with quad-drive control, capable of driving 1700-V SiC switches, yet the design did not specifically address CSIV-induced oscillation [20]. Xiang et al. proposed an active gate driver using Rogowski coils for feedback-based control, achieving fast response but requiring external magnetic sensors [21]. Similarly, Cao et al. developed an integrated driver with adaptive multi-level control, capable of responding quickly to voltage and current changes, though its reliance on parasitic inductance as a sensing element introduces sensitivity to EMI [22].

Despite these advances, most existing approaches share common drawbacks: they rely on sensing circuits [23], complex multi-stage feedback [24], or additional FPGA or digital processors to control AGD [25], all of which increase design cost, chip area, and delay. Moreover, these methods often struggle to maintain stability under high dv/dt conditions or to operate efficiently in compact Integrated Circuit (IC) implementations. Consequently, there remains a strong demand for a simpler, more power-efficient gate driver architecture that provides both fast switching capability and inherent oscillation suppression without requiring extra sensing or feedback modules.

To address these challenges, this paper presents a novel all-NMOS adaptive active gate driver (ANA-AGD) architecture that leverages a dual-floating dual-buffer system to achieve high-speed operation and self-regulated oscillation suppression. Unlike conventional designs that depend on PMOS–NMOS output stages, the proposed driver employs NMOS transistors as the Output Stage: a Main Source Buffer for primary gate driving and a Boost-Damp (B–D) Source Buffer for transient control. The key innovation lies in the use of separate floating ground systems for each buffer, enabling differential detection of CSIV spikes through passive circuit responses. Specifically, the two buffer systems form distinct low-pass filters (LPF_M and $LPF_{B\text{-}D}$) via resistors with different impedance values. When a CSIV spike occurs, the voltage difference between the two floating systems naturally exceeds a threshold, activating the B–D buffer to counteract oscillations. This mechanism enables automatic, detection-free suppression of parasitic oscillations while maintaining fast switching transitions.

To facilitate stable operation under floating conditions, the proposed design integrates an Active float bridge (AFB) circuit, which safely transmits control signals across different ground domains without voltage overstress or signal distortion. The AFB uses push–pull mechanisms and feedback diodes to ensure complete signal transfer and automatic recovery, effectively resolving the challenge of control communication across floating potentials. Furthermore, a Hanging Buffer structure isolates the Main and B–D buffer control systems, allowing voltage differentials to form during transients while protecting devices from overvoltage. This configuration ensures that the B–D buffer can respond rapidly to CSIV events without interfering with the main driving loop.

Another important feature of this work is the incorporation of an adaptive drive strength (ADS) control mechanism that dynamically adjusts the gate driving current according to the switching phase. By forming low-pass feedback loops through resistors R_enh and R_dec, the driver suppresses excessive charging or discharging currents during high di/dt transitions and enhances drive strength during the Miller plateau region. This negative feedback-based adaptive control not only improves switching speed and efficiency but also minimizes oscillation energy and EMI. Simulation results demonstrate that the driver automatically balances between strong and weak driving modes, delivering optimal gate control under various switching conditions. Compared to prior designs, the proposed gate driver achieves several key improvements:

1) All-NMOS Output Structure: Utilizes high carrier mobility of NMOS transistors for superior speed and efficiency while eliminating the limitations of PMOS pull-up paths.
2) Dual-Floating Dual-Buffer System: Provides intrinsic detection and suppression of CSIV spikes without external sensing circuits.
3) Active float bridge: Enables safe and complete signal transmission across floating systems under high-voltage conditions.
4) Adaptive Drive Strength: Dynamically adjusts drive force to optimize switching behavior and reduce EMI.
5) Simplified Implementation: Achieves high-speed, low-power operation with reduced circuit complexity and area overhead.

II. ALL-NMOS ADAPTIVE ACTIVE GATE DRIVER

The architecture of the proposed all-NMOS adaptive active gate driver (ANA-AGD) is shown in Fig. 1. The Output Stage comprises a Main Source Buffer Array and a Sink Buffer Array, which respectively control the turn-on and turn-off transitions of the SiC MOSFET. To suppress parasitic oscillations that occur during fast switching, especially at the gate-source node of the SiC MOSFET, a Boost-Damp (B-D) Source Buffer with a control circuit is introduced.

The B-D Source Buffer shares the same output node as the Main Source Buffer Array, but it is connected via a different low-pass filter path with lower impedance. This difference in

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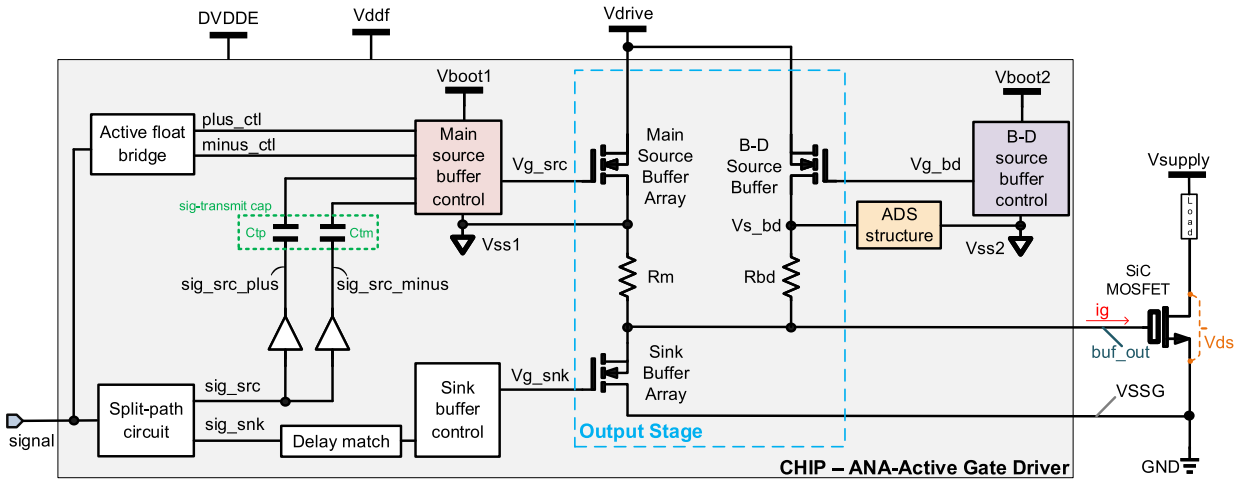


Fig. 1. Proposed architecture of all-NMOS adaptive active gate driver (ANA-AGD).

impedance allows the circuit to detect high-frequency spikes without additional detection circuits. Control of these buffers is managed through several specialized sub-circuits, such as Main source buffer control, the Sink buffer control, and the Active float bridge. This architecture also includes several pre-existing circuits such as the Split-path circuit and Delay match [9], [26], [27].

The ANA-AGD is partitioned into functional blocks optimized for adaptive high-voltage driving of SiC MOSFETs. These blocks and their associated sub-blocks are summarized as follows.

A. **Main Source Buffer Array:** It is the pull-up network responsible for turning on the SiC MOSFET.

1) Main source buffer control (MSBC)–It is a control circuit used to regulate the switching behavior of the Main Source Buffer Array.
2) Active float bridge (AFB)–This circuit generates the two signals, 'plus_ctl' and 'minus_ctl', for the Main Source Buffer Control.

B. **Sink Buffer Array:** It is the pull-down network responsible for turning off the SiC MOSFET.

1) Sink buffer control–It is a control circuit used to manage the operation of the Sink Buffer Array.
2) Split-path circuit and Delay match – These two circuits contains a chain of matched inverters used to ensure proper delay alignment.

C. **B–D Source Buffer:** It is an auxiliary network used to suppress parasitic oscillations in the system.

1) B–D Source Buffer Control - It is a control circuit to regulate the behavior of the B–D Source Buffer.
2) Adaptive Drive Strength (ADS) Structure - It implements an optimal driving mechanism during high-current transmission and during the Miller plateau.

The Main Source Buffer Array and the B–D Source Buffer form distinct low-pass filters with the resistors Rm and Rbd, respectively. By exploiting the differential frequency responses of these filters, CSIV spike events are inherently detected and used to trigger oscillation suppression, without auxiliary detection circuits.

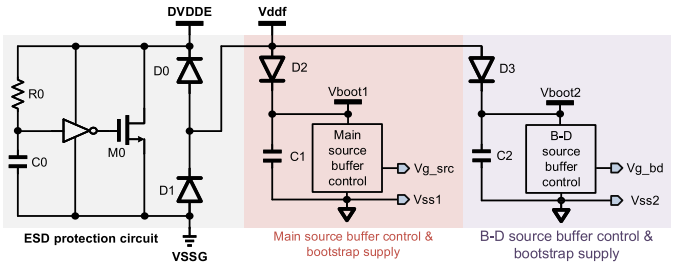


Fig. 2. Illustration of the power supply network.

The external supply voltages to the chip are DVVDE, Vddf and Vdrive which are 5 V, 5 V and 12 V, respectively, while VSSG serves as global ground for the chip. Vdrive is the power supply for the Output Stage of the ANA-AGD. Vboot1 and Vss1 form floating power system 1 for the Main source buffer control and for the AFB, while Vboot2 and Vss2 form floating power system 2 for the B-D source buffer control. Vboot1, Vss1, Vboot2, Vss2 are generated internally within the chip. Vsupply and GND are power supplies for the external SiC MOSFET. Vsupply is varied from 30 V to 1.2 kV. The simplified illustration of these power supplies is shown in Fig. 2. D2 and D3 serve as bootstrap diodes, while C1 and C2 serve as bootstrap capacitors.

As shown in Fig. 3, the floating supply rails Vboot1 and Vboot2 follow the corresponding floating source potentials, varying from 5 V to 17 V, while the floating grounds Vss1 and Vss2 vary from 0 V to 12 V. The external control signal, signal, serves as the input to the proposed ANA-AGD and operates with a logic swing of 0–5 V. The Main Source Buffer Control directly receives this low-voltage logic input and generates the floating control signal Vg_src, which swings from 0 V to 17 V to drive the Main Source Buffer Array. The complete ANA-AGD generates the gate-driving output buf_out with a voltage swing of 0–12 V. Unlike conventional adaptive gate drivers that rely on dedicated level shifters [9], [14], [15], [16], [17], [18], [23], the proposed

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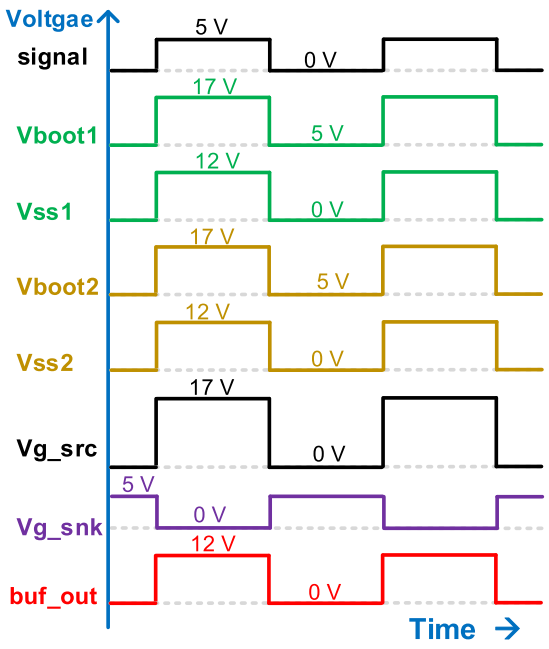


Fig. 3. Voltage-level illustration of the nodes in the proposed ANA-AGD.

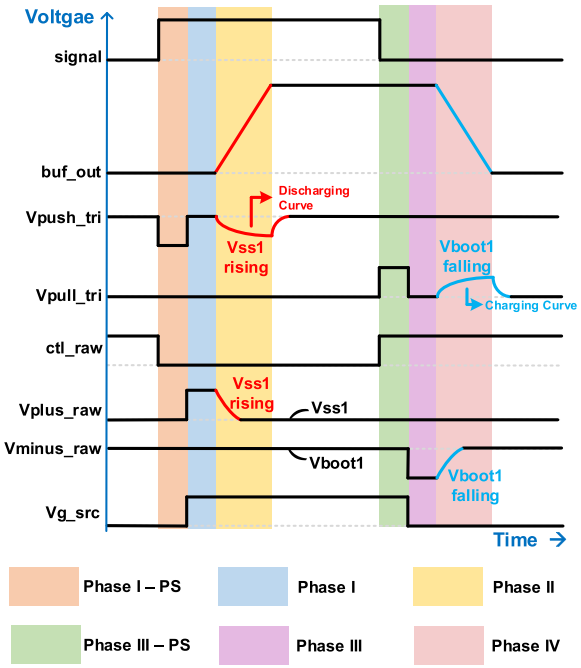


Fig. 4. Overall operating sequence of the AFB and MSBC.

ANA-AGD directly interfaces with a 5-V logic input, eliminating the level shifter and reducing circuit complexity, and power consumption.

A. Main Source Buffer Array

The Main Source Buffer Array is an NMOS pull-up network that drives the SiC MOSFET gate to a high level. This design leverages the characteristics of high-side NMOS devices with negative-feedback control to detect and process the CSIV spikes and to regulate gate voltage during the Miller plateau transition.

Fig. 4 illustrates the overall operating sequence of the AFB and MSBC, showing the input to the ANA-AGD (signal), the AFB trigger signals (Vpush_tri and Vpull_tri), the AFB internal node (ctl_raw), the MSBC voltage nodes (Vplus_raw and Vminus_raw), and the MSBC output (Vg_src). Since the AFB output control signals, plus_ctl and minus_ctl, are simply buffered versions of ctl_raw, they are omitted from the timing diagram for clarity. The coordinated operation of the AFB and MSBC is divided into six phases: Phase I–PS, Phase I, Phase II, Phase III–PS, Phase III, and Phase IV.

During the turn-on sequence of the SiC MOSFET, the AFB first presets the control signals in Phase I–PS, after which the preset state is released in Phase I to trigger the MSBC, thereby generating Vg_src to activate the Main Source Buffer Array. During Phase II, the floating system potential rises together with buf_out, while Vplus_raw and Vminus_raw track the floating potential to maintain the proper bias conditions of the MSBC. Similarly, during the turn-off sequence of the SiC MOSFET, the AFB presets the control signals in Phase III–PS before releasing the preset state in Phase III to deactivate the Main Source Buffer Array through Vg_src. During Phase IV, the floating system potential returns to its initial level, while Vplus_raw and Vminus_raw continue to track the

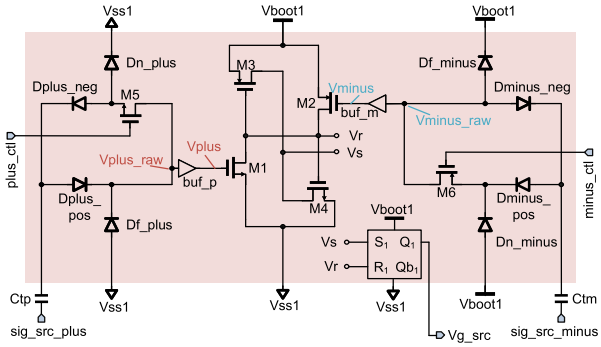


Fig. 5. Schematic of main source buffer control (MSBC).

floating potential to maintain the proper bias conditions of the MSBC. The detailed operations of the AFB and the MSBC corresponding to each phase are described in the following subsections.

1) Main Source Buffer Control (MSBC): Gate drivers with a buffer composed of high-side and low-side NMOS as the final stages are relatively difficult to control, as they cause the system to enter a floating state and create a floating ground. Since the proposed buffer exhibits similar characteristics to a high-side NMOS buffer, a floating-ground system is adopted in the control circuitry, as shown in Fig. 5. Vboot1 and Vss1 denote the floating supply and ground of the MSBC, respectively. Their potential difference is regulated to 5 V.

As illustrated in Fig. 4, the turn-on operation begins when the input to the ANA-AGD, signal, transitions to a high level at the beginning of Phase I–PS. During this preset phase, the AFB establishes the required initial condition for the turn-on operation. In Phase I, the preset state is released, generating the trigger signals for the MSBC. Consequently, both sig_src_plus and

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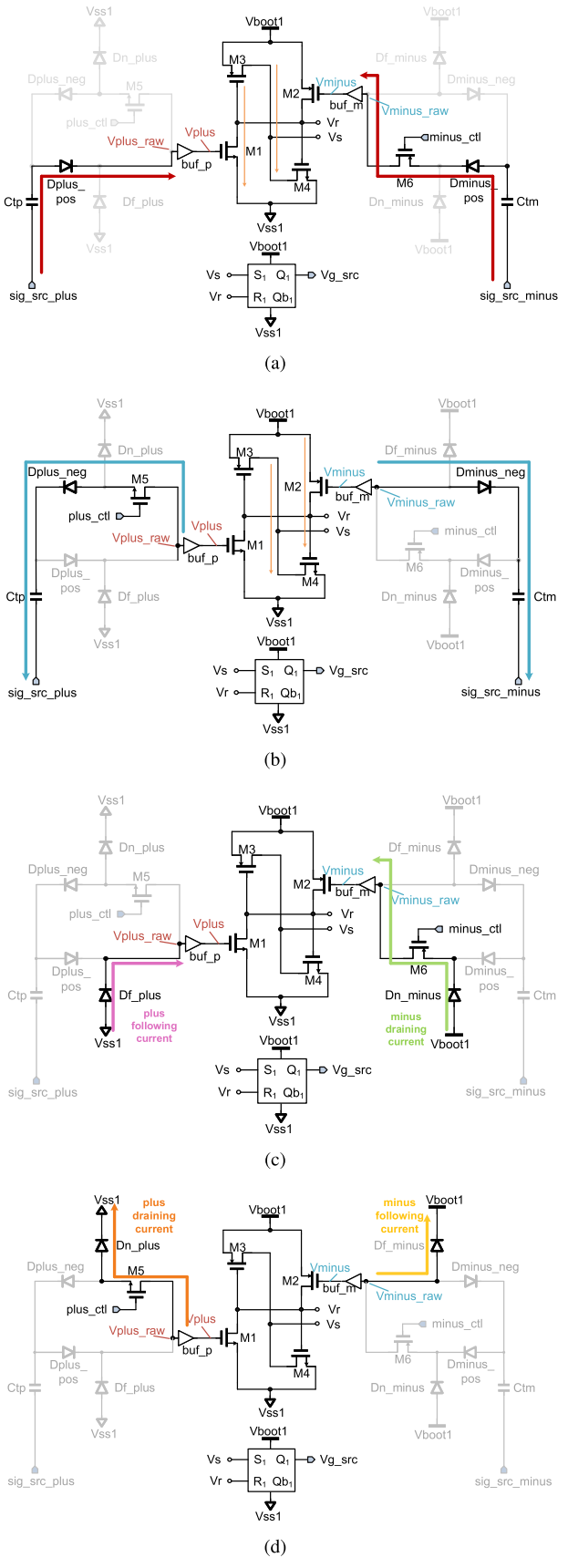


Fig. 6. Main Source Buffer Control (MSBC): (a) Turn-on operation; (b) Turn-off operation; (c) Voltage-rise behavior and corrective current paths; (d) Voltage-fall behavior and corrective current paths.

sig_src_minus in Fig. 1 become high. As shown in Fig. 6(a), these signals propagate through the rectifying diodes Dplus_pos and Dminus_pos, generating pulse signals that couple through the capacitors and pull Vplus_raw and Vminus_raw high. This voltage transition turns on transistor M1 while turning off M2, allowing Vr to discharge to a logic-low level. Subsequently, transistor M3 turns on while M4 turns off, charging Vs to a logic-high level. The SR1 latch is thereby set, generating Vg_src to activate the Main Source Buffer Array. The corresponding active signal path is highlighted by the maroon-colored lines in Fig. 6(a). During Phase II, the floating system potential rises together with the output stage, while the internal nodes maintain the required bias voltages for continuous MSBC operations.

Similarly, the turn-off sequence begins when input to the ANA-AGD, signal, transitions to a low level at the beginning of Phase III–PS, during which the AFB establishes the preset condition for turn-off. In Phase III, the preset state is released to trigger the MSBC. As illustrated in Fig. 6(b), both sig_src_plus and sig_src_minus become low and propagate through the rectifying diodes Dplus_neg and Dminus_neg, generating pulse signals that couple through the capacitors and pull Vplus_raw and Vminus_raw low. Consequently, transistor M1 turns off while M2 turns on, allowing Vs to discharge to a logic-low level. Thereafter, transistor M4 turns on while M3 turns off, charging Vr to a logic-high level. The SR1 latch is reset, causing Vg_src to deactivate the Main Source Buffer Array. The corresponding active signal path is indicated by the blue-colored lines in Fig. 6(b). During Phase IV, the floating system potential returns to its initial level while the MSBC maintains the proper bias conditions throughout the voltage-fall interval.

During the voltage-rise interval (Phase II), the internal nodes Vplus_raw and Vminus_raw cannot inherently follow the rising floating system potential because they are not directly referenced to the floating supply rails. Consequently, charge accumulation and undesirable negative voltage stress may occur. As shown in Fig. 6(c), after transistor M1 turns off, the potential difference between Vplus_raw and Vss1 decreases from 5 V to 0 V. However, as the floating system continues to rise, Vss1 increases by an additional 7 V while Vplus_raw remains nearly unchanged. Consequently, the potential difference becomes -7 V (Vplus_raw - Vss1 = -7 V), which exceeds the allowable operating range of the buf_p devices and may cause gate-oxide overstress. To eliminate this negative voltage buildup, the following diode Df_plus is introduced. Once Vss1 exceeds Vplus_raw, Df_plus becomes forward biased, establishing a following-current path that clamps Vplus_raw to Vss1. As a result, Vplus_raw closely follows the floating ground throughout the voltage-rise interval. The corresponding conduction path is indicated by the pink-colored lines in Fig. 6(c). Meanwhile, charge accumulated at Vminus_raw during the voltage-rise interval may unintentionally turn on transistor M2, causing Vs to discharge and disrupting the intended turn-on operation. To prevent this condition, the draining diode Dn_minus establishes a minus-draining current path that removes the accumulated charge from Vminus_raw. When Vboot1 exceeds Vminus_raw, Dn_minus becomes forward biased

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and clamps Vminus_raw to Vboot1, thereby preventing unintended activation of M2. The corresponding conduction path is highlighted by the green-colored lines in Fig. 6(c).

During the voltage-fall interval (Phase IV), the internal nodes Vplus_raw and Vminus_raw cannot inherently follow the falling floating system potential because they are not directly referenced to the floating supply rails. Consequently, charge accumulation and excessive negative voltage may occur, resulting in unintended transistor activation or overvoltage stress. As shown in Fig. 6(d), charge accumulated at Vplus_raw may unintentionally activate transistor M1, resulting in an undesired rise of Vs. To suppress this behavior, the draining diode Dn_plus provides a discharge path that clamps Vplus_raw to Vss1, once Vss1 falls below Vplus_raw. The corresponding conduction path is indicated by the orange-colored lines in Fig. 6(d). Meanwhile, after transistor M2 turns off, the potential difference between Vboot1 and Vminus_raw decreases from 5 V to 0 V. However, as the floating system continues to fall, Vboot1 decreases by an additional 7 V, while Vminus_raw remains nearly unchanged because it is not directly referenced to the floating supply. Consequently, the potential difference becomes -7 V (Vboot1 - Vminus_raw = -7 V), which exceeds the allowable operating range of the buf_m devices and may cause gate-oxide overstress. To eliminate this negative voltage buildup, the following diode Df_minus is introduced. Once Vboot1 falls below Vminus_raw, Df_minus becomes forward biased, establishing a following-current path that clamps Vminus_raw to Vboot1. As a result, Vminus_raw closely follows the floating supply throughout the voltage-fall interval, preventing overvoltage stress. The corresponding conduction path is indicated by the yellow-colored lines in Fig. 6(d).

Consequently, the addition of the following diodes Df_plus and Df_minus, together with the draining diodes Dn_minus and Dn_plus, effectively stabilizes the voltage transitions of Vplus_raw and Vminus_raw. These corrective elements suppress negative voltage stress, prevent unintended transistor activation, and ensure that both nodes properly follow the floating system potential throughout the voltage-rise and voltage-fall intervals, thereby guaranteeing reliable MSBC operation under all switching conditions.

2) Active Float Bridge (AFB): To ensure reliable operation of the floating system without overstressing internal devices, the AFB generates the plus_ctl and minus_ctl control signals required by the MSBC. As shown in Fig. 7(a), the AFB circuit accepts a single input, signal, and produces the outputs, plus_ctl and minus_ctl, by buffering the internal node ctl_raw.

During Phase I–PS, the input to the ANA-AGD, signal, transitions to a high level while signal_bar becomes low. As shown in Fig. 7(b), the falling transition of signal_bar is capacitively coupled through Ctgp and Ctgm, pulling both Vpush_tri and Vpull_tri toward the floating ground reference. Once these trigger nodes reach the logic-low level, the corresponding inverters, inv3 and inv4, drive Vpush and Vpull high. Consequently, the Push MOS turns on while the Pull MOS remains off, rapidly discharging ctl_raw to the floating ground Vss1. The buffered outputs, plus_ctl and minus_ctl,

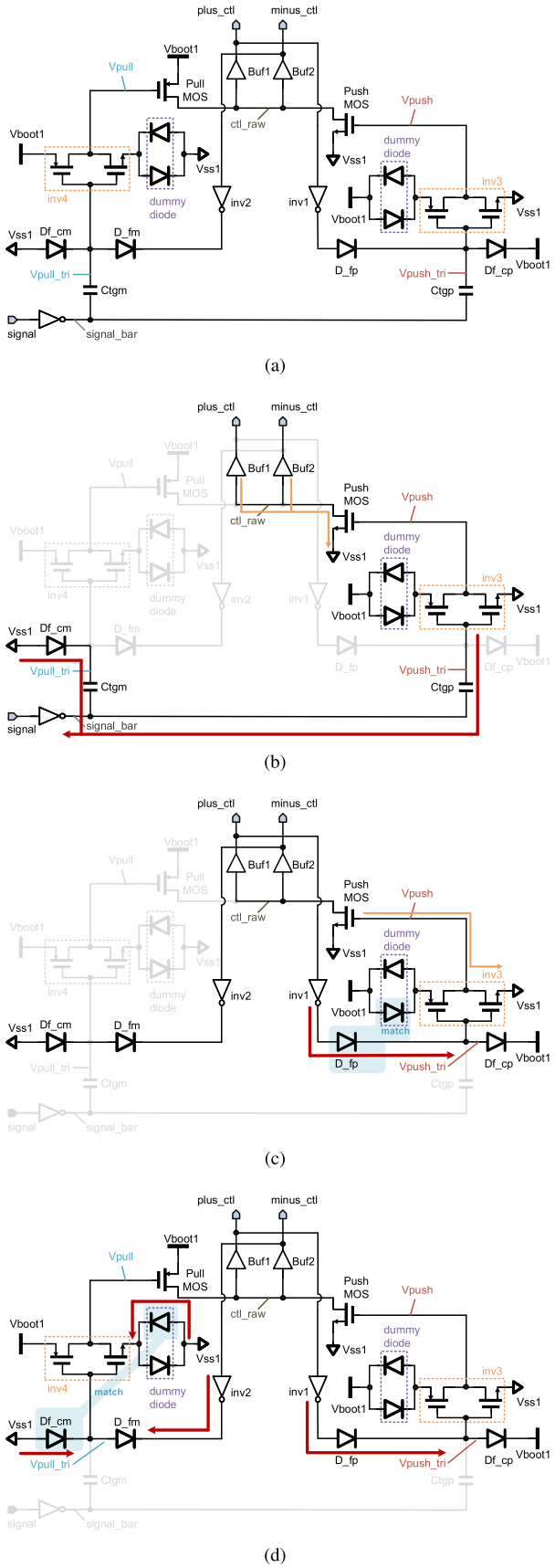


Fig. 7. Active Float Bridge (AFB): (a) Circuit schematic; (b) Phase I–PS (preset operation); (c) Phase I (preset release); (d) Phase II (voltage-rise operation).

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are thereby initialized to the required logic-low state before activation of the Main Source Buffer Array.

After the preset operation is completed, Phase I begins by releasing the preset state. As illustrated in Fig. 7(c), inverter inv1 charges Vpush_tri back toward the logic-high level, thereby turning off the Push MOS and completing the reset operation. During this interval, diode D_fm prevents Vpull_tri from being unintentionally charged to the logic-high level, thereby avoiding false activation of the Pull MOS. As the preset state is released, the MSBC is triggered to generate Vg_src, initiating the activation of the Main Source Buffer Array.

During the subsequent voltage-rise interval (Phase II), the floating system potential increases together with the output stage. As shown in Fig. 7(d), the presence of the coupling capacitor Ctgp slows the voltage rise of Vpush_tri, which may temporarily reactivate the Push MOS. Through the internal feedback path, the unwanted charge accumulated at ctl_raw is rapidly discharged, restoring the node to the floating ground and immediately turning off the Push MOS. Meanwhile, the following diode Df_cm ensures that Vpull_tri continuously follows the floating ground Vss1, preventing inadvertent activation of the Pull MOS throughout the voltage-rise interval.

The turn-off sequence operates in a complementary manner. During Phase III–PS, the Pull MOS presets ctl_raw before the preset state is released in Phase III to deactivate the Main Source Buffer Array. During the subsequent voltage-fall interval (Phase IV), the internal feedback path removes any residual charge from ctl_raw, while diodes D_fp and Df_cp ensure that the control nodes properly follow the falling floating system potential, thereby preventing false switching of the Push and Pull MOS devices. In addition, the pair of dummy diodes, shown by the purple dotted boxes in Fig. 7(a), compensates for the voltage mismatch introduced by diodes Df_cm and D_fp during the turn-on sequence, and by diodes D_fm and Df_cp during the turn-off sequence, thereby ensuring symmetrical operation under both switching conditions.

B. Sink Buffer Array

The Sink Buffer Array is an NMOS-based pull-down network responsible for turning off the SiC MOSFET. During the turn-off transition, it provides the required discharge current to pull the gate voltage to a low level.

1) Sink Buffer Control: This circuit used to manage the operation of the Sink Buffer Array. It functions as a strong buffer for driving the Sink Buffer Array and operates using the global supply and ground references, Vddf and VSSG, respectively.

2) Split-Path Circuit and Delay Match: The Split-Path circuit generates two complementary and non-overlapping control signals to drive the pull-up and pull-down networks while while preventing shoot-through conditions, which have been reported [9], [26], [27]. The Delay match circuit compensates for the intrinsic delay of the pull-up path, ensuring timing symmetry between the two networks.

C. B-D Source Buffer

The B-D Source Buffer is an auxiliary circuit introduced alongside the B-D source buffer control and operates in parallel

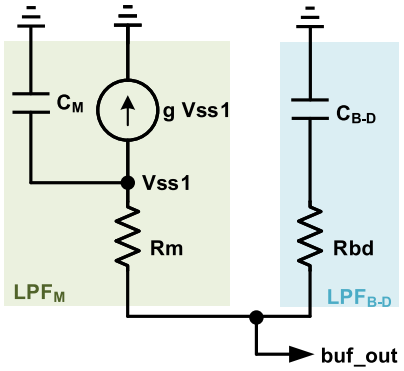


Fig. 8. Equivalent small-signal model illustrating the formation of two low-pass filters from buf_out view.

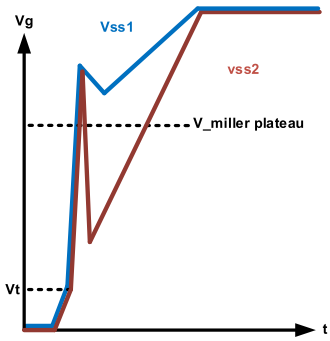


Fig. 9. Transient voltage difference between Vss1 and Vss2 caused by high-frequency CSIV components.

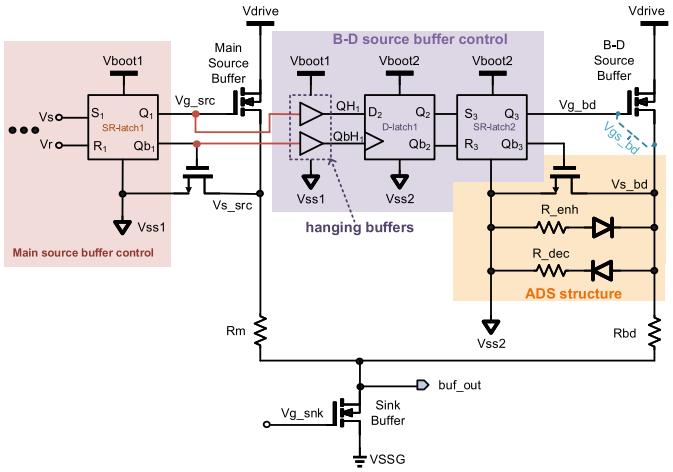


Fig. 10. B-D source buffer control with ADS structure.

with the Main Source Buffer Array, as shown in Fig. 1. Its purpose is to suppress the CSIV spikes that appear at the gate during fast switching of the SiC MOSFET. Since the CSIV spike appears at the common source node, which serves as the reference ground for both the Main Source Buffer Array and the B-D Source Buffer, their reference grounds are intentionally separated using a large resistor Rm and a small resistor Rbd, creating three distinct voltage nodes (buf_out, Vs_bd and Vs_src in Fig. 10). The small signal equivalent circuit is shown in the Fig. 8. From the buf_out node, the two source buffers and their channel impedances form two low-

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pass filters, LPF_M and $LPF_{B\text{-}D}$, each with a different cutoff frequency, respectively given by:

$$f_{LPF,M} = \frac{1}{2\pi \cdot Rm \cdot C_M} \tag{1}$$

$$f_{LPF,B-D} = \frac{1}{2\pi \cdot Rbd \cdot C_{B-D}} \tag{2}$$

where $f_{LPF,M}$ and $f_{LPF,B-D}$ denotes the cutoff frequencies of the LPF_M and LPF_{B-D} paths, respectively; Rm and Rbd are the corresponding resistances; and C_M and C_{B-D} are the effective capacitances associated with each path.

To explain the detection-free mechanism, the two buffer paths can be modeled as first-order low-pass filters with distinct dynamic responses. The Main Source Buffer path (LPF_M) and the B–D Source Buffer path (LPF_{B-D}) can be expressed as:

$$H_1(s) = \frac{Vss1}{V_{buf_out}} \approx \frac{1}{1 + g_{ds,sat} \cdot Rm + s \cdot Rm \cdot C_M} \tag{3}$$

$$H_2(s) = \frac{Vss2}{V_{buf_out}} \approx \frac{1}{1 + s \cdot Rbd \cdot C_{B_D}} \tag{4}$$

where $H_1(s)$ and $H_2(s)$ represent the transfer functions of LPF_M and LPF_{B-D}, respectively. Since Rm ≫ Rbd, the corresponding time constants satisfy:

$$\tau_M = Rm \cdot C_M \gg \tau_{B_D} = Rbd \cdot C_{B_D} \tag{5}$$

indicating that LPF_M behaves as a slow low-pass filter, while LPF_{B-D} exhibits a much faster dynamic response.

During fast switching of SiC MOSFETs, the CSIV spike contains high-frequency components typically in the tens to hundreds of MHz range. For these high-frequency components, the response of LPF_M is significantly attenuated due to its low cutoff frequency, whereas LPF_{B-D} allows the signal to pass with relatively small attenuation. As a result, a transient voltage difference is generated between the two floating grounds:

$$\Delta V(s) = Vss2(s) - Vss1(s) = [H_2(s) - H_1(s)]\, V_{buf_out} \tag{6}$$

For frequencies much higher than the cutoff of LPF_M (i.e., $\omega \gg \frac{1}{\tau_M}$), $H_1(j\omega) \approx 0$ while $H_2(j\omega) \approx 1$, leading to:

$$\Delta V \approx V_{buf_out} \tag{7}$$

In contrast, for low-frequency components, both paths exhibit similar gains ($H_1 \approx H_2 \approx 1$), resulting in negligible voltage difference. Therefore, only high-frequency CSIV spikes produce a significant transient ΔV, which naturally serves as the trigger signal for the B–D Source Buffer control.

Due to these differing frequency responses, the two buffer systems produce different voltage responses to the signal at buf_out. When a CSIV spike occurs, this mismatch generates a significant voltage difference between the two systems. The resulting voltage difference between Vss1 and Vss2, as depicted in Fig. 9, becomes large enough to exceed the logic-high threshold of the B-D Source Buffer device in Fig. 1. This voltage difference directly serves as the trigger for the B-D source buffer control, which activates the B-D Source Buffer to counteract and suppress the CSIV spike.

This behavior demonstrates that the proposed dual-buffer structure inherently performs frequency-selective differential of CSIV spikes, eliminating the need for explicit sensing circuitry.

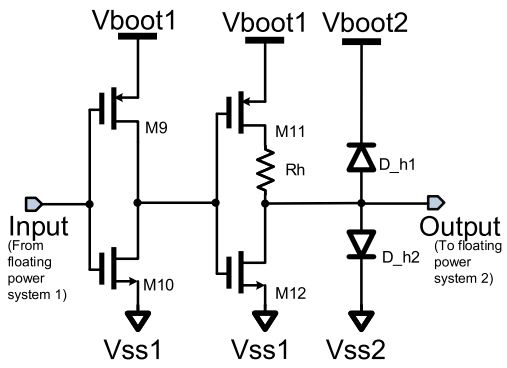


Fig. 11. Schematic of the hanging buffer in the B-D source buffer control.

1) B-D Source Buffer Control: Based on the observed CSIV-induced voltage difference between the two source buffer systems, the B-D source buffer control is implemented using a pair of hanging buffers, a D-latch, and an SR-latch, as shown in the purple block of Fig. 10. During SiC MOS turn-on, the Main Source Buffer is activated first, causing a rapid voltage rise due to the CSIV spike. The subsequent voltage disturbance at buf_out, combined with the different ground isolation resistances Rm and Rbd, generates a voltage difference between the two source buffer systems. This voltage difference directly triggers the B-D Source Buffer, which supplies additional current to suppress CSIV-induced oscillations.

In the IC implementation, the detection mechanism is further optimized. During turn-on, the Qb1 signal from the Main Source Buffer system is transferred through the hanging buffer and compared with the B-D system ground in the D-latch. Once the voltage difference exceeds the logic threshold, the event is captured and stored by the SR-latch, activating the B-D Source Buffer. During turn-off, the B-D Source Buffer is disabled simultaneously with the Main Source Buffer via the Q1 signal, terminating the compensation current.

The hanging buffers in purple-colored block of Fig. 10 are used to safely transmit signals between the two floating systems without collapsing their voltage difference. The hanging buffers employ a cascaded inverter structure with a series resistor (Rh) and output clamping diodes, a novel design, as shown in the Fig. 11. The series resistor (Rh) absorbs most of the inter-system voltage stress while preserving sufficient voltage variation to trigger CSIV cancellation. This structure allows the B-D system to momentarily drop relative to the Main Source Buffer system during a CSIV spike, enabling fast and reliable spike detection without additional sensing circuitry.

2) Adaptive Drive Strength (ADS) Structure: The ADS structure is implemented by inserting R_enh and R_dec between the gate and source terminals of the B–D Source Buffer, forming a negative-feedback loop that dynamically regulates its drive strength (current), as shown in the orange block in Fig. 10. Unlike conventional fixed-strength gate drivers, the proposed ADS automatically adjusts the compen-

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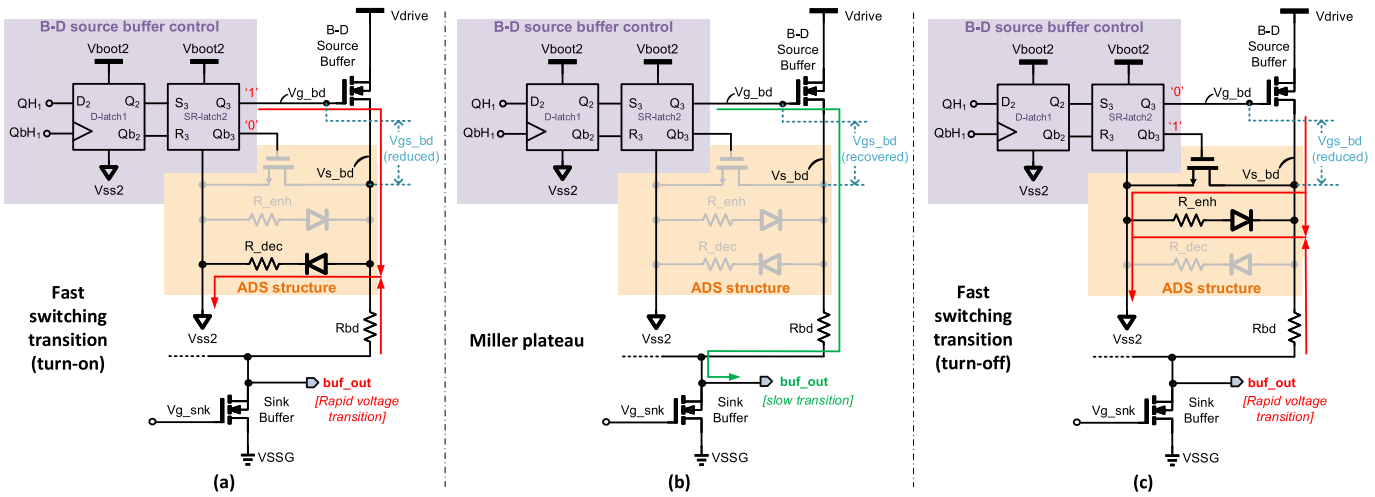


Fig. 12. Operating mechanism and current conduction paths of the proposed ADS structure during different switching stages: (a) Fast turn-on transition; (b) Miller plateau; (c) Fast turn-off transition.

sation current according to the switching condition, thereby suppressing excessive current injection during fast switching transitions while providing enhanced driving capability during the Miller plateau. Consequently, the proposed ADS realizes the adaptive gate-driving strategy reported in [28] without requiring additional timing or interval detection circuits. The operating mechanism and corresponding current paths of the proposed ADS during different switching stages are illustrated in Fig. 12.

As shown in Fig. 12(a), during the turn-on transition, the rapid rise of buf_out introduces high-frequency voltage components at the source terminal of the B–D Source Buffer. Through the feedback network formed by R_dec and C_{B-D}, these high-frequency components generate a transient voltage drop across R_dec, thereby reducing the effective gate-to-source voltage, Vgs_bd. Consequently, the driving strength of the B–D Source Buffer is temporarily weakened, limiting the compensation current injected into buf_out. As highlighted by the red-colored current path in Fig. 12(a), the compensation current is therefore reduced during the rapid switching interval, suppressing excessive current injection and mitigating CSIV-induced oscillations.

As shown in Fig. 12(b), when the switching process enters the Miller plateau, the variation of buf_out becomes significantly slower and is dominated by low-frequency components. Under this condition, the voltage drop across R_dec becomes negligible, allowing Vgs_bd to recover toward its steady-state value. Consequently, the B–D Source Buffer provides a larger compensation current, enabling the SiC MOSFET gate voltage to traverse the Miller plateau more rapidly, thereby reducing the switching time and switching loss. The highlighted green-colored current path in Fig. 12(b) illustrates the enhanced driving capability provided during this stage.

Similarly, Fig. 12(c) illustrates the fast turn-off transition. As buf_out decreases rapidly, the feedback network formed by R_enh and C_{B-D} provides an analogous negative-feedback mechanism. The rapid decrease of buf_out generates a transient voltage across R_enh, which dynamically regulates Vgs_bd and automatically adjusts the discharge current according to the switching speed. As indicated by the highlighted red-colored current path in Fig. 12(c), excessive discharge current during the fast switching interval is effectively suppressed while sufficient driving capability is maintained throughout the remainder of the turn-off process.

The frequency-dependent behavior of the proposed ADS can be modeled as a first-order low-pass network. Accordingly, the effective gate-to-source voltage of the B–D Source Buffer is expressed as,

$$\mathrm{Vgs_bd} = \frac{1}{1 + \mathrm{j}\left(\frac{\mathrm{f}}{\mathrm{f_c}}\right)} \tag{8}$$

where f denotes the frequency component of the switching transient and f_c is the cutoff frequency of the corresponding feedback network. The cutoff frequency (f_c) during charging and discharging of buf_out are given by,

$$\mathrm{f_{c1}} = \frac{1}{2\pi \cdot R_enh \cdot C_{B-D}} \tag{9}$$

$$\mathrm{f_{c2}} = \frac{1}{2\pi \cdot R_dec \cdot C_{B-D}} \tag{10}$$

Therefore, the proposed ADS inherently provides a reduced driving strength during the high di/dt interval, where excessive compensation current may induce CSIV-related oscillations, while automatically increasing the driving strength during the Miller plateau to accelerate the switching process and reduce switching loss. This adaptive behavior is consistent with the optimal SiC MOSFET gate-driving strategy reported in [28], which recommends a lower driving current during the high di/dt interval and a higher driving current during the Miller plateau to achieve an improved trade-off between switching stability and efficiency. The proposed ADS realizes this adaptive strategy solely through the passive feedback network, eliminating the need for additional sensing or interval detection circuitry.

III. Simulation and Measurement Verifications

The proposed ANA-AGD is implemented using the TSMC 0.18-μm CMOS HV BCD (T18HVG2) process. Fig. 13 shows the chip layout, floor plan and die photo of the proposed

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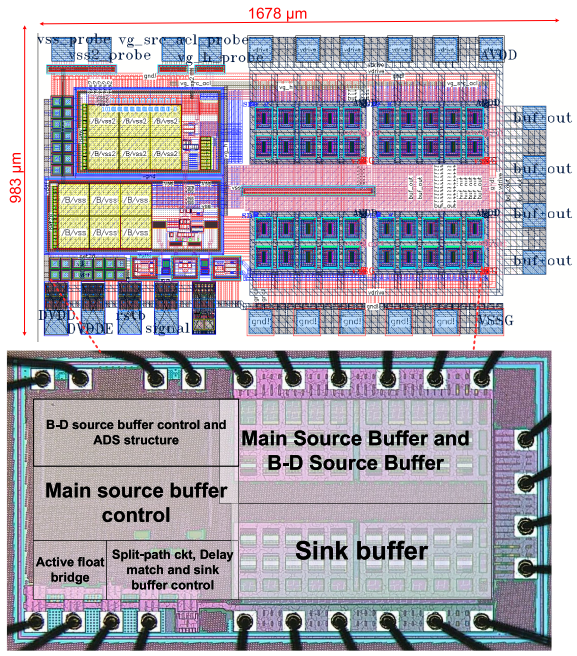


Fig. 13. Layout, Floorplan and die photo of the proposed ANA-AGD.

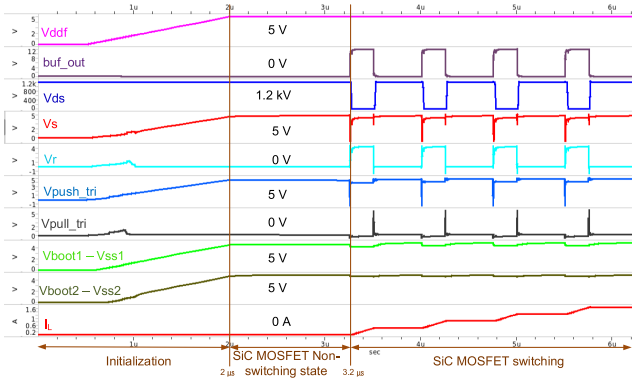


Fig. 14. Post-layout transient simulation showing start-up, and inductive-load switching behaviour of the proposed ANA-AGD.

ANA-AGD. The total chip area is 1678 μm $\times$983 μm, while the core area measures 1451.9 μm $\times$678.31 μm.

A. Post-Layout Simulations

Fig. 14 shows the simulated startup and non-switching behavior of the proposed ANA-AGD, where all relevant internal nodes are naturally established from zero initial conditions as the bootstrap supply voltages Vboot1−Vss1 and Vboot2−Vss2 reach their nominal 5 V levels. During the non-switching interval, Vr, Vs, Vpull_tri, and Vpush_tri remain at well-defined and stable voltage levels, confirming proper initialization before the first switching event. Subsequently, the proposed ANA-AGD successfully drives the SiC MOSFET under a 1.2 kV inductive-load switching condition, with stable internal-node behavior during the fast switching transients.

Fig. 15 illustrates the post-layout DPT simulation used to evaluate the ANA-AGD with a parasitic-aware SiC MOSFET model, under inductive-load and 1.2 kV high-voltage switching condition, representative of the high-dv/dt environment

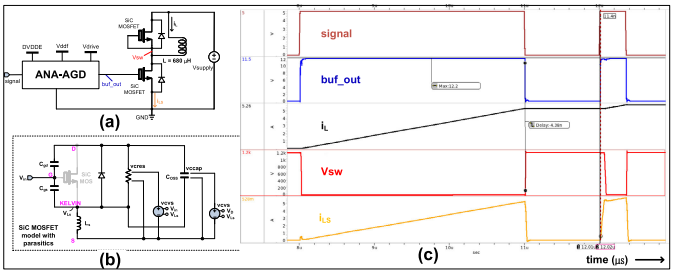


Fig. 15. Double-pulse-test (DPT) setup and post-layout simulation of the proposed ANA-AGD: (a) Schematic of the DPT circuit; (b) Parasitic-aware IMBF170R450M1 SiC MOSFET model, including C_{gs}, C_{gd}, C_{ds} source inductance (L_s), and drain inductance (L_d); (c) Simulated DPT waveforms of the input signal, gate-drive output voltage, inductor current, switching-node voltage, and source current.

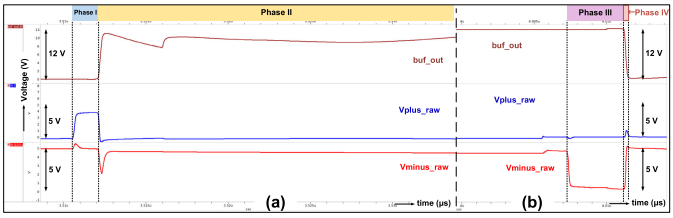


Fig. 16. Post-layout transient simulation of the MSBC: (a) during turn-on operation (Phases I and II); (b) during turn-off operation (Phases III and IV).

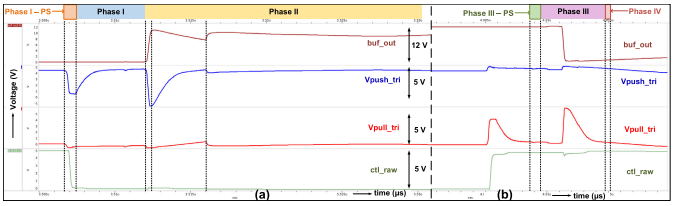


Fig. 17. Post-layout transient simulation of the AFB: (a) during turn-on operation (Phases I–PS, I, and II); (b) during turn-off operation (Phases III–PS, III, and IV).

encountered during high-voltage SiC switching. As shown in Fig. 15(a), the ANA-AGD drives the lower SiC MOSFET of the DPT circuit, while the upper device provides the commutation path for the inductive load. The parasitic-aware SiC MOSFET model shown in Fig. 15(b) incorporates the major device parasitics.The simulated waveforms in Fig. 15(c) demonstrate that the gate-drive output buf_out maintains a well-defined 12 V level during the conduction interval, while the inductor current i_L increases approximately linearly. During the switching transition, Vsw undergoes a rapid voltage transition and the source current i_{LS} exhibits the corresponding transient response, demonstrating proper operation of the ANA-AGD under inductive-load switching conditions.

As described in Sec. II-A, the MSBC and the AFB operate according to the timing sequence illustrated in Fig. 4. To verify their operation, post-layout transient simulations were performed using a 5 V input signal with a switching frequency of 500 kHz and rise and fall times of 10 ns. The simulated waveforms are presented in Figs. 16, and 17. Fig. 16(a) verifies the MSBC during turn-on operation corresponding to Phases I and II of Fig. 4, while Fig. 16(b) verifies the MSBC during the turn-off operation corresponding to Phases III and IV.

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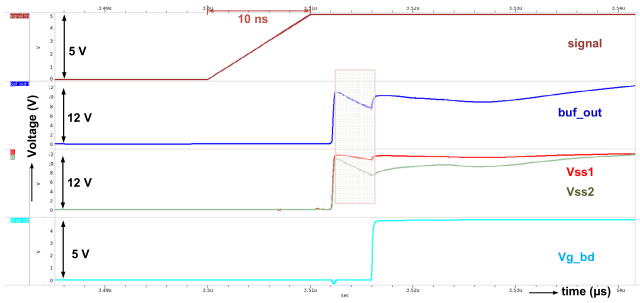


Fig. 18. Post-layout transient simulation demonstrating CSIV spike suppression by the B-D source buffer control with ADS structure.

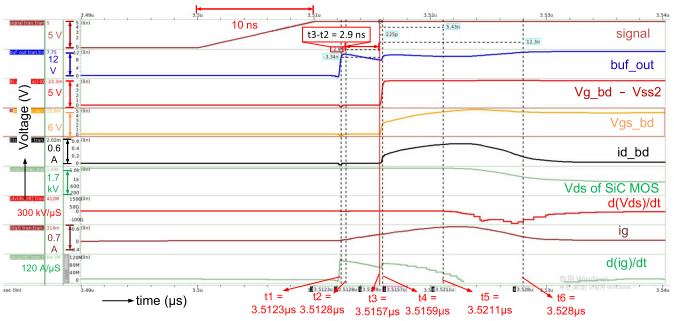


Fig. 19. Post-layout transient simulation illustrating the operating mechanism of the ADS during the CSIV spike suppression.

Similarly, Fig. 17(a) verifies the AFB during turn-on operation corresponding to Phases I - PS, I, and II, while, Fig. 17(b) verifies the AFB during turn-off operation corresponding to Phases III - PS, III, and IV. The simulated waveforms demonstrate the expected transitions of Vplus_raw, Vminus_raw, Vpush_tri, Vpull_tri, ctl_raw, and buf_out, confirming the correct operation of the proposed MSBC and AFB throughout the complete switching cycle.

As described in Sec. II-C, B-D source buffer control with ADS detects and suppresses the CSIV spikes appearing at buf_out during switching. To verify its operation, post-layout transient simulations were performed using a 5 V input signal with a switching frequency of 500 kHz and rise and fall times of 10 ns. The simulated waveform is presented in Fig. 18, demonstrating the CSIV spike suppression function of the proposed B-D source buffer control. The relationships among signal, buf_out, Vg_bd, Vss1, and Vss2 show that the CSIV spikes are rapidly detected, and the corresponding control signal is generated to suppress the transient, confirming the fast response and correct operation of the proposed B-D source buffer control.

The functionality of the ADS structure is verified in Fig. 19. The time markers t1~t6 indicate the critical operating points during the switching event. During t1~t2, generates the first di/dt peak, where the di/dt is limited by Rm. At t3, the B–D source buffer control is activated upon detecting oscillations at buf_out, effectively suppressing the oscillations. Following the onset of oscillation, the B–D source buffer responds within 2.9 ns. At t4, the B–D Source Buffer produces the second di/dt peak; at this instant, the ADS structure reduces the drive-strength current (id_bd) to accommodate the high di/dt

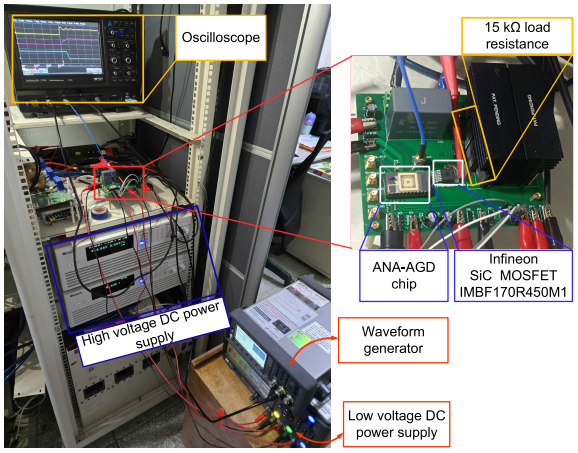


Fig. 20. Measurement environment.

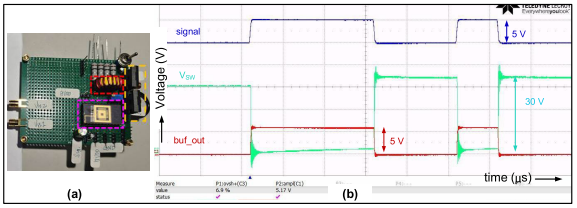


Fig. 21. Experimental DPT evaluation of the proposed ANA-AGD: (a) prototype DPT setup implemented on a perfboard; (b) measured DPT waveforms.

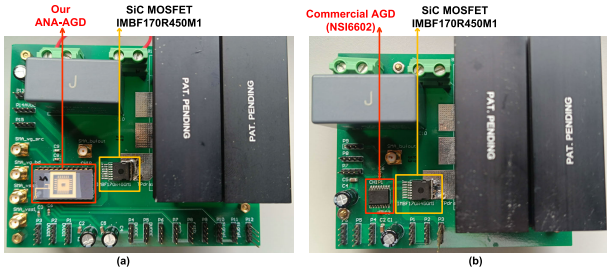


Fig. 22. PCBs used for testing the proposed ANA-AGD and the commercial AGD (NSI6602).

condition. From t5 to t6, when the dv/dt reaches its maximum, the ADS dynamically enhances the drive strength to maintain efficient switching. The simulated Vgs_bd, id_bd, Vds, and Vgs waveforms of the SiC MOSFET confirm the fast response and reliable operation of the proposed ANA-AGD.

With supply voltages of Vdrive = 12 V, DVVDE = 5 V, and Vddf = 5 V, the ANA-AGD demonstrates a rise time of 28.9 ns, a fall time of 20.5 ns, a rise delay of 40.2 ns, a fall delay of 30.2 ns, and a power consumption of 138 mW at 500 kHz as the worst-case conditions in all-PVT-corner simulations. This power consumption is lower by 99.5%, 52.2%, 17.37%, and 37.56% compared with [13], [14], [15], and [16], respectively.

B. Measurements

The ANA-AGD is evaluated while driving an Infineon SiC MOSFET (IMBF170R45M1) with a 15 kΩ load resistance, using high-voltage DC supplies from 30 V to 1.2 kV (Vsupply) and low-voltage supplies 5 V (DVVDE, Vddf) and 12 V

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TABLE I
PERFORMANCE COMPARISON

	[30]	[8]	[12]	[31]	[9]	[17]	[18]	This work
Year	2018	2019	2022	2023	2025	2025	2026	2026
Publication	TI	TPE	ISPSD	TI	OJCAS	TCAS II	JCSC	TCAS-I
Technology (nm)	N.A.	CPLD	180 BCD + FPGA	N.A.	T18HVG2 (180)	T18HVG2 (180)	T18HVG2 (180)	T18HVG2 (180)
Driver type	Active	Active	Active	Active	Active	Active	Active	Active
VDD (V)	10∼20	20 & -5	1.8, 3.3 & 20	5∼18	5 & 10	5 & 10	5 & 10	5 & 12
f_{PWM} (MHz)	0.5	9.2	0.1	1	0.5	0.5	0.4	**0.001∼3**
t_{rise} (ns)	35 at 15 V	N.A.	N.A.	28 at 12 V	164 at 10 V	260 at 10 V	197.8 at 10 V	**21.6 at 1.2 kV**
t_{fall} (ns)	16 at 15 V	N.A.	N.A.	18 at 12 V	165 at 10 V	257 at 10 V	94.2 at 10 V	**2.3 at 1.2 kV**
Chip area (mm^2)	N.A.	N.A.	2.5 x 2.5	N.A.	5.26 × 1.05	5.26 × 1.05	4.9 x 1.05	**1.67 x 0.98**
P_{dis_total}	187 mW at 0.35 MHz	N.A.	79.51 mW*	180 mW at 0.5 MHz	787 mW at 0.5 MHz	568 mW at 0.5 MHz	533 mW at 0.4 MHz	**58 mW** at 0.5 MHz
FoM	N.A.	N.A.	N.A.	N.A.	0.000699	0.000617	0.000999	2.624215

*Power consumption of FPGA is excluded

$$\text{FoM} = \frac{f_{PWM}(\max)}{\text{Chip area} \times P_{dis_total} \times \frac{t_{rise}+t_{fall}}{2}}$$

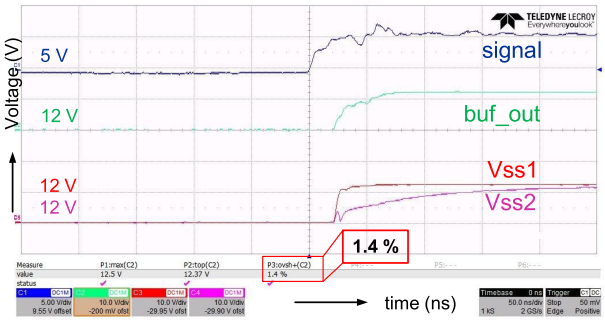


Fig. 23. Detailed view of measurements of the ANA-AGD at the rising edge of buf_out for signal = 500 kHz, Vsupply = 1.2 kV.

(Vdrive). The measurement setup is shown in the Fig. 20. Experimental DPT evaluation of the proposed ANA-AGD was also performed using a prototype implemented on a perfboard, as shown in Fig. 21(a). Owing to the available laboratory supply voltage, the test was performed at Vsupply = 30 V, with a 5 V input signal and a 12 V gate-drive supply. The measured waveforms in Fig. 21(b) demonstrate successful gate-drive operation and switching-node transitions during the DPT, providing additional experimental evidence of the ANA-AGD's operation under inductive-load (25 μH) switching conditions.

Fig. 22 shows the designed PCB to test the proposed ANA-AGD (Fig. 22(a)), as well as a similar PCB (Fig. 22(b)) used to evaluate the commercially available gate driver (NSI6602) [29] under identical measurement conditions. The NSI6602 employs an architecture consisting of an input logic stage, isolation barrier, Under voltage lock-out protection, and a push-pull output driver. To ensure a fair comparison, both drivers were evaluated using the same PCB configuration, SiC MOSFET device, supply voltages, load resistance, and switching frequency. Similar to commercially available gate drivers UCC27710 [30] and LM2105 [31] listed in Table I, the NSI6602 datasheet does not describe dedicated adaptive gate-driving or CSIV spike suppression circuitry in its architecture. In contrast, the proposed ANA-AGD incorporates the Boost-Damp (B-D) Source Buffer with a control and Adaptive Driving Strength structure to actively suppress CSIV spikes

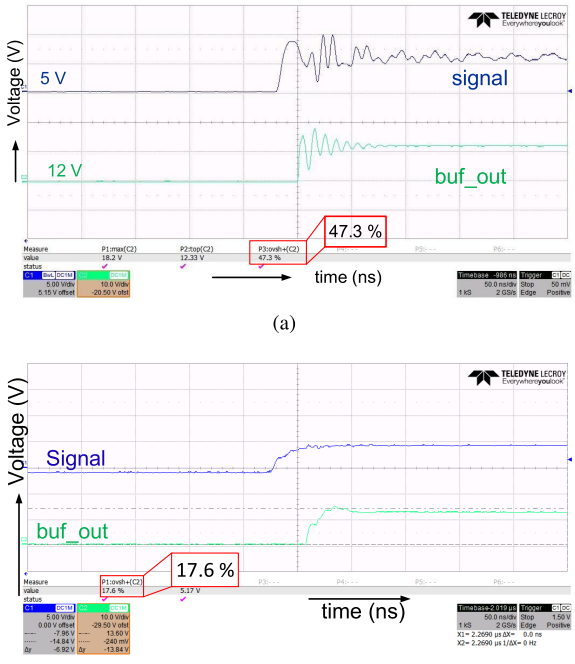


Fig. 24. Measurements of the Commercial chip under the same operating conditions (signal = 500 kHz, Vsupply = 1.2 kV): (a) Commercial chip without external drive strength adjustment, Detailed view at the rising edge of buf_out; (b) Commercial chip with external drive strength adjustment, Detailed view.

while dynamically regulating the gate-driving current during switching. The percentage values annotated in Fig. 24 represent the overshoot in the buf_out (gate voltage) waveform, defined as:

$$\text{Overshoot}(\%) = \frac{V_{peak} - V_{steady}}{V_{steady}} \times 100\% \qquad (11)$$

where V_{peak} is the maximum transient voltage during switching and V_{steady} is the steady-state gate voltage level.

For a signal frequency of 500 kHz and Vsupply of 1.2 kV, the detailed view of measurements at the rising edge of buf_out of the proposed ANA-AGD when driving the SiC MOSFET, is shown in Fig. 23. The measured overshoot in

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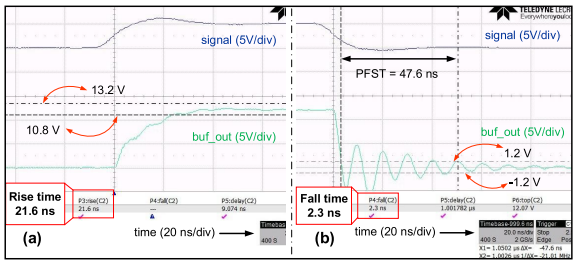


Fig. 25. Rise time and fall time measurements of the ANA-AGD for signal = 500 kHz, Vsupply = 1.2 kV.

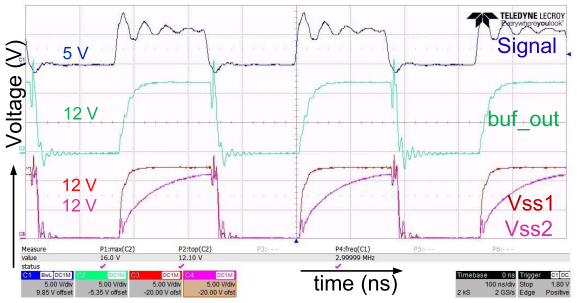


Fig. 26. ANA-AGD working at at signal = 3 MHz, Vsupply = 1.2 kV.

buf_out of the ANA-AGD is 1.4%, the post-rise settling time (PRST) is 0 ns and post-fall settling time (PFST) is 47.6 ns. Under the same measurement environment, Fig. 24(a) presents the measurement results of the commercial AGD without any external gate-drive adjustment. The measured overshoot in the buf_out of the commercial AGD is 47.3%, the post-rise settling time (PRST) is 43.6 ns and post-fall settling time (PFST) is 45.5 ns. After introducing an external adjustable gate resistor to reduce and match its effective gate-driving strength with that of the proposed ANA-AGD, the overshoot is reduced to 17.6%, as shown in Fig. 24(b). This comparison demonstrates the influence of external drive-strength adjustment on the switching transient of the commercial gate driver, but the proposed ANA-AGD achieves low overshoot through its intrinsic adaptive gate-driving mechanism without requiring external gate-drive adjustment. For a signal frequency of 500 kHz, with the supply voltages of 5 V (DVVDE, Vddf) and 12 V (Vdrive) while driving the Infineon SiC MOSFET (IMBF170R45M1), the proposed ANA-AGD exhibits a measured power consumption of 58 mW. Under the same measuring environment, the commercial AGD (NSI6602) exhibits a measured power consumption of 82 mW. Fig. 25 shows the measured turn-on and turn-off switching waveforms of the proposed ANA-AGD at a signal frequency of 500 kHz and a Vsupply of 1.2 kV. The measured rise and fall times are 21.6 ns and 2.3 ns, respectively. As shown in Fig. 25(a), the output reaches its steady-state value immediately after the rise transition without observable residual oscillation. As shown in Fig. 25(b), though the output reaches the 10% voltage level within 2.3 ns during turn-off transition, the remaining oscillatory transient settles within approximately 47.6 ns.

For a Vsupply of 1.2 kV, Fig. 26 further confirm that the proposed ANA-AGD operates reliably up to 3 MHz, with successful suppression of CSIV spikes on the rising edge of the buffer in all cases. In addition, for signal frequency of 100 kHz

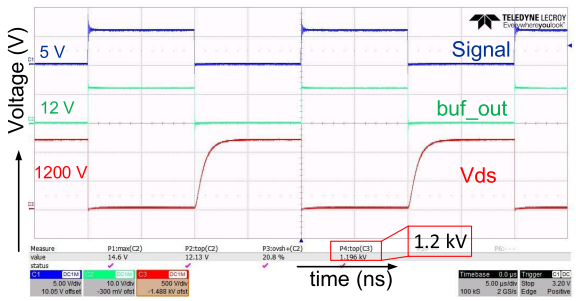


Fig. 27. Measurements of the ANA-AGD for signal = 100 kHz, Vsupply = 1.2 kV.

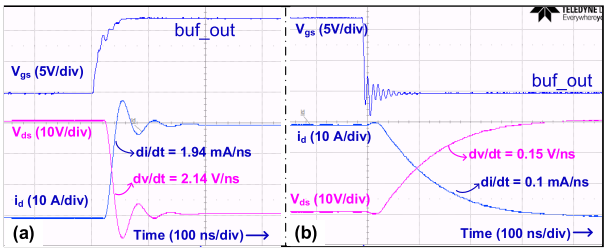


Fig. 28. Measured Vgs, Vds and i_d waveforms of the SiC MOSFET, during (a) turn-on and (b) turn-off transitions at Vsupply = 30 V.

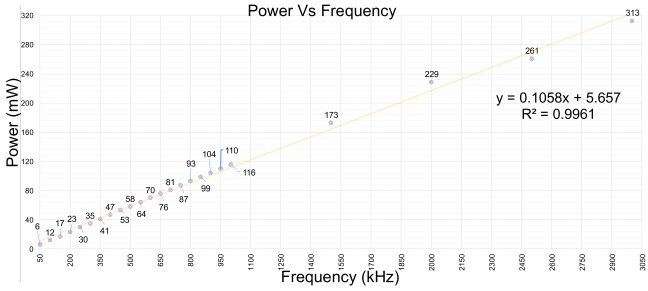


Fig. 29. Power of proposed ANA-AGD in different frequencies (50 kHz ~ 3 MHz).

and Vsupply of 1.2 kV, Fig. 27 shows the measured waveforms of the proposed ANA-AGD when driving the SiC MOSFET, including the signal, buf_out (Vgs of the SiC MOSFET), and the Vds of the SiC MOSFET. Fig. 28 shows the measured Vgs, Vds, and i_d waveforms of the SiC MOSFET during the turn-on and turn-off transitions. These measured results verify the switching behavior of the proposed ANA-AGD at Vsupply = 30 V. The comparison with the prior works for power transistor drivers is summarized in Table I, showing that our core area (1.6494 mm^2) is 73.6%, 70.14%, 70.14%, and 67.93% smaller than [9], [12], [17], and [18], respectively, with no off-chip FPGA or external logic required. The power consumption of ANA-AGD for various frequencies of signal is provided in Fig. 29, along with a linear trend line.

IV. Conclusion

This work demonstrates that an all-NMOS adaptive gate driver architecture can simultaneously achieve high switching speed, robust oscillation suppression, and compact IC implementation for high-voltage SiC MOSFET applications. By exploiting the differential transient behavior of two floating

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NMOS source buffers, the proposed ANA-AGD suppresses CSIV-induced oscillations intrinsically, without relying on explicit sensing circuits or complex feedback networks. The integration of AFB and adaptive drive-strength control further ensures reliable signal transfer and optimal gate-current regulation under rapidly changing floating potentials.

The fabricated prototype in a 0.18-μm HV CMOS process validates the practicality of the proposed concept through both post-layout simulations and measurements. Stable operation is achieved over a wide frequency range from 1 kHz to 3 MHz while driving a 1.2 kV SiC MOSFET, with measured rise times below 25 ns at 500 kHz and 58 mW power consumption. These results indicate that the proposed driver is well-suited for demanding applications such as high-frequency isolated DC–DC converters, solid-state transformers, and electric-vehicle traction inverters, where fast switching, low EMI, and high-voltage robustness are essential.

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