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A 155 V/ns-CMTI on-chip digital multi-layer coreless transformer-based isolated gate driver using 0.18-μm HV CMOS process

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Abstract
The increasing demand for efficient and reliable power electronic systems in applications such as data centers, motor drivers, solar inverters, and industrial automation has necessitated advancements in gate driver technologies. This paper presents a novel isolated gate driver (IGD) that incorporates a coreless, six-layer overlapping coil structure integrated into a digital transformer, fabricated using a standard 0.18-μm HV CMOS process. The design achieves high mutual inductance within a compact footprint, with an overall chip area of 1980 μm × 1580 μm and a core area of 1514.96 μm × 1205.36 μm on silicon. The IGD was evaluated through both simulations and measurements to assess its common-mode transient immunity (CMTI) and signal regeneration capabilities. The results demonstrate a CMTI tolerance of up to 155 V/ns in post-layout simulations. The IGD maintains stable operation across a wide input frequency range from 1 kHz to 5 MHz, demonstrates reliable duty-cycle regeneration from 5% to 95%, and achieves a maximum measured power consumption of 248 mW at 1 MHz.

Keywords Isolated gate driver (IGD) · Coreless · Common-mode transient immunity (CMTI) · Digital transformer · Duty cycle

1 Introduction

Several practical applications, such as data centers, motor drivers, solar inverters, telecommunications, and industrial automation, demand robust and highly efficient power electronic systems with sophisticated intelligence to meet the increasing power demands. Over the past decade, medium-voltage and high-voltage converters have evolved significantly, achieving notable improvements in performance [1–3]. Silicon (Si) power semiconductors and Wide bandgap (WBG) devices are extensively utilized in multi-level converters that operate with pulse width modulation (PWM) and rely on isolated high-side voltage supplies [4, 5].

Many on-chip active gate driver (AGD) designs have been reported before to drive the SiC MOSFET with various innovations. However, these designs often suffer form high power consumption, poor noise immunity [6, 7]. An AGD design using Differential Timing-Based Miller Detection (DTMD) improves accuracy and reduces level shifter losses via power gating, but still exhibits large rise/fall times [8, 9]. It is important to note that all our prior works in [6–9]

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focused exclusively on non-isolated AGD architectures, targeting power-reduction techniques, improved Miller detection, and buffer-array equalization, but none addressed the isolation interface, transformer design, or common-mode transient immunity (CMTI) robustness required for high-side gate driving. Thus, although effective within low-side environments, these earlier AGDs cannot be directly used in medium- and high-voltage systems that demand isolation.

Electrical isolation is essential in modern systems to protect human operators, prevent processor damage in high-voltage environments, eliminate ground loops in communication networks, and enable reliable communication with high-side devices in power converters and motor drives. Figure 1 shows a typical power drive system employing isolation [10]. CMTI is an important parameter to measure the isolator's ability to tolerate high-slew-rate voltage transients without corrupting signals [11].

Traditional circuits often use optically coupled drivers to achieve high-level isolation, which necessitates power isolation. However, these conventional gate drivers have drawbacks, such as bulky size and significant power consumption during current conduction. [12]. Capacitive isolation transmits signals via parallel-plate capacitors, supporting bi-directional communication and reducing channel requirements [13]. However, its performance is limited by sensitivity to high dv/dt noise and difficulty in handling low-frequency signals. Magnetic isolation uses primary and secondary coils, which can be cored or coreless, to transfer signals from controller to driver [14]. Coil-based transformers exhibit higher CMTI, making them more robust against dv/dt noise. Cored transformers provide better signal fidelity, while coreless designs are more compact and suitable for on-chip integration.

An IGD with a pulse polarity modulation scheme was reported [15], which was designed with discrete components and had a high propagation delay.

To address these limitations, and to overcome the absence of isolation capability in our earlier AGD works [6–9], this paper presents a fundamentally different contribution. We propose an isolated gate driver (IGD) that integrates a coreless, six-layer overlapping-coil digital transformer directly on silicon. The term "digital transformer" is used because the transformer does not transmit continuous analog waveforms. Instead, it conveys short-duration, edge-based pulses generated by switching events on the primary side. These pulses encode only the timing of rising and falling edges, not amplitude information. On the secondary side, a level shifter, Schmitt trigger, and control logic regenerate a clean digital waveform based solely on these transitions. As a result, the transformer functions as a digital isolator that transfers discrete switching edges rather than analog signal levels.

The proposed coil configuration consists of three interwound coil sets implemented across six metal layers. This arrangement achieves high coupling efficiency while occupying approximately the same area as a single-layer coil. The design is fabricated using the standard 0.18-μm high-voltage CMOS process (T18HVG2). The effectiveness of the high mutual inductance in the IGD is tested using CMTI between input V_{SOURSE} and V_G.

The key contributions of this work are summarized below:

- **A fully integrated digital-isolation architecture:** The proposed IGD incorporates a six-layer coreless transformer implemented entirely within a standard 0.18 μ m HV CMOS process, eliminating the need for external isolation components.
- **A compact multi-layer overlapping transformer design:** The transformer structure achieves high mutual inductance within a limited silicon footprint while ensuring robust CMTI performance.
- **On-chip bipolar and unipolar gate-drive capability:** The driver supports both 0 V to 5 V (unipolar) and −5 V to 5 V (bipolar) output modes without external HV MOSFETs.
- **High CMTI performance:** The design achieves a simulated CMTI of 155 V/ns and a measured CMTI of 5 V/ns (due to the limitations of instrument), demonstrating strong immunity to high dv/dt conditions.
- **Wide operating frequency and duty-cycle range:** The IGD operates reliably from 1 kHz to 5 MHz and supports duty cycles from 5% to 95% with accurate digital regeneration.
- **Experimental validation:** Full-chip measurements using a SiC MOSFET load confirm the robustness and practicality of the proposed architecture.

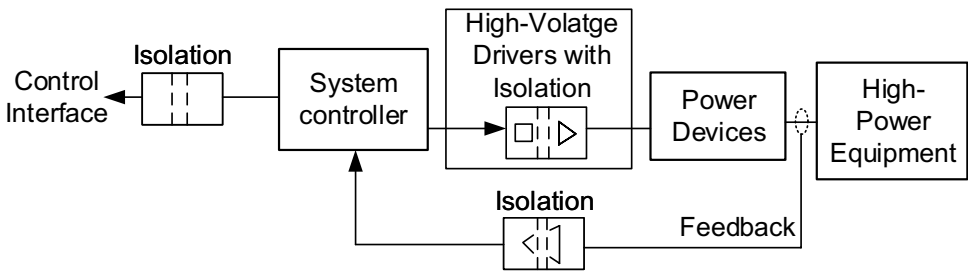
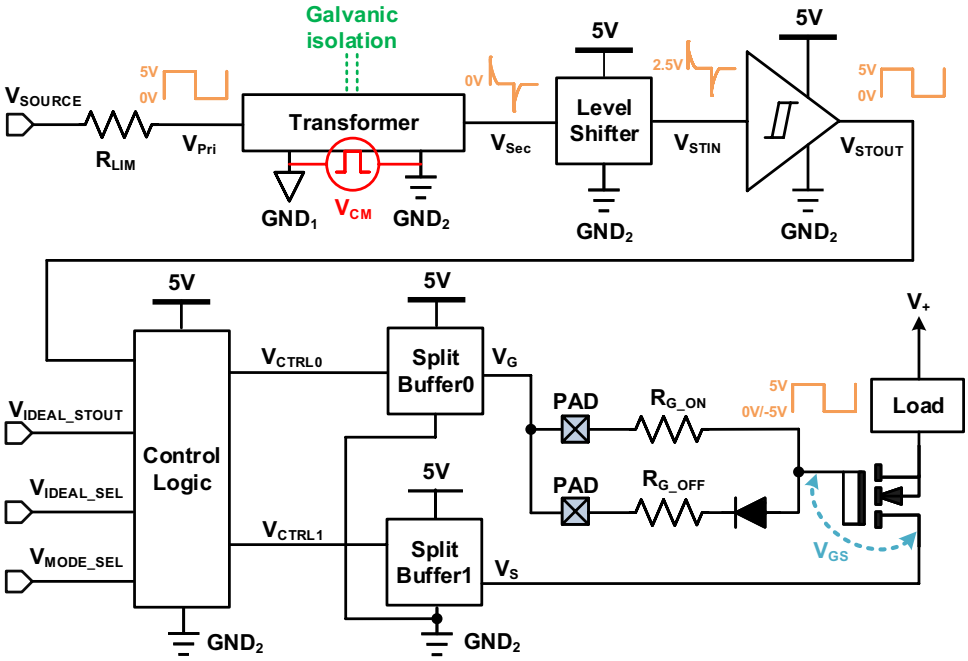


Fig. 1 Power drive system with typical isolation configuration [10]



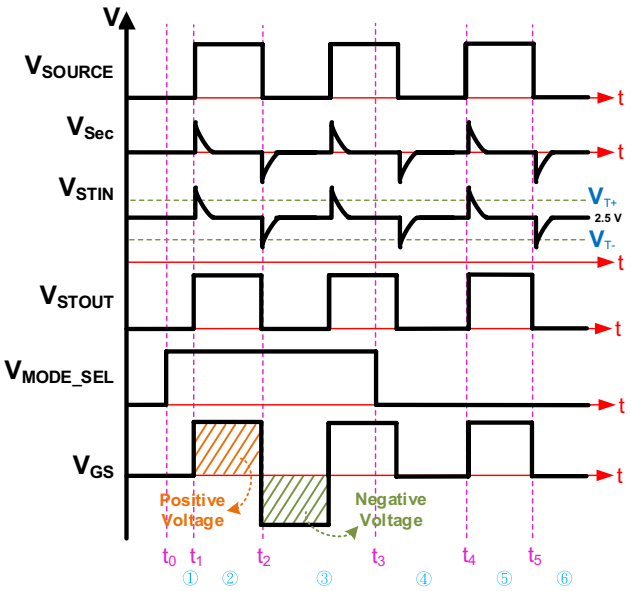


Fig. 2 System architecture of proposed isolated gate driver (IGD)

Fig. 3 Timing diagram of the proposed isolated gate driver

2 Design of the isolated gate driver (IGD) with transformer

The system architecture of the proposed isolated gate driver (IGD) with transformer is shown in Fig. 2. It integrates multiple functional sub-circuits to achieve isolated signal transmission and bipolar gate driving capability for power transistors. A low voltage digital input (for example, 5 V), denoted as V_{SOURCE}, is connected to a current-limiting resistor (R_{LIM}), which protects the circuit by limiting excessive current. The resulting voltage across R_{LIM} (V_{Pri}) is applied to the primary-side (low side) of a transformer, generating a corresponding secondary-side (high side) voltage (V_{Sec}). This design protects primary-side devices such as FPGAs and MCUs from being directly exposed to high-voltage surges that could otherwise propagate through wiring and cause damage.

The secondary-side voltage, V_{Sec}, is adjusted to the desired level using a Level Shifter, which is based on our previous works [6, 7]. By utilizing the Level Shifter, the DC noise in V_{Sec} is removed. Its signal shape is then restored by a subsequent Schmitt trigger circuit. The Control Logic determines whether the output operates in either unipolar or bipolar mode.

- When only the internal control signal V_{CTRL0} is activated, the Split Buffer0 is enabled, delivering a gate-driving signal ranging from 0 V to 5 V.
- When both the internal control signals V_{CTRL0} and V_{CTRL1} are activated, both Split Buffer0 and Split buffer1 are enabled, delivering a gate-driving signal ranging from −5 V to 5 V.

Finally, the generated digital signal will be transmitted via the Split Buffers, also based on our previous works [8, 9], and PADs to activate/deactivate the load and external power devices. The timing diagram of the proposed IGD is illustrated in Fig. 3, which can be divided into six phases:

- In Phase 1 (t_0 to t_1): During this stage, there is still no driving signal from V_{SOURCE}, so that the gate voltage (V_{GS}) of the power device remains at a logic low level.

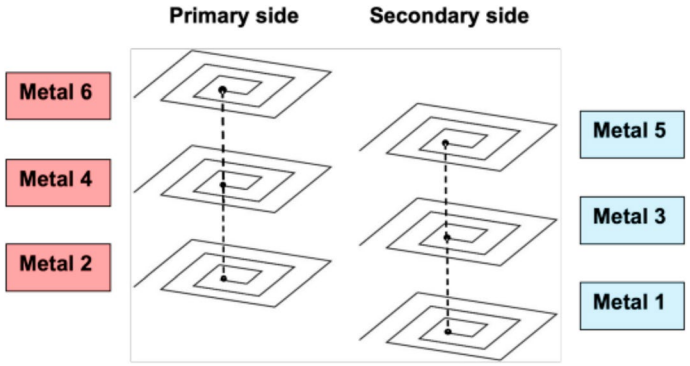


Fig. 4 Transformer with coil pairs designed with metal layers

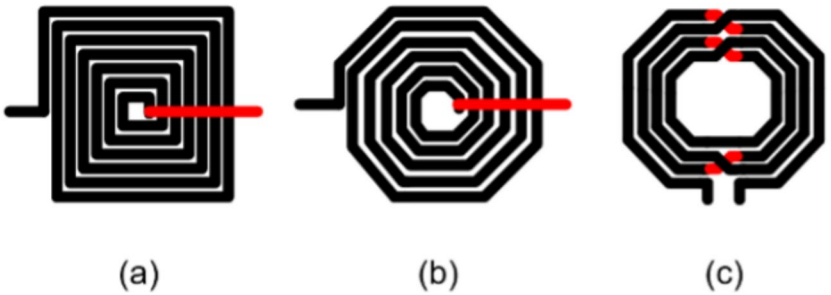


Fig. 5 Coil shapes (**a**) Square, (**b**) Octagonal, (**c**) Octagonal symmetric

Once the V_{MODE_SEL} signal is pulled high, the circuit enables Split Buffer1 and then proceeds to the next phase.

- In Phase 2 (t_1 to t_2): When V_{SOURCE} rises to a high level, the secondary voltage V_{Sec} induces a positive surge at the rising edge. The V_{STIN} signal is level-shifted to 2.5 V, and V_{STOUT} restores the waveform of V_{SOURCE}, resulting in an output gate voltage (V_{GS}) of 5 V.
- In Phase 3 (t_2 to t_3): When V_{SOURCE} falls to a low level, the secondary voltage V_{Sec} induces a negative surge at the falling edge. The V_{STIN} signal is again level-shifted to 2.5 V, and V_{STOUT} restores the waveform of V_{SOURCE}, producing an output gate voltage (V_{GS}) of –5 V.
- In Phase 4 (t_3 to t_4): At this moment, both V_{SOURCE} and V_{GS} remain at a logic high level. When the V_{MODE_SEL} signal is pulled low, the circuit disables Split Buffer1 and enters the next phase.
- In Phase 5 (t_4 to t_5): The operation is the same as in Phase 2, so that the output gate voltage (V_{GS}) is 5 V.
- In Phase 6 (t_5 to t_6): The operation follows the same sequence as Phase 3. However, since V_{MODE_SEL} is at a logic low level, Split Buffer1 is disabled, and the output gate voltage (V_{GS}) becomes 0 V.

2.1 Transformer

In this investigation, the proposed transformer is designed using six metal layers, which are available in HV CMOS process provided by the TSMC (T18HVG2). As shown in Fig. 4, metal layers 1, 3, and 5 are interwoven and connected through vias, forming the primary side of the transformer. Similarly, metal layers 2, 4, and 6 are interwoven and connected through vias to form the secondary side of the transformer. Different metal coil shapes on silicon are explored and reported as shown in Fig. 5. Prior to the realization of the coil pair, it is imperative to perform a series of simulations to ascertain the most suitable layout style for our design. Therefore, with an area boundary of 525 × 525 μm^2, a metal width of 20 μm, and a line spacing of 2 μm, the characteristics of the three different layout styles at 1 MHz frequency are summarized in Table 1. Among these, the Square layout is identified as the most favorable choice for maximizing inductance on silicon to ensure transmission quality.

Table 1 Characteristics of 3 on-chip coil shapes

	(a) Square	(b) Octagonal	(c) Octagonal symmetric
Inductance (nH)	10.4	4.13	3.63
Resistance (Ω)	16.79	12.92	9.92
Capacitance (pF)	1.18	0.79	0.89

2.2 Level shifter

Figure 6 illustrates the implementation of the Level Shifter in Fig. 2. The voltage level of sensed pulses from the coil pair is elevated to a higher level by the Level Shifter such that the following Schmitt trigger can correctly slice the pulses into a square wave train. In this work, the voltage level is elevated to 2.5 V from 0 V to prevent negative voltage coupled to the Schmitt trigger. Referring to the schematic in Fig. 6, it is implemented using a resistive voltage

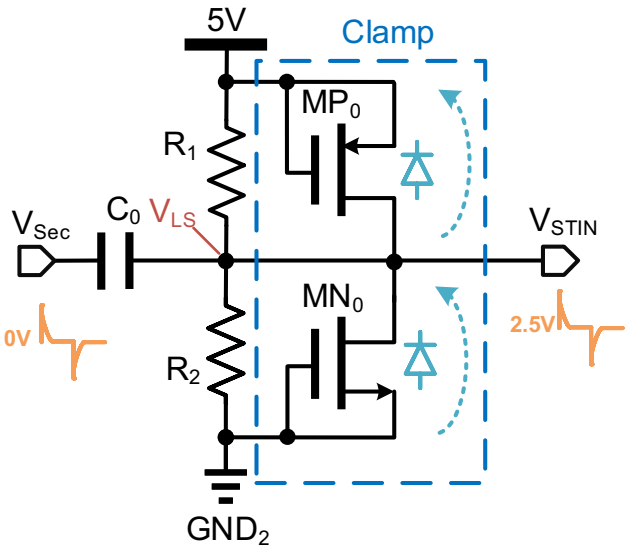


Fig. 6 Schematic of the Level Shifter

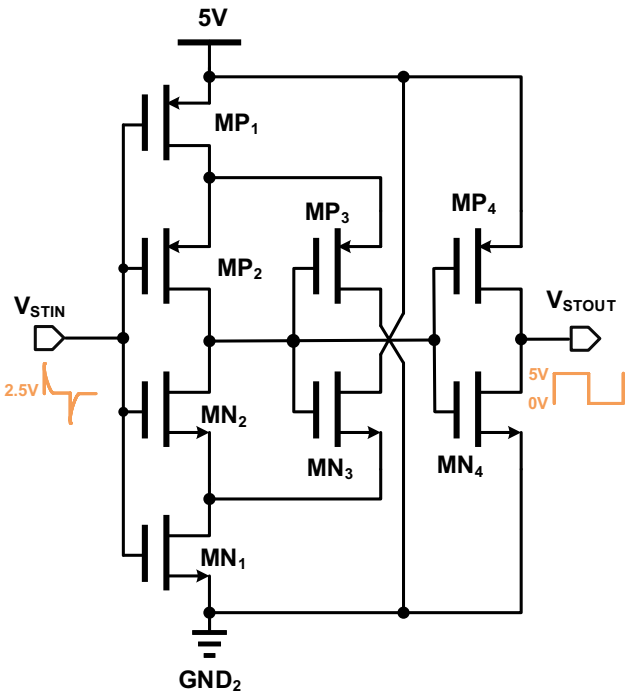


Fig. 7 Schematic of the Schmitt trigger [16]

divider. With R1 and R2 chosen to be identical, the supply voltage (VDD = 5 V) establishes a bias point of 2.5 V at node V_{LS}. To suppress undesired DC components coupled from the secondary-side signal (V_{Sec}), a coupling capacitor (C0) is placed before node V_{LS}, effectively blocking DC interference while preserving the AC signal content. Furthermore, to ensure reliable operation of the subsequent Schmitt trigger stage, transistors MP_0 and MN_0 inherently provide a diode-clamping function through their parasitic body diodes. This mechanism constrains the induced waveform within a safe voltage range, thereby mitigating the risk of overstress or functional degradation in the following circuitry.

2.3 Schmitt trigger

The Schmitt trigger, implemented using transistors MP_1–MP_3 and MN_1–MN_3, shown in Fig. 7 provides reliable waveform restoration. Transistor dimensions (width and length) are carefully optimized so that the positive and negative threshold voltages (V_{T+} and V_{T-}) effectively reshape the input signal (V_{STIN}), producing a clean inverted output. This output is subsequently converted back to an in-phase waveform using MP_4 and MN_4, ensuring accurate signal reconstruction for downstream circuitry. The use of a Schmitt trigger enhances noise immunity and sharpens signal transitions, which is critical for maintaining timing integrity in high-speed gate-driving applications.

2.4 Control logic

A control logic block is needed at the secondary side to take charge of output signal generation. The Control in Fig. 2 is revealed in Fig. 8. All the signals in said figure are briefed as follows.

1. V_{STOUT}: this input signal is generated by the previous stage, Schmitt trigger.
2. V_{IDEAL_STOUT}: this is an external input signal, used to run the direct testing of the secondary side functions. The selection signal is V_{IDEAL_SEL} to Mux0.
3. V_{MODE_SEL}: this is an external input signal, used to select whether V_{CTRL1} is a GND signal or the inverse of V_{ST}. When V_{MODE_SEL} is set high, Mux1 is enabled and V_{CTRL1} generates a –5 V signal, corresponding to bipolar operation and attains 10 V swing. Conversely, when V_{MODE_SEL} is low, Mux1 is disabled and V_{CTRL1} outputs 0 V, corresponding to unipolar operation and attains 5 V swing.
4. V_{CTRL0}, V_{CTRL1}: they are a pair of output signals to drive the Split Buffer0 and Split Buffer1, respectively.

Notably, the Dum Mux is meant to provide a delay for V_{CTRL0}, which is matched with that of Mux1 for V_{CTRL0}. Thus, the generation of V_{CTRL0} and V_{CTRL1} will be synchronized perfectly.

2.5 Split buffers

The schematic of Split Buffer is shown in Fig. 9, which is designed to introduce a dead-time interval during the switching transitions of the PMOS and NMOS buffer arrays. This

Fig. 8 Control logic

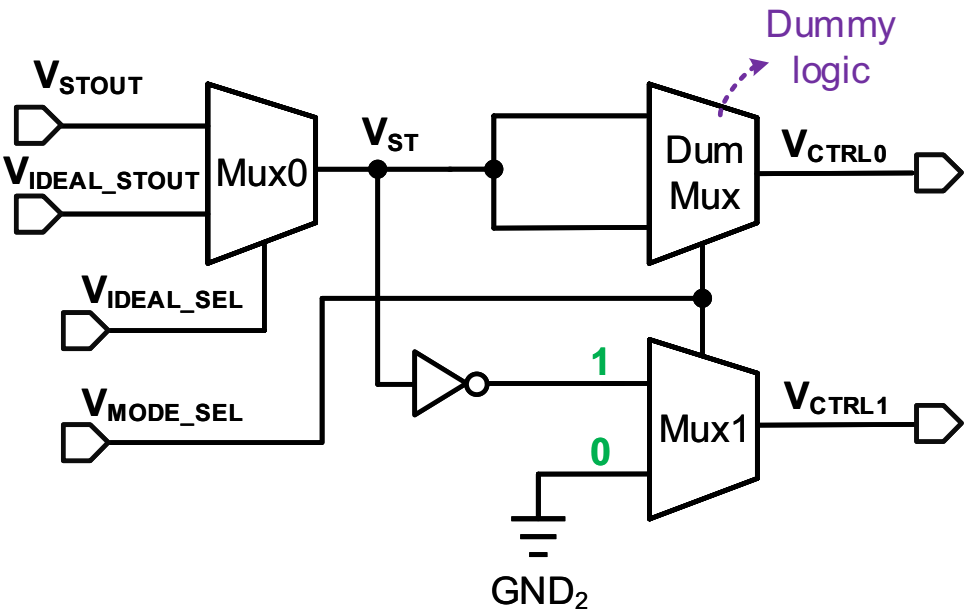
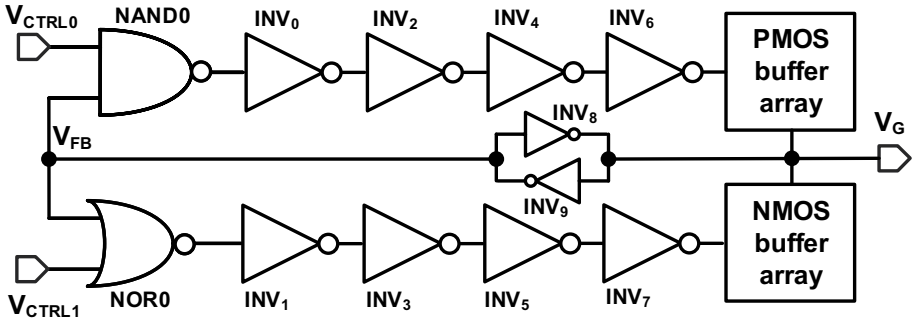


Fig. 9 Schematic of Split Buffers



mechanism prevents simultaneous conduction of both transistor arrays and thereby eliminates shoot-through current.

When V_{CTRL0} transitions from 0 to 1, the output of NAND0 switches to 1 and then pulls down to 0. Consequently, INV6 outputs a logic 0, turning on the PMOS buffer array, which drives the gate node (V_G) to logic 1. At this point, the feedback signal (V_{FB}) is also set to 0, forcing NAND0 to switch from 0 to 1. This in turn causes INV6 to output a logic 1, effectively disabling the PMOS buffer array. However, the logic state of V_G remains latched at logic 1 by inverters INV8 and INV9, ensuring output stability.

Conversely, when V_{CTRL0} transitions from 1 to 0, the output of NOR0 switches to 0 and then pulls up to 1. As a result, INV7 outputs a logic 1, enabling the NMOS buffer array. The feedback signal (V_{FB}) simultaneously switches to 1, causing NOR0 to change its output from 1 to 0. This forces INV7 to output 0, thereby disabling the NMOS buffer array. In this case, the logic state of V_G is latched at 0 by INV8 and INV9, again maintaining a stable output.

Through this feedback-controlled dead-time generation, the circuit effectively prevents the PMOS and NMOS buffer arrays from being activated simultaneously, thereby avoiding shoot-through and improving power efficiency and reliability of the gate driver.

3 Simulation and on-silicon measurements

The layout and die photo of the proposed IGD, fabricated using the 0.18-μm HVCMOS, are shown in Fig. 10. The overall chip area is 1980 μm × 1580 μm and the core area is 1514.96 μm × 1205.36 μm. The measured maximum power consumption is 248 mW at an input frequency of 1 MHz.

Figure 11 shows the simulation results of the proposed IGD circuit under various PVT (Process, Voltage, and Temperature) conditions. The supply voltage was varied at VDD = 5.5 V, 5 V, and 4.5 V, and simulations were conducted across multiple process corners (FF, FS, TT, SF, and SS) as well as at three operating temperatures (−25°C, 25°C, and 125°C). The IGD demonstrated stable operation at an input frequency (V_{SOURCE}) of 1 MHz during these simulations.

The measurement setup used to evaluate the IGD is depicted in Fig. 12. A Keysight EDU36311A programmable power supply was utilized both as the system power source and for power consumption monitoring. A Keysight 33600A

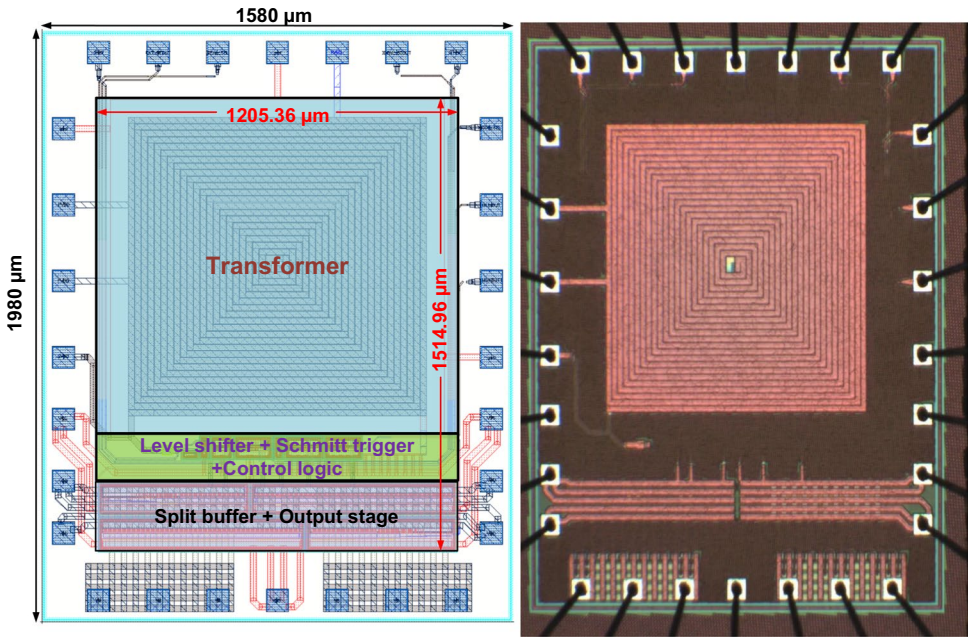


Fig. 10 Layout and die photo of the proposed IGD

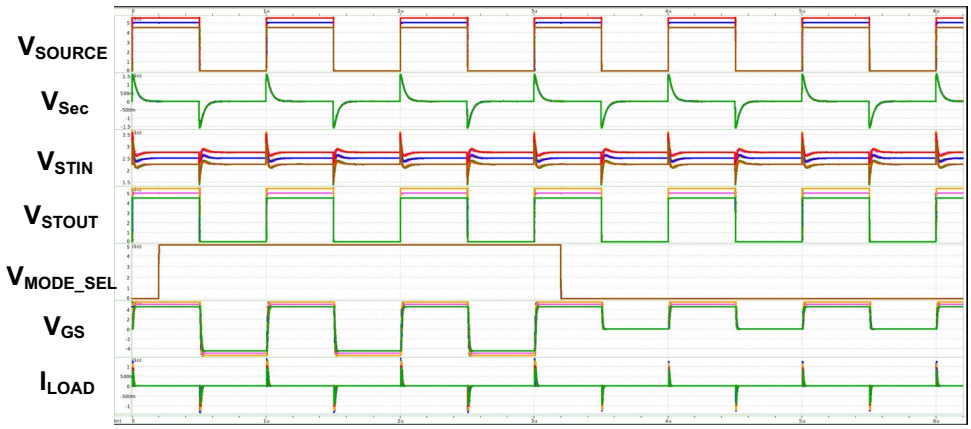


Fig. 11 Post-layout simulation results of the proposed IGD at all-PVT corners

waveform generator provided the input signal V_{SOURCE}, while a Wavesurfer 3104z oscilloscope was employed to capture the output gate waveform V_{GS}. The inputs to the chip consist of the V_{SOURCE} and V_{MODE_SEL} signals. Once the measurement environment was established, performance evaluation was carried out by supplying V_{SOURCE} and configuring V_{MODE_SEL} to select between unipolar and bipolar output modes. All measurements were carried out when the proposed IGD was driving a Infineon SiC MOSFET (IMW65R048M1H). This setup enabled comprehensive validation of the chip's functionality and performance characteristics.

As described in the introduction, both CMTI simulations and measurements were conducted to test the proposed IGD, with the results presented in Figs. 13 and 14. The CMTI simulation indicates a maximum tolerable common-mode rate of 155 V/ns, corresponding to the rise or fall voltage between the primary and secondary sides. In contrast, the CMTI measurement demonstrates a tolerance of 5 V/ns, which is constrained by the upper limit of the measurement instrument (Keysight 33600A).

Figures 15 and 16 show the obtained output V_{GS}, measured at various V_{SOURCE} frequencies, confirming that the proposed IGD operates effectively over a frequency range of 1 kHz to 1 MHz. To test the limits of the designed IGD, the work is tested at an operating frequency of 2 MHz to 5 MHz, as shown in Figs. 17 and 18. Figures 19 and 20 illustrates the IGD's ability to regenerate an input signal with varying duty cycles (5%∼95%) at a frequency of 1 MHz, successfully producing the output V_{GS}.

Figure 21 shows the propagation delay from V_{SOURCE} to V_G is measured as 23 ns and 24 ns at low-to-high and high-to-low transitions, respectively.

Figure 22 present the measurement results of the IGD under unipolar and bipolar output modes. The results demonstrate that the proposed driver is capable of reliably driving

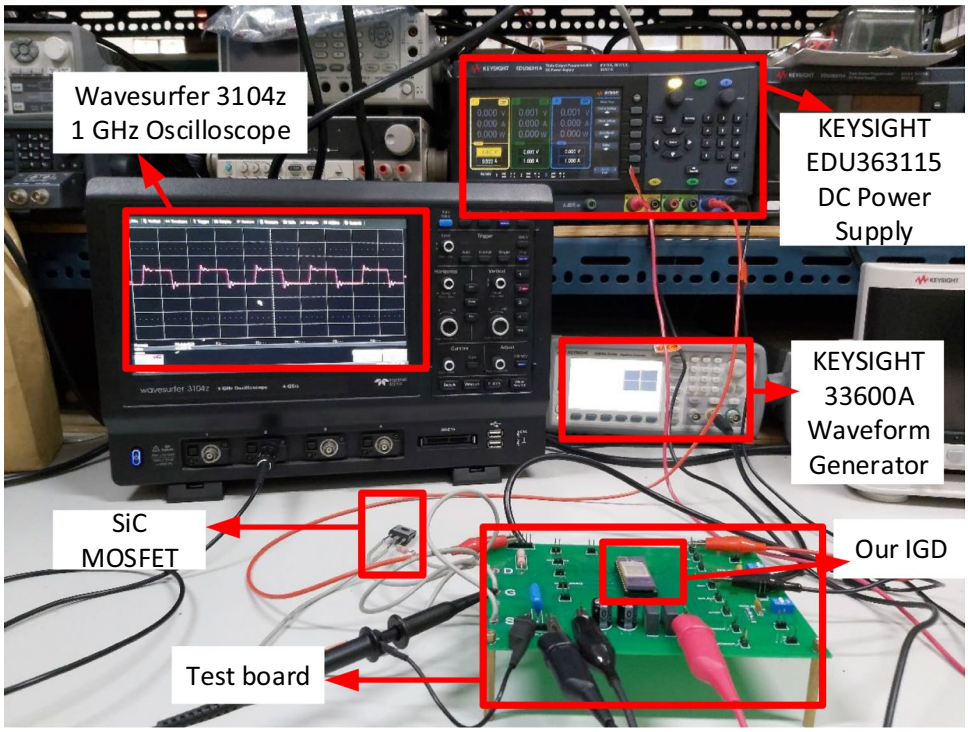


Fig. 12 Measurement environment

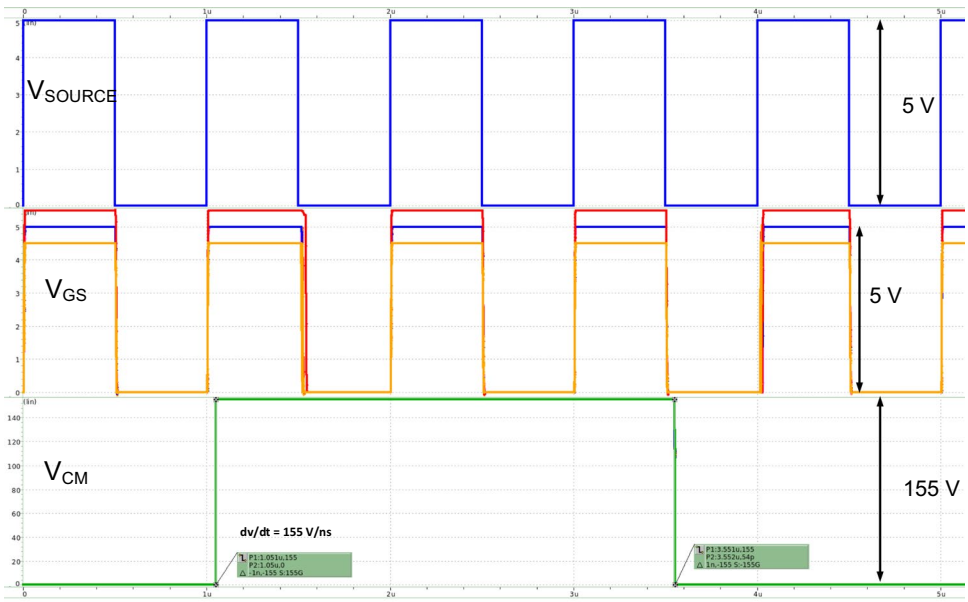


Fig. 13 CMTI simulation of IGD

the power transistor load in both configurations. This confirms the circuit's flexibility and robustness across different operating modes, validating its suitability for diverse power switching applications.

The simulation and measurement results confirm the anticipated performance of the proposed IGD, validating its design and functionality. To demonstrate the superiority of the proposed design, we compare several recent works, namely state of the art, in Table 2. As highlighted in Table 2, our driver not only attains the edge of speed (short propagation delay and high clock rate), it also shows that a single chip without any HV MOSFET is feasible. This is never been reported before. On top of these advantages, there is also no need for any additional components.

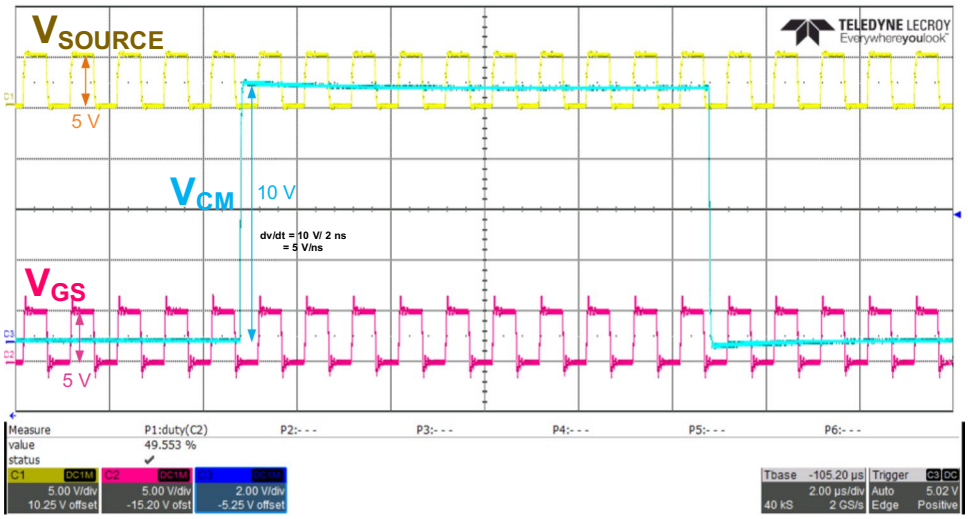


Fig. 14 CMTI measurement of IGD

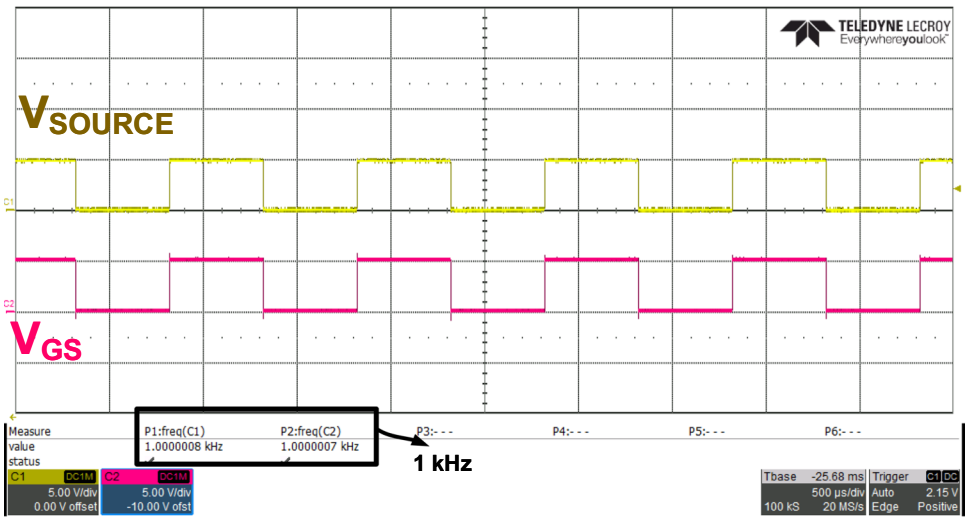


Fig. 15 Output V_{GS} measurement at 1 kHz input V_{SOURCE} frequency

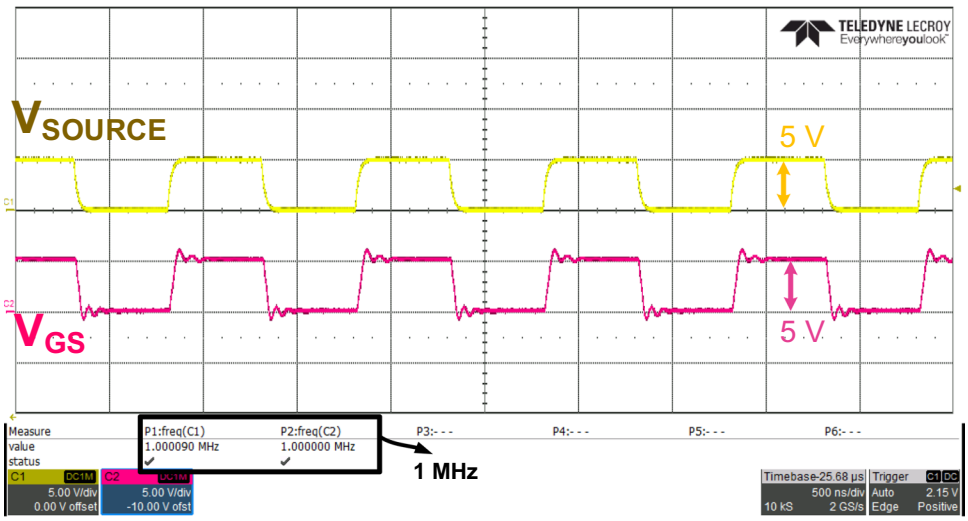


Fig. 16 Output V_{GS} measurement at 1 MHz input V_{SOURCE} frequency

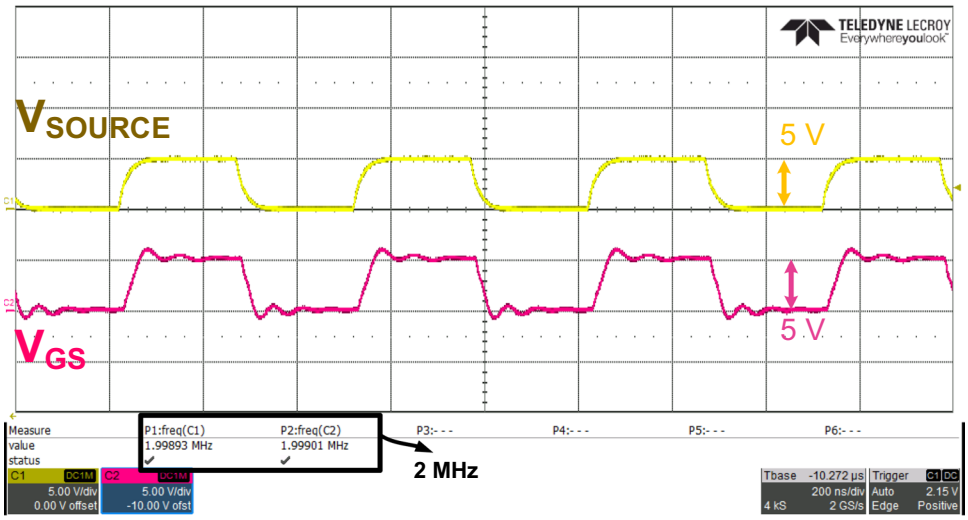


Fig. 17 Output V_{GS} measurement at 2 MHz input V_{SOURCE} frequency

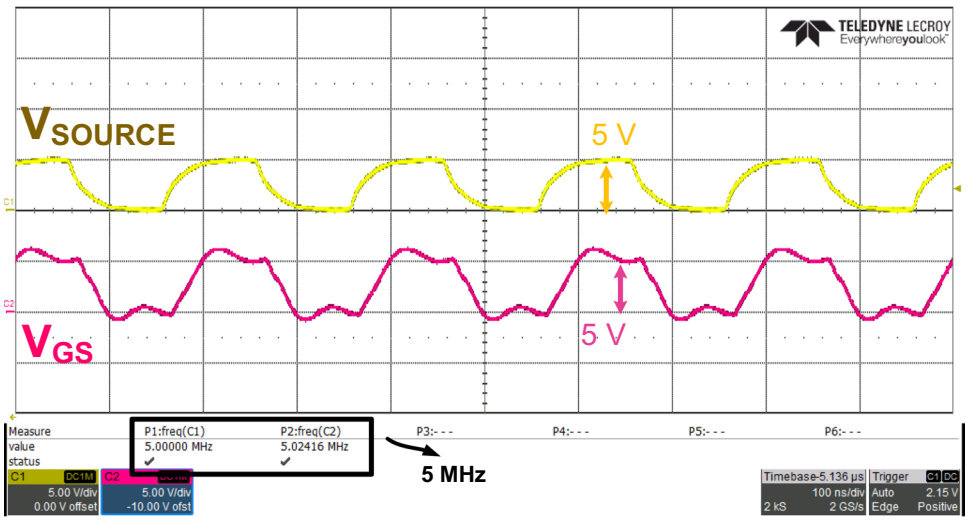


Fig. 18 Output V_{GS} measurement at 5 MHz input V_{SOURCE} frequency

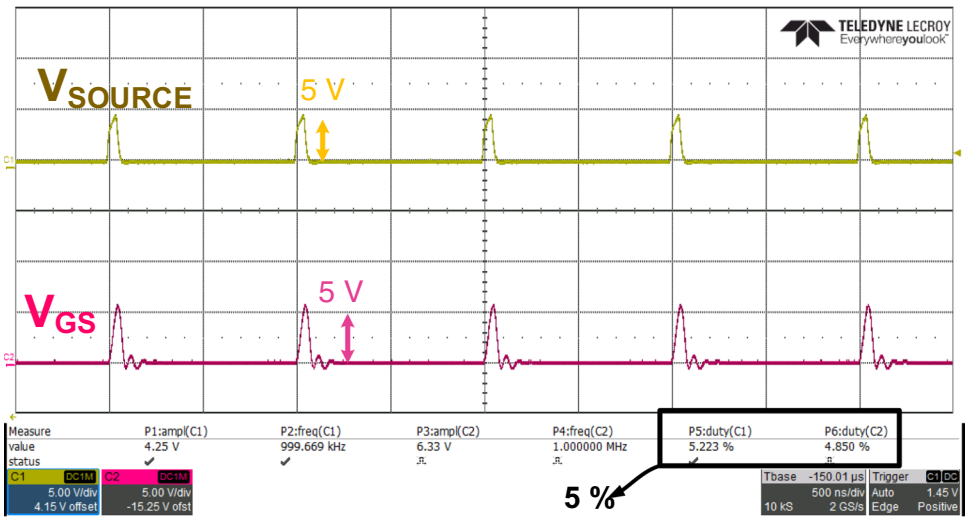


Fig. 19 Different duty cycles @ 1 MHz, 5%

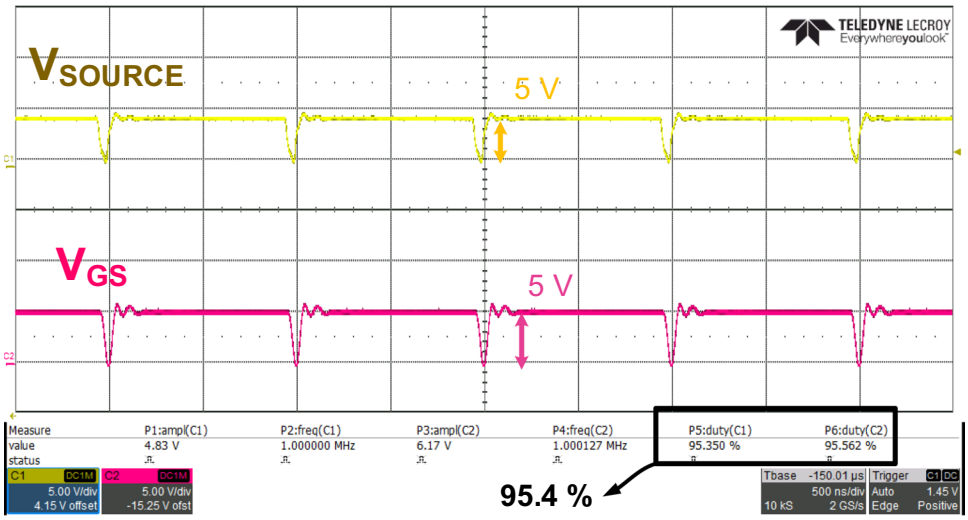
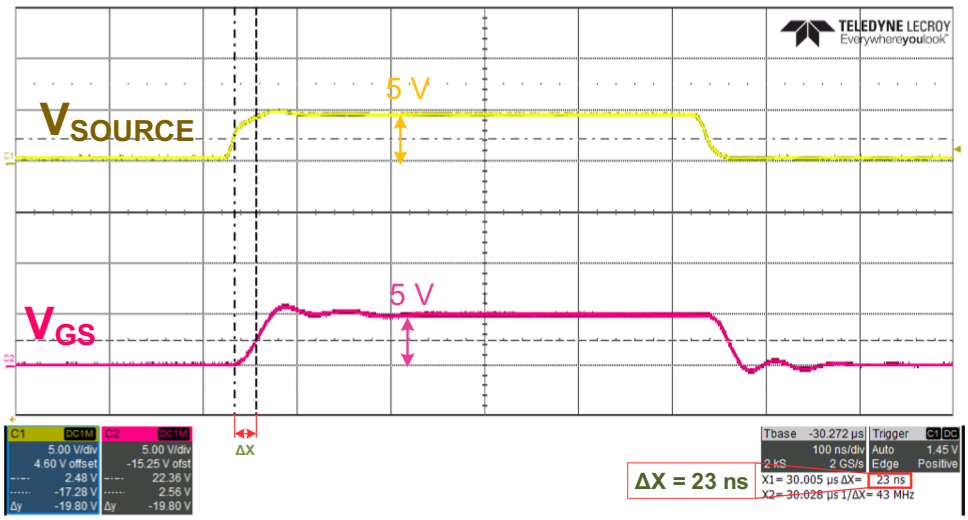
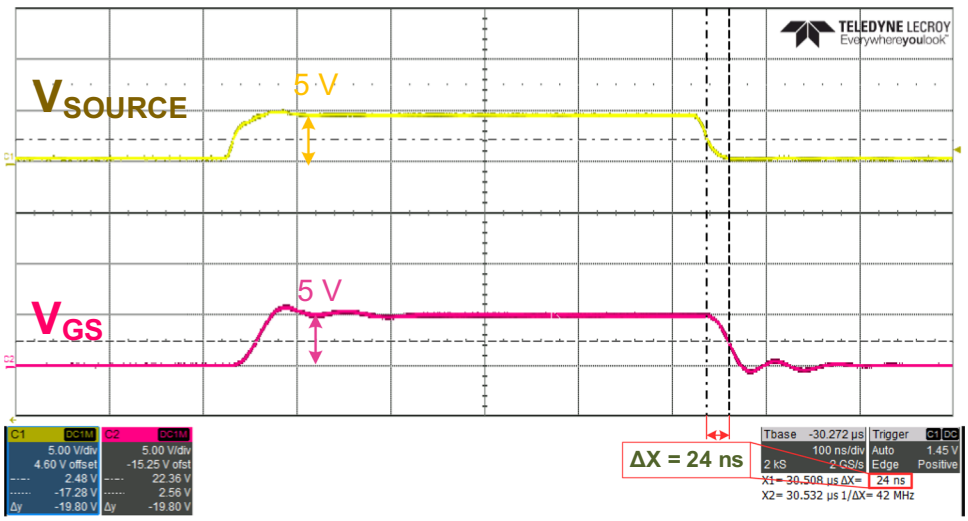


Fig. 20 Different duty cycles @ 1 MHz, 95.4%



(a)



(b)

Fig. 21 Propagation delay, (**a**) Low-to-high; (**b**) High-to-low

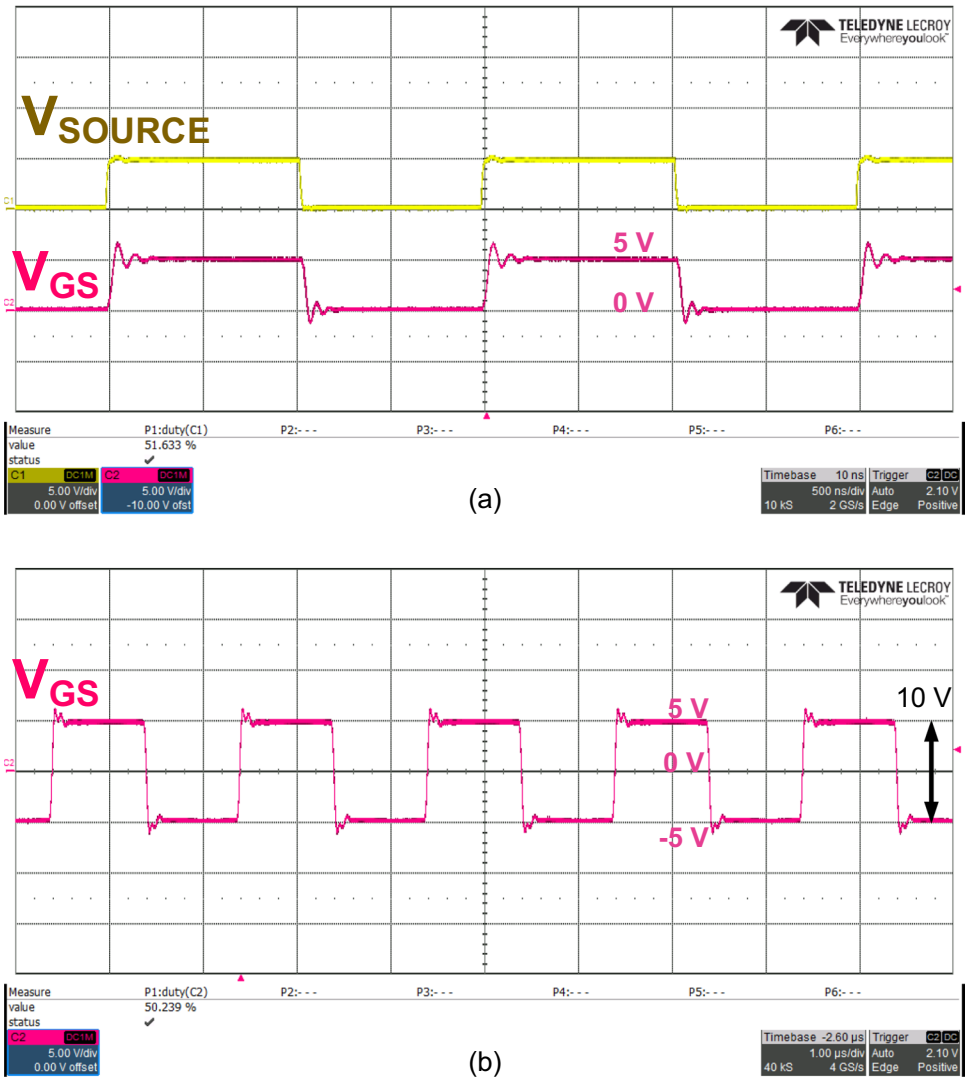


Fig. 22 Measurement results of the IGD under (**a**) unipolar and (**b**) bipolar output modes

Table 2 Performance comparison with state of the art

	[17]	[3]	[4]	[15]	[18]	[19]	This work
Year	2015	2020	2021	2022	2023	2024	2025
Publication	TI Data sheet	ECICE	TPE	IJESTPE	ESSCIRC	L-SSC	
Process (nm)	N/A	180	Discretes	Discretes	250	180	180 T18HVG2
Supply voltage (V)	5.5	5	+15/−5	10	3.3, 5.5	5	5
Isolation barrier	Capacitor	Transformer	Transformer	Transformer	Transformer	Capacitor	Transformer
Modulation architecture	Pulse polarity	OOK	Pulse polarity	Pulse polarity	OOK	OOK	Pulse polarity
PWM range	–	50%	–	15% to 90%	–	–	5% to 95%
Area (mm^2)	–	–	–	–	–	–	3.13
Operating frequency (Hz)	500 k	100 k	300 k	500 k - 1 M	–	500 M	1 M
Propagation delay (ns)	76	250	–	180	–	5.2	24
CMTI (V/ns)	100	–	20	50	150	100*	155 **

* CMTI in simulations

** This is post-layout simulation CMTI and the maximum measurable CMTI value by the instrument is 5 V/ns (Keysight 33600 A)

4 Conclusion

The proposed IGD employs a coreless, six-layer overlapping coil structure integrated into a digital transformer on silicon. This innovative design achieves high mutual inductance within a compact footprint, ensuring excellent performance while maintaining isolation. Both simulation and measurement results validate the IGD's capability to handle high CMTI, with tolerances up to 5 V/ns in measurements and a simulated maximum rate of 155 V/ns. Furthermore, the IGD demonstrates robust functionality across a wide frequency range (1 kHz to 5 MHz) and supports unipolar and bipolar signal operation, with a maximum power consumption of 248 mW at a 1 MHz input signal.

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Author contributions Pradyumna Vellanki and L S S Pavan Kumar Chodisetti take charge of writing the text. Yun-Che Chang is in charge of layout design. Prof. Chou provide the measurement facility. Prof. Chua-Chin Wang is the leader of the power IC project.

Data availability No datasets were generated or analysed during the current study.

Declarations

Competing interests The authors declare no competing interests.

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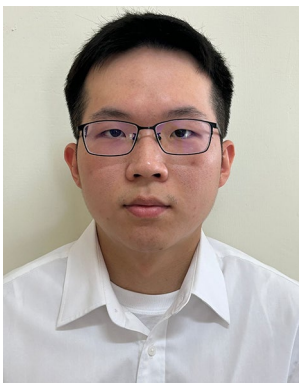
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