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A 1.22 fJ/bit/Search Shared BL/SL Single-Ended 32×32 CAM Using 40-nm CMOS Process

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***Abstract*—This paper presents a fully integrated, energy-efficient 32 × 32 content addressable memory (CAM) based on single-ended memory cells to realize an access and search architecture with a shared bit-line and search-line (BL/SL). Traditional CAMs depend on differential bit-lines and search-lines, which introduce excessive routing capacitance, power consumption, and redundant switching activity. To address these issues, the proposed design combines read, write and search signaling into a single physical line and adopts single-ended operation throughout the write, read, and search modes. A dynamic voltage scaling (DVS) controller manages local supply voltage at the column level for each CAM cell to reduce standby leakage power, while a regenerative sense amplifier (Re-SA) aids full-swing match line sensing under low-voltage operation. Furthermore, an on-chip built-in self-test (BIST) architecture is also integrated to improve observability, controllability, and silicon validation efficiency. The proposed CAM is implemented using TSMC 40-nm CMOS technology and confirmed through post-layout simulations and silicon measurements. Measurement results validate the correct read, write, and search functionality of the proposed CAM at a 0.9-V supply voltage, with the fabricated prototype exhibiting a total chip power dissipation of 6.14 mW. It achieves a measured energy efficiency of 1.22 fJ/bit/search with a search time of 2.16 ns at a 20-MHz clock frequency. These findings validate the proposed CAM as an energy-efficient solution for lookup-intensive and power-constrained applications.**

***Index Terms*—Content addressable memory (CAM), single-ended cells, shared bit-line/search-line (BL/SL), dynamic voltage scaling (DVS), regenerative sense amplifier (Re-SA), low-voltage operation, built-in self-test (BIST), energy efficiency, silicon measurement.**

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I. Introduction

MODERN computing systems require fast and deterministic data retrieval to satisfy increasingly stringent latency and performance requirements [1]. Most conventional memory architectures rely on sequential search making them suitable for high-speed lookup applications such as cache tag matching, translation lookaside buffers (TLBs), network routing, data search for Artificial Intelligence (AI) and pattern recognition [2], [3]. Intrinsic parallelism is commonly used in high-performance systems, since it reduces search latency compared to conventional ones [4], [5].

Content Addressable Memory (CAM) is well suited for high-speed lookup applications because it performs single-cycle searches by comparing input data against all stored entries in parallel [6]. However, this fully parallel operation presents significant challenges: high dynamic power consumption results from repeated charging and discharging of highly capacitive bit-lines (BLs) and match-lines (MLs), while conventional differential signaling increases routing complexity and switching activity [7].

Despite recent improvements, leakage currents in large arrays, frequent BL/ML transitions, and energy overhead from precharge procedures still make conventional CAMs power-hungry. These limitations hinder the adoption of CAMs in low-power system designs, limit scalability, and increase energy consumption. As a result, CAM architectures that accomplish high-speed searches while enhancing array scalability and energy efficiency are desperately needed. Many low-power CAM design techniques have been proposed to overcome these issues, with notable advantages:

- **Decreased Dynamic Power:** Techniques that eliminate the switching activity and unwanted voltage transitions during searches, thereby lowering overall energy usage while maintaining reliable and high-speed operation.
- **Improved Energy Efficiency:** Strategies that remove unnecessary precharge and discharge processes lower overall energy consumption when doing searches.
- **Enhanced Scalability:** Techniques like shared line architectures and simpler signaling allow dense CAM arrays with reduced connection overhead and routing complexity, enabling scalable high-performance systems.

To overcome these obstacles, a variety of low-power CAM design techniques have been reported. The two traditional

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CAM cell topologies, NOR-type and NAND-type [8], provide complementary trade-offs. High-speed memory access is made possible by NOR-type CAMs, but they also consume more energy because match lines account for the majority of the overall power. Folded match-line topologies with charge recycling help to lower this overhead without compromising performance [9].

However, hybrid CAM architectures use local NOR-global NAND partitioning [10], segmented NAND-to-NOR activation [11], and pulsed NAND–NOR evaluation [12] to exploit their complementary strengths. A MLCU-based hybrid CAM uses NAND mismatch detection to reduce redundant NOR activity and offer a short discharge path to lower match-line switching activity [13]. Moreover, a hybrid CAM with NOR–NAND match lines, pre-charge-free operation, and facilitating localized search mechanisms achieve higher energy efficiency and increase search frequency [14].

A precharge-free CAM (PCAM) employs segmented match-line evaluation, local search, and selective discharge paths to perform comparisons rather than precharging the match lines prior to each search [15]. Based on this, a pseudo-precharge-free CAM (PPFC) is proposed that addresses low search speed and erroneous outputs in existing precharge-free CAM designs by employing NAND cells in the middle of each row to truncate the interconnect length and improve the overall performance [16]. The Self-Controlled High-Performance Precharge-Free (SCPF) CAM further eliminates precharge and inter-cell dependencies, minimizing match-line latency and enlightening search capabilities, but the power consumption during search operations remains a challenge [17].

Moreover, adaptive ML discharge designs with selectively gated pull-down routes, ML boosting, and timing calibration have been shown in previous research to minimize ML swing and redundant SL switching, leading to notable gains in delay and energy [18]. Notably, by removing DC current channels with the aid of charge domain, 3T1R1C RRAM-based TCAM cells offer parallel, energy-efficient search operations [19]. Techniques such as Noise-tolerant XOR-based conditional keepers [20], two-bit CAM cells with shared match-line schemes (SMS) [21], selective-charging and adaptive-discharging (SCAD) dynamic match-line architectures [22], and Hamming distance-tolerant CAMs (HD-CAM) [23] were introduced to reduce match-line transitions, optimize energy efficiency, and support approximate searches.

Furthermore, many previous research reports have shown that dynamic storage-based CAM architectures optimized for large-scale similarity search in computational genomics [24] and high-performance compute-SRAM designs utilizing multirow activation and disturbance-aware circuit techniques [25], [26] offer an efficient way to boost in-memory search efficiency and computational throughput, complementing the developments in precharge-free CAM architectures.

Moreover, contemporary AI accelerators, networking systems, and data-oriented computing architectures require substantial search throughput to facilitate real-time data processing [2], [3]. To meet these throughput demands, current high-performance CAMs are usually run at elevated clock frequencies, which leads to higher dynamic power consumption from the frequent switching of search lines, match lines, and sensing circuits [18]. Moreover, many CAM architectures still depend on specific search-line routing and precharge methods [6], [17], leading to considerable interconnect energy costs and heightened circuit complexity. While earlier research has enhanced distinct design elements, such as reducing match-line switching [9], eliminating precharge [15], and facilitating low-voltage sensing [18], the concurrent optimization of search energy, standby leakage, routing overhead, sensing reliability, and search latency in compact CAM arrays continues to be a significant research challenge [3].

This study presents a unified single-ended CAM architecture using a shared bit-line/search-line (BL/SL) topology to address the aforementioned issues. By eliminating the requirement for particular search-line routing and using a single physical interconnect for write, read, and search functions, the proposed design reduces interconnect capacitance, switching activity, and circuit complexity. In particular, column level dynamic voltage scaling (DVS) minimizes standby leakage of the 10T CAM cell and the regenerative sense amplifier (Re-SA) provides reliable low-voltage sensing. The proposed architecture reduces search latency, enabling the CAM to achieve the required search throughput at a lower operating frequency while reducing dynamic power consumption. Therefore, without compromising search performance, the proposed solution reduces dynamic power consumption and improves overall energy efficiency.

The key contributions of this work can be outlined as follows:

- **Shared BL/SL Single-Ended Architecture:** Unifies read, write, and search functions onto a single physical line.
- **Dynamic Voltage Scaling (DVS):** Lowers standby leakage.
- **Regenerative Sense Amplifier (Re-SA):** Provides dependable low-voltage sensing.

The proposed 32×32 CAM prototype in 40-nm CMOS is validated by post-layout simulations and silicon tests.

II. Shared BL/SL CAM Architecture and Operations

Fig. 1 illustrates the overall architecture of the proposed 32×32 CAM, consists of column decoder, row decoder, bit controller, DVS assisted 32×32 CAM array with Regenerative Sense Amplifiers (Re-SA), Match Arbitration Encoder (MAE), column selector with output buffer and Built-In Self-Test (BIST) circuit. The proposed approach reduces interconnect overhead and switching activity by combining memory access with associative search over a shared BL/SL lines, in contrast to previous single-ended CAM systems that maintain discrete search-line routing. With the use of DVS-assisted sensing, controlled precharge and evaluation phases, coordinated row/column decoding, and effective match-line resolution, the architecture allows for high-speed and energy-efficient associative search.

Column-level access is achieved by decoding Word_Addr [4:0], where the column decoder generates WA [31:0] and the row decoder activates the corresponding row through BA [31:0].

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TABLE I

SIGNAL SUMMARY OF THE PROPOSED 32 × 32 DVS-ASSISTED CAM

Signal	Name	Description
Global Control and Addressing Signals		
V_{DD}	Supply voltage	provides the power supply to the CAM array through DVS controller and other peripherals.
V_{DDS}	Local Supply Voltage	Provides regulated local voltage from the DVS controller to the CAM array.
Word_Addr[4:0]	Column Address	A 5-bit input that selects column j in the CAM array, allowing data access for read/write operations.
Bit_Addr[4:0]	Row Address	A 5-bit input that selects row i in the CAM array, used for targeting specific rows for operations.
Wr_En	Write Enable	Activates the write operation, allowing data to be written to the selected CAM cell in the array.
SA_En	Search/Read Enable	Enables the regenerative sense amplifiers, crucial for conducting search or read operations.
SA_Pre	Search Precharge	Precharges the sense amplifiers before performing a search operation, optimizing the search speed.
Row and Column Decoding Signals		
WL[i]	Word Line	Activates the word line for row i during write,read and or search operations to select the target row.
BA[i]	Row Select	Decoded output selecting the specific row i within the CAM for accessing or writing data.
WA[j]	Column Select	Decoded output that selects column j within the CAM, enabling data access or modification.
WD[j]	Data Control	Active during the write,read and search operations, disabled in standby.
WH[i]	Write Header	Enables the write path for row i during write operations, ensuring proper data storage.
Match-line and Sensing Signals		
PRE[i]	Precharge	Precharges the Bit line/search line for row i, preparing it for comparison during search operations.
BL/SL[j]	Bit/Search Line	A shared line used for both reading data and performing search operations in column j.
SD[i]	Search Data	1-bit search data for row i, used in comparison during the search operation for matching.
Match	Global Match	A signal that is asserted when at least one row matches the target data, indicating a successful search.
MA[31:0]	Match Address	A 32-bit encoded address representing the row index of the matching entry within the CAM array.
Output and Data Path Signals		
Bit[4:0]	Bit Select Address	A 5-bit address used to select the specific bit position for matching between the CAM and the target.
Data_out	Output Data	The final buffered output from the selected CAM cell, representing the matched data.
Built-In Self-Test (BIST) Signals		
BIST_En	BIST Enable	A signal that enables the Built-In Self-Test operation, allowing the CAM to perform self-diagnostics.
BIST_Word[4:0]	BIST Word Address	A 5-bit input that selects the word line under test in the CAM array during BIST operation.
BIST_Data[4:0]	BIST Data Input	A 5-bit input that provides test data to the selected CAM word during BIST operation.
BIST_Pass	BIST Flag	A flag indicating successful completion of the BIST process, signaling the test's pass status.

**Note:* i is the CAM row index (0–31) selected by Bit_Addr[4:0], and j is the CAM column index (0–31) selected by Word_Addr[4:0].

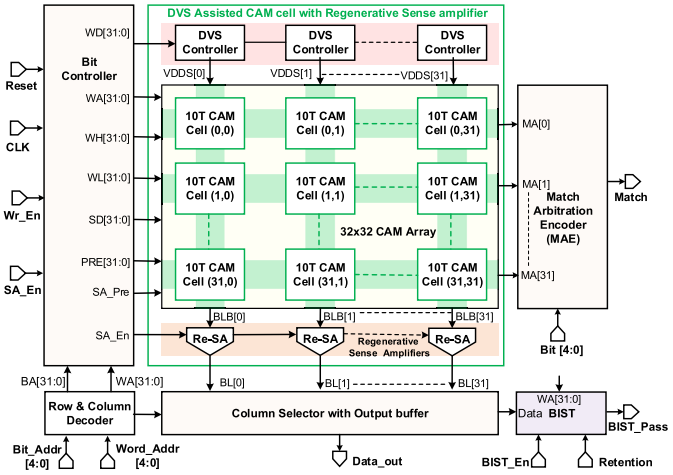


Fig. 1. Proposed block diagram of the 32 × 32 CAM architecture.

The bit controller receives decoding signals as well as control inputs like CLK, Reset, Wr_En, SA_En and BIST_En and generates the necessary timing and control signals, such as WD[31:0], WH[31:0], WA[31:0], PRE[31:0], and SD[31:0], depending on the operation mode chosen (write, read, search, and BIST). Each operating modes follows distinct sequence of operations coordinated by control signals as summarized in Table I.

During **Write cycle** as shown in Fig. 2(a), a 32-bit CAM word [i,j] is written by synchronizing with the clock's rising edge (CLK).

1) The internal nodes are precharged by PRE[i] during the precharge phase, creating consistent initial conditions.
2) The target CAM word [i,j] is chosen during activation by WL[i] and WH[i], and the write is enabled by Wr_En and WD[j]. Under lower supply voltage (V_{DDS}), the write-assist signal WA[j] improves write reliability.
3) In the evaluation phase, WD[j] can program Word_Addr[4:0] of the CAM word [i,j], which within a predetermined window settles to WL[i].
4) When PRE[i] is deasserted, Word_Addr[4:0] keep the intended 32-bit data, but CAM cells are typically idle.

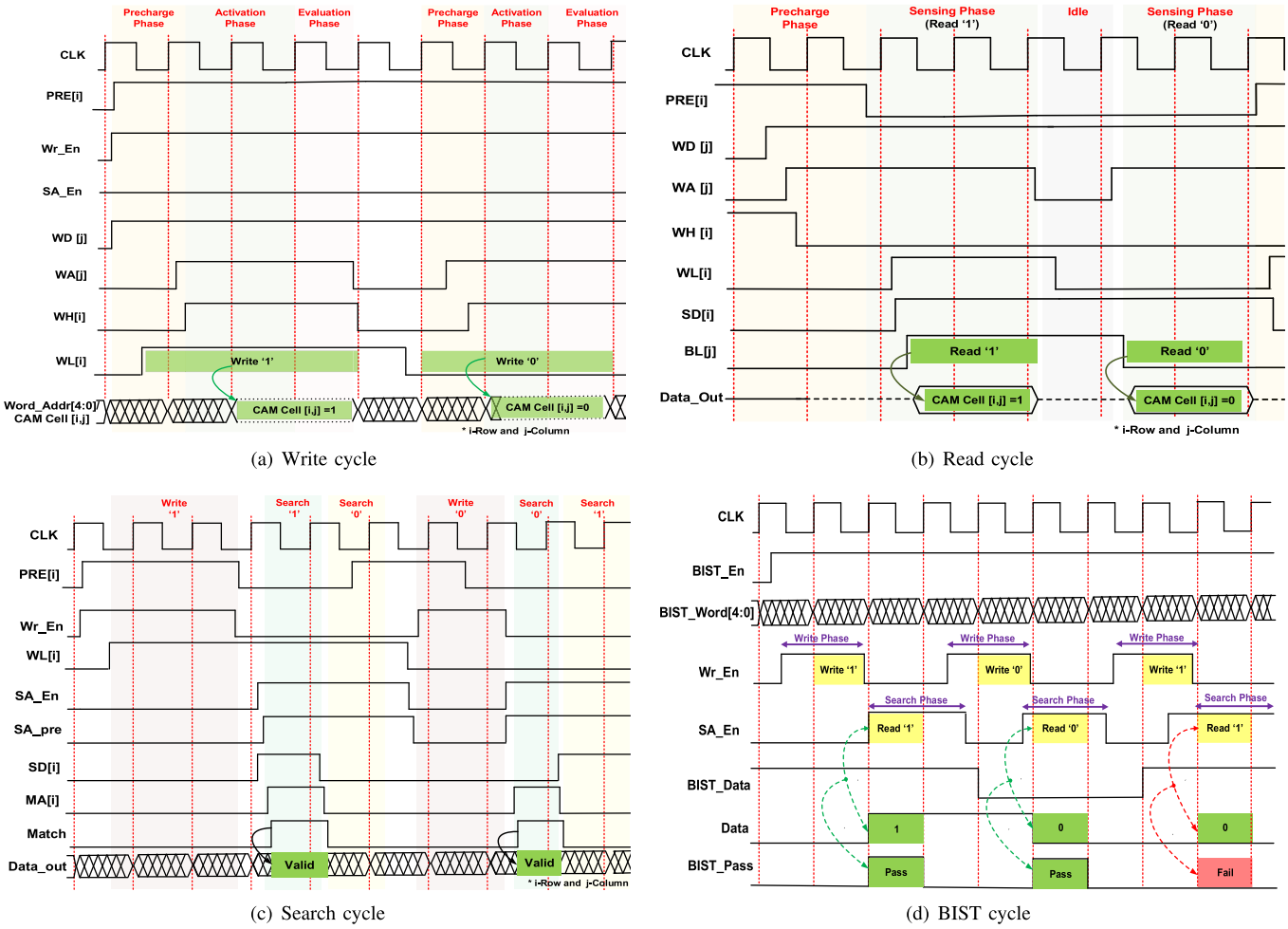
During **Read Cycle** as shown in Fig. 2(b), the CAM's read operation is divided into discrete precharge, sensing, and idle phases and synchronized by the CLK for reliable operation under stable conditions.

1) In the Precharge phase, PRE[i] is asserted to precharge the bitline BL[j] to a known reference voltage and the chosen CAM (i,j) cell is electrically isolated from BL[j] by keeping SA[i] deasserted.
2) To prevent any write disturbance, the control signal WH[i] is inactive. At this stage, the previously read value is stored in Data_Out, and BL[j] to a stable state.
3) In the Sensing phase, CLK transition causes WL[i] to be asserted in order to link CAM (i,j) to BL[j].
4) The precharged voltage on BL[j] is maintained if CAM (i,j) stores logic '1', producing a high level at Data_Out.
5) Finally, the selected data is latched and driven by the output buffer, producing a stable Data_out at the output.

During **Search Cycle**, the stored data and an input search data (SD[i]) are compared to provide a match address. The

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(a) Write cycle

(b) Read cycle

(c) Search cycle

(d) BIST cycle

Fig. 2. Timing diagrams for different memory operations: (a) Write cycle, (b) Read cycle, (c) Search cycle, and (d) BIST cycle.

chosen search lines (SLs) are precharged by PRE[i] before a search operation is started, and it is expected that the CAM array contains previously stored data (SD[i]). The timing diagram of a typical search operation is shown in Fig. 2(c).

1) SA_En is asserted to start the search process, and SA_pre is asserted to allow the application of the input search data, SD[i] to the CAM array.
2) SD [i] is driven high during a search for logic '1', and the stored word on the search line [SL] is compared with the search data at every bit position.
3) The global Match signal (MA[i]) is produced for a whole match, while the related SL stays at the precharged level. Only when Match = 1, which indicates that a matching word has been found and Data_out is vaild.
4) SD[i] is driven down during a search for logic '0', and any mismatch results in the relevant SL discharging.
5) An unsuccessful search is indicated if the SL is discharged, as MA[i] stays deasserted and Match stays low.
6) Data_out is invalid during the active search cycle if there isn't an asserted Match signal.

Consequently, the same structured control is leveraged during the **BIST cycle** as shown in Fig. 2(d) to systematically test the memory array as follows.

1) When BIST_En is asserted, the BIST controller takes over the CAM interface and provides the row decoder and column decoder with BIST_Data and BIST_Word[4:0].
2) There are two separate phases to every BIST operation:
   - Write phase: A predetermined test pattern (logic '1' or '0') is written into the chosen CAM word indicated by BIST_Word[4:0] once Wr_En is asserted.
   - Search phase: To find and verify the stored data against the anticipated BIST pattern, SA_En is declared to initiate read process.
3) After every read phase of the BIST verification process, the comparison findings are assessed internally. A failure indicated by BIST_Pass signal.
4) When every self-test procedure is successful, the BIST controller sets BIST_Pass to logic'1'; if not, BIST Pass is set to logic'0', indicating a fault condition.
5) In addition, internal observability is enhanced using observation bit address lines, which allow selective monitoring of internal bit nodes by limiting the external pin count.

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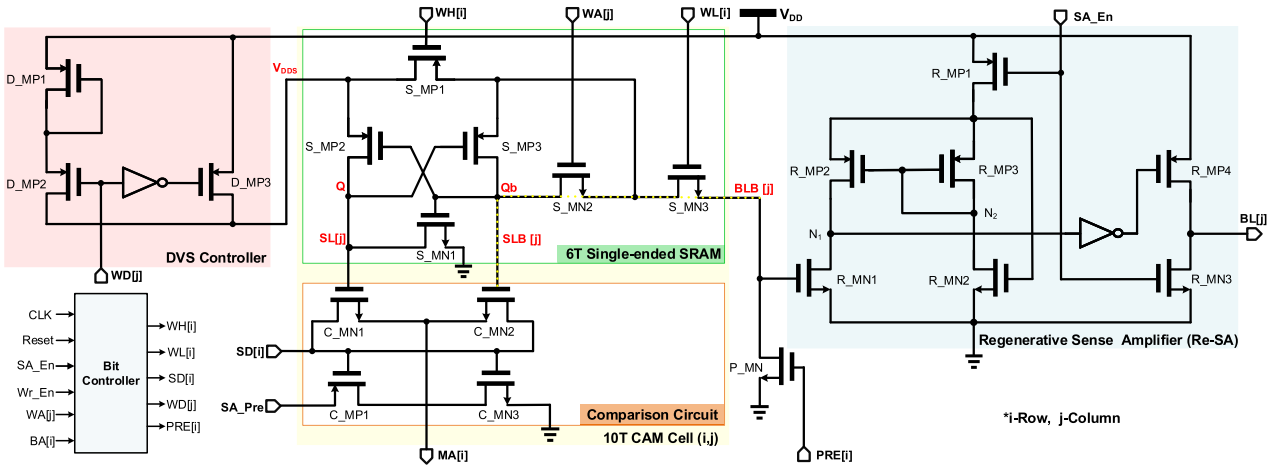


Fig. 3. Proposed DVS-assisted CAM cell with Regenerative Sense amplifier (Re-SA).

TABLE II

CONTROL SIGNALS AND MODES OF OPERATION FOR THE PROPOSED CAM CELL

Mode / Operation	WD[j]	WA[j]	WH[i]	WL[i]	PRE[i]	SD[i]	SA_En	SA_Pre	MA[i]	Operation Outcome
Standby Mode ($V_{DDS,Standby}$ = V_{DD} - 2$\|V_{DS}\|$)										
Standby	0	0	1	0	1	0	0	0	0	Low-power retention.
Active Mode ($V_{DDS,Active}$ = V_{DD} - $\|V_{DS}\|$): SRAM Write										
Write '1'	1	1	1	1	1	0	0	0	0	Stores logic '1' in Q, Re-SA off.
Write '0'	1	1	0	0	1	0	0	0	0	Stores logic '0' in Q, Re-SA off.
Active Mode: SRAM Read										
Read '1' (Q=1)	1	1	1	1	0	1	1	0	0	BL[j] remains near precharge.
Read '0' (Q=0)	1	1	0	1	0	1	1	0	0	BL[j] discharged.
Active Mode: CAM Search										
Search '1' (SL[j]=1)	1	1	0	1	0	1	1	1	1	Match detected.
Search '1' (SL[j]=0)	1	1	0	0	0	1	1	1	0	Mismatch detected.
Search '0' (SL[j]=0)	1	1	0	0	0	0	1	1	1	Match detected.
Search '0' (SL[j]=1)	1	1	0	1	0	0	1	1	0	Mismatch detected.

**Note:* i is the row index and j is the column index of CAM cell (i,j).

A. DVS-Assisted 10T CAM Cell With Regenerative Sense Amplifier (Re-SA)

The proposed 10T CAM cell with DVS support and column-level Regenerative Sense Amplifier is shown in Fig. 3. It incorporates a Dynamic Voltage Scaling (DVS) controller ((D_MP1–D_MP3), a 6T single-ended SRAM cell (S_MP1–S_MP3,S_MN1–S_MN3), a Comparison Circuit (C_MP1, C_MN1–C_MN3) and a Regenerative Sense Amplifier (Re-SA) (R_MP1–R_MP4,R_MN1–R_MN3). The design facilitates high-speed operation, enhanced energy efficiency, and a compact layout by integrating sensing, comparison, and storage components at the column level. Besides, bit controller, which will be described later in Section II-D1, all other circuit operations will be explained in this section.

The DVS controller dynamically adjusts the local supply voltage V_{DDS} according to the operational mode of the CAM cell, enabling energy-efficient operation while maintaining reliable functionality. Reliable SRAM and CAM operations are ensured while dynamic and leakage power reduced through adaptive voltage scaling. The proposed DVS controller uses a transistor-level local voltage scaling method, which eliminates the requirement for external regulation circuitry and minimizes implementation overhead in contrast to traditional architectures that require separate voltage regulators. The Re-SA amplifies tiny voltage differentials on the bit-lines/search lines to full-swing outputs with low static power consumption during SRAM cell read and CAM search operations. The control signals and associated operating modes of the CAM cell are compiled in the Table II, which also describes how each signal is set during standby, SRAM write/read, and CAM search operations and their functional results.

The following subsections describe the operational behavior in detail, highlighting the role of the DVS controller, bit-line management, and regenerative sensing.

1) Standby Mode: The CAM cell stays inactive in standby mode to preserve stored data and reduce dynamic and leakage power. The local supply voltage V_{DDS} is adaptively adjusted by the DVS controller (Fig. 3) in response to memory activity. The proposed DVS controller enables column-level supply modulation with minimal area overhead by a compact transistor network (D_MP1, D_MP2, D_MP3) and an inverter powered by the write data signal WDB[j]. While D_MP3 is off, the transistors D_MP1 and D_MP2 stack to introduce two drain-source drops, stabilizing internal transitions and lowering short-circuit currents. This results in $V_{DDS,Standby}$ = V_{DD} - 2 $|V_{DS}|$.

The SRAM storage nodes Q and Qb are electrically isolated from the bit lines BL during standby with WD[j] = 0 and

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WA[j] = 0. The stored data is maintained by the pull-up PMOS network (S_MP2-S_MP3) and the pull-down NMOS network (S_MN1-S_MN2), where S_MN1 acts as the primary pull-down path for node Q, while S_MN2 form the pull-down path for node Qb through S_MN3. Additionally, S_MP1 controls the power supply using WH [i], and S_MN3 functions as a wordline-controlled access switch providing the discharge path for Qb= 0 while isolating node Qb when Qb= 1. While, the Re-SA (SA_En = 0) is turned off to reduce leakage, the precharge transistor P_MN (PRE[i] = 1) precharges BLB[j] to a specified voltage level for subsequent operations.

To further evaluate the benefits of the proposed DVS controller, CAM columns' dynamic and leaky power performance is examined in both active and standby scenarios. The dynamic power consumption of a CAM column can be written as

$$P_{\text{dyn}} = \alpha \cdot C_{\text{eff}} \cdot {V_{\text{DDS}}}^2 \cdot f \tag{1}$$

where f is the working frequency, C_{eff} is the effective switching capacitance, and α is the activity factor. In contrast to a traditional fixed-V_{DD} design, the standby mode's normalized dynamic power becomes

$$\frac{P_{\text{dyn,Standby}}}{P_{\text{dyn,Conv}}} \approx \left(\frac{V_{\text{DD}} - 2 \cdot |V_{\text{DS}}|}{V_{\text{DD}}}\right)^2 \tag{2}$$

demonstrating a quadratic reduction enabled by local voltage scaling. While, Leakage power is given by

$$P_{\text{leak}} = I_{\text{leak}} \cdot V_{\text{DDS}} \tag{3}$$

For CAM arrays with a high number of inactive columns, the proposed strategy is quite effective since the stacked PMOS devices minimize both gate and drain biases, resulting in an exponential decrease in leakage current (I_{leak}).

2) Active Mode: As illustrated in Table II, When WD[j] = 1, the DVS controller activates DVS_MP3 in the linear region, setting the local supply voltage in active mode to $V_{\text{DDS,Active}} = V_{\text{DD}} - |V_{\text{DS}}|$. This lowers switching energy while providing enough voltage for dependable SRAM write, read and CAM search operations. The normalized dynamic power in Active mode can be written as

$$\frac{P_{\text{dyn,Active}}}{P_{\text{dyn,Conv}}} \approx \left(\frac{V_{\text{DD}} - |V_{\text{DS}}|}{V_{\text{DD}}}\right)^2 \tag{4}$$

exhibiting how local voltage scaling results in a quadratic reduction.

To illustrate the expected power savings, consider a nominal supply voltage of V_{DD} = 0.9 V and $|V_{\text{DS}}|$ = 0.1 V. In the proposed DVS controller, the local supply voltage becomes $V_{\text{DDS,Active}}$ = 0.8 V in active mode and is further reduced to $V_{\text{DDS,Standby}}$ = 0.7 V in standby mode. The dynamic power savings in standby mode is expressed as:

$$1 - \frac{P_{\text{dyn,Standby}}}{P_{\text{dyn,Conv}}} = 1 - \left(\frac{0.7}{0.9}\right)^2 \approx 0.395\ (\approx 40\%) \tag{5}$$

resulting in a 40% decrease in dynamic power compared to a traditional fixed-V_{DD} configuration. Even when operating actively, the dynamic power savings is estimated by:

$$1 - \frac{P_{\text{dyn,Active}}}{P_{\text{dyn,Conv}}} = 1 - \left(\frac{0.8}{0.9}\right)^2 \approx 0.210\ (21\%) \tag{6}$$

resulting in a power savings of about 21% without sacrificing functionality. These theoretical targets are closely validated by simulation results as discussed in Section III-B.

Furthermore, the V_{DDS} settles within less than the search cycle duration and has no effect on functional timing, according to post-layout transient simulations as discussed in section III. The area overhead is negligible because each column only requires the addition of three PMOS transistors, and the power overhead is still less than the leakage savings. Consequently, under both standby and active operation, the proposed DVS scheme offers a net energy benefit.

a) Sram write operation: The DVS controller supplies $V_{\text{DDS,Active}}$, during SRAM write operations to provide adequate voltage for reliable data storage while reducing switching energy. Depending on the input data, the internal storage node Qb driven through the respective access paths as illustrated in Fig. 4. Specifically, during a write '0' operation, S_MN3 is kept OFF (WL[i] = 0) to isolate the Qb from the complementary bit line BLB[j] as shown in Fig. 4(a). Conversely, during a write '1' operation, S_MN3 turns ON to establish a discharge path for Qb via S_MN2 as shown in Fig. 4(b).

- **Write '0' (WL[i] = '0'):** With WH[i] = '0' and WA[j] = '1', both access transistors S_MN2 and S_MN3 are OFF. Transistors S_MP1 and S_MP3 turn ON to drive Qb = '1', which activates S_MN1 and pulls Q = '0' while S_MP2 stays OFF.
- **Write '1' (WL[i] = '1'):** With WH[i] = WA[j] = '1', S_MN2–S_MN3 are activated, and PRE[i] = '1' turns ON P_MN to ground BLB[j]. Node Qb discharges to '0', turning ON S_MP2 to pull Q = V_{DDS}(Q = '1'), while S_MP1, S_MP3, and S_MN1 remain OFF.

Before writing, the precharge transistor P_MN (PRE[i] = 1) stabilizes the bit lines BLB[j], guaranteeing a reliable and regulated data injection. During this stage, Re-SA (SA_En = 0) is kept inactive to avoid spurious amplification.

b) Sram read operation: During the read operation, WL[i] and WA[j] are asserted, while PRE[i] = '0' and SA_En = '1', as summarized in Table II. First, the read path is established via access transistors, S_MN2 and S_MN3, which connect the SRAM cell to the Re-SA. The cross-coupled transistors S_MP2 and S_MP3 retain the stored state and determine which branch of the read path is activated. The resulting transistor operation is illustrated in Fig. 5.

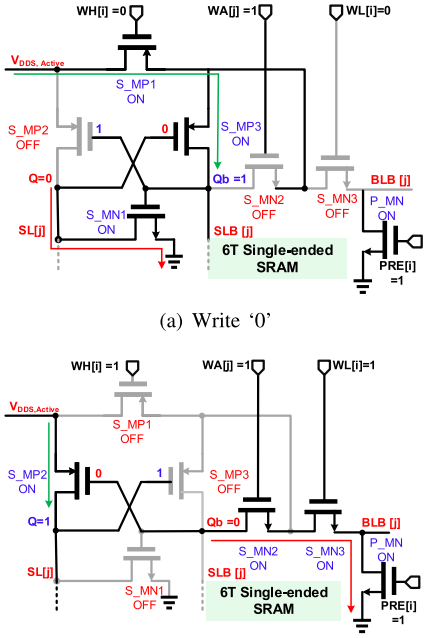
- **Read '0' (Q = '0', Qb = '1'):** As shown in Fig. 5(a), S_MP1 and S_MP3 turn ON to hold node Qb high while S_MN1 grounds node Q, keeping BLB[j] charged high so the sense amplifier detects a logic '0'.
- **Read '1' (Q = '1', Qb = '0'):** As shown in Fig. 5(b), the stored state keeps S_MP2 ON; when the read path is enabled via access transistors, this discharges BLB[j] to '0', enabling the Re-SA to sense the signal and resolve a full-swing logic 1 output.

When activated by SA_En, the Re-SA uses regenerative feedback to amplify the small bitline signal BLB[j], resolve its polarity, and restore it into a full-swing logic output BL[j].

c) Cam search operation: The CAM comparison circuit, consisting of C_MP1 and C_MN1–C_MN3, evaluates the match condition between the stored data SD[i] and the search line SL[j] as illustrated in Fig. 6.

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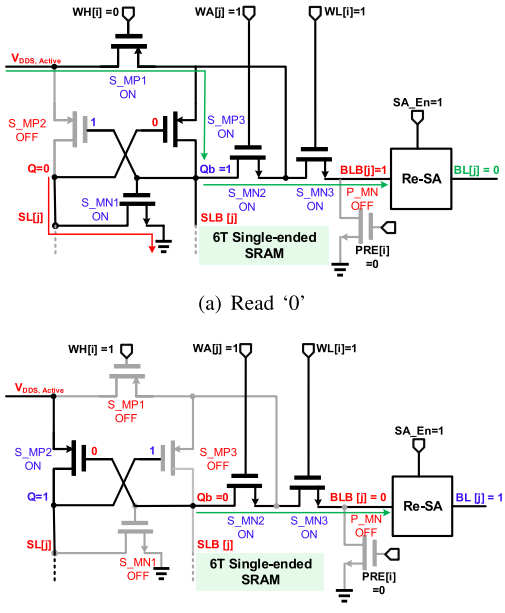
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(a) Write '0'

(b) Write '1'

Fig. 4. 6T single-ended SRAM write operations.



(a) Read '0'

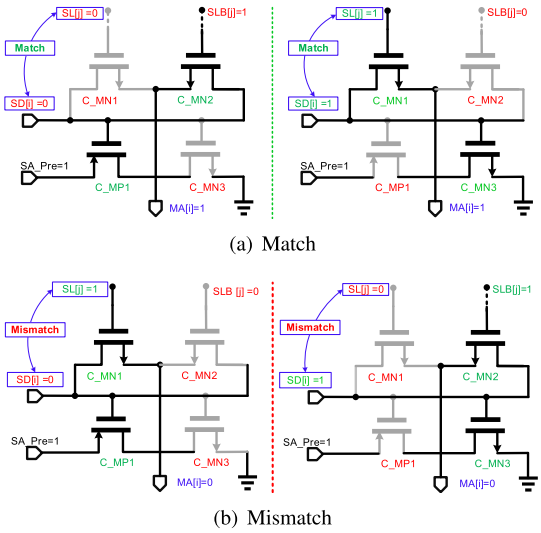
(b) Read '1'

Fig. 5. 6T single-ended SRAM read operations.

- **Match (SL[j] = SD[i]):** In the match condition shown in Fig. 6(a), the discharge path remains OFF, maintaining MA[i] at logic '1'.
- **Mismatch (SL[j] ≠ SD[i]):** In the mismatch condition shown in Fig. 6(b), the mismatched search input activates the pull-down path, discharging MA[i] to logic '0'.

This results in MA remains high for a match and is discharged low whenever the stored data and search data are no match.

3) Robust CAM Search and SRAM Read via Re-SA: The Regenerative Sense Amplifier (Re-SA) amplifies minor differentials in BLB[j] using positive feedback and precharges internal nodes to ensure strong BL[j] signaling with low static current under V_{DDS}-scaled conditions.



(a) Match

(b) Mismatch

Fig. 6. CAM operations.

As shown in Fig. 3, the Re-SA is made up of an output discharge transistor (R_MN3), a cross-coupled latch (R_MP3/R_MP4/R_MN1/R_MN2), and precharge devices (R_MP1/R_MP2) and its operation summarized as follows:

- **Precharge (SA_En = 0):** Internal nodes are charged to V_{DD}, eliminating residual voltages from previous cycles.
- **Evaluation (SA_En = 1):** Positive feedback through the cross-coupled latch amplifies the small SLB[j]/BLB[j] differential, producing a full-swing BL[j] output.

The sensing behavior of the Re-SA, as shown in Fig. 7, is analytically described in the following aspects.

1) **Regenerative Behavior:** The exponential amplification during evaluation is modeled as:

$$\Delta V_{out}(t) = \Delta V_0 e^{t/\tau} \tag{7}$$

where ΔV_0 is the initial differential voltage at the bit line BLB[j], and τ is the regeneration time constant. The corresponding regeneration delay is:

$$t_{reg} = \tau \ln\left(\frac{V_{DD}}{\Delta V_{BLB}}\right) \tag{8}$$

2) **Noise and Offset Considerations:** The signal differential must continue to be larger than the comparable noise and offset components for reliable operation:

$$\Delta V_{BLB} > V_{OS} + V_{noise} \tag{9}$$

where V_{OS} is the input-referred offset and V_{noise} represents thermal and coupling noise at nodes N_1 and N_2.

3) **Metastability Condition:** The regenerative latch enters a metastable state when the internal nodes satisfy $N_1 \approx N_2$, which causes a considerable slowdown in the output. This state can be roughly represented by:

$$t_{meta} \propto \tau \ln\left(\frac{1}{\Delta V_{BLB}}\right) \tag{10}$$

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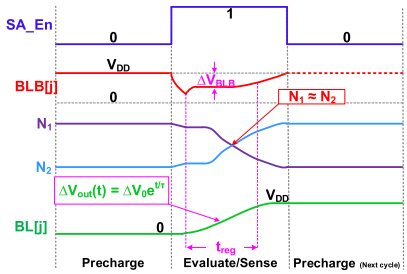


Fig. 7. Illustrative waveforms of the Regenerative Sense Amplifier (Re-SA).

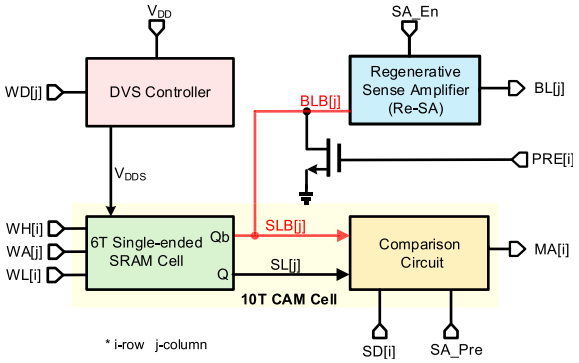


Fig. 8. Simplified view point of the proposed CAM with BL/SL Sharing.

The regenerative feedback mechanism enables rapid recovery from metastability by reducing the effective regeneration time.

Overall, the proposed Re-SA converts a small voltage perturbation (ΔV_{BLB}) on BLB[j] into a full-swing output voltage ($\Delta V_{\mathrm{out}}(t)$) at BL[j] as shown in Fig. 7 through regenerative amplification, enabling fast, low-power, and robust sensing.

B. Unified Bit-Line/Search-Line (BL/SL) Sharing Strategy

To improve array density and maximize routing resources, the proposed CAM uses an effective bit-line/search-line (BL/SL) sharing design as highlighted in Fig. 3 and Fig. 8. The main difference between the proposed CAM and previous single-ended or precharge-reduced CAM designs is that the shared BL/SL is a unified physical access-search path that simultaneously supports write, read, and search operations under DVS controller, rather than merely a reused interconnect. The 10T CAM cell's single-ended bit-line BLB[j]/SLB[j] is made to effectively manage SRAM read,write operations and CAM search operations. The concept greatly reduces column pitch and metal routing complexity by avoiding the need for dedicated search lines by leveraging the existing SRAM bit-line for search evaluation. With the comparison path separated by SA_Pre, BL[j] functions as a traditional read/write node during SRAM operations, guaranteeing complete compatibility with normal memory capabilities. While SLB [j] carries the search input in CAM mode, the word-line [WL[i]] stays inactive, allowing for effective match assessment without interfering with the stored data.

With little additional hardware, CAM functionality can be seamlessly integrated into an SRAM array thanks to this unified BL/SL sharing technique. The method preserves strong functionality while lowering dynamic power consumption, connection capacitance, and area efficiency. Reliable functioning in both SRAM and CAM operations is ensured by careful phase control and the addition of an isolation device between BLB[j] and the comparison circuit. Consequently, the architecture produces a high-performance, small, and power-efficient embedded CAM solution that is ideal for designs with limited space and scalability.

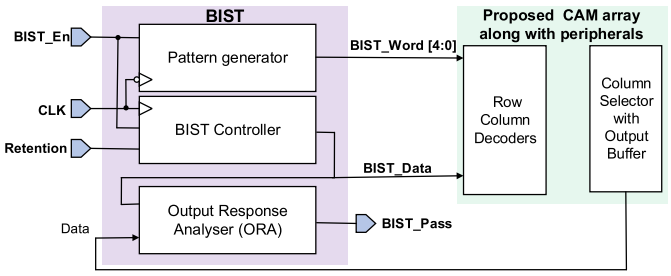


Fig. 9. On-Chip BIST for CAM Verification.

C. Built-In Self-Test (BIST)

In contemporary CAM designs, on-chip BIST is crucial for precise and economical memory array testing. It's become more difficult to find time, search, and retention issues with outside testers, and costly post-package testing drives up production prices even more. On-chip BIST minimizes dependency on expensive automatic test equipment (ATE), enhances fault coverage, and permits at-speed testing.

The on-chip BIST for the CAM as shown in Fig. 9 is intended to enable efficient functional, search, and retention testing with minimal external support. The BIST_En signal runs synchronously with the system CLK. The Pattern Generator responsible for predefined test data (BIST_Data) and corresponding word addresses (BIST_Word[4:0]), applied to the CAM during self-test operations. The BIST controller responds to the Retention signal for aid data-retention, and controls the timing and sequencing of test phases.

The generated BIST_Data and BIST_Word [4:0] are forwarded to the CAM Access and Control Interface, comprising the row decoder and controller and the column selector with output buffer. The row decoder initiates the selected word lines and related control signals, while the column selector with output buffer routes the equivalent data from the CAM array to the output path. The observed read data fed back to the Output Response Analyzer (ORA), where it is compared against the expected response generated internally by the BIST logic. Based on this comparison, the ORA governs the correctness of the CAM operation and declares the BIST_Pass signal upon successful completion of all test sequences. The proposed on-chip BIST significantly improves the testability, observability, and reliability of the CAM while lowering pin overhead and external testing complexity.

D. Peripheral Circuits

The peripheral circuits of the proposed 32 × 32 CAM architecture, namely the row decoder, column decoder, bit

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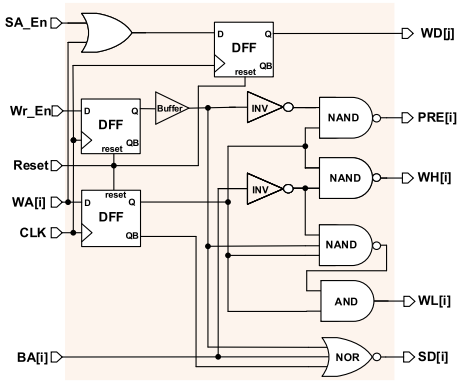


Fig. 10. Circuit diagram of bit controller.

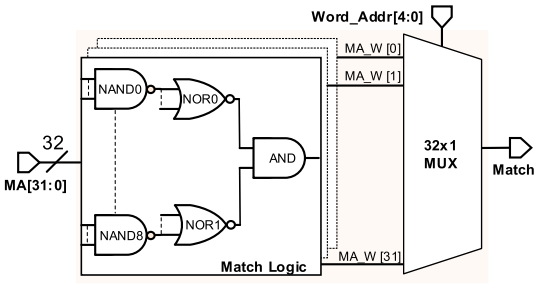


Fig. 11. Schematic of Match Arbitration Encoder (MAE).

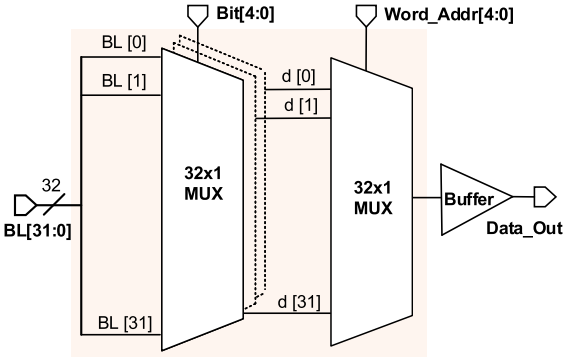


Fig. 12. Schematic of column selector with output buffer.

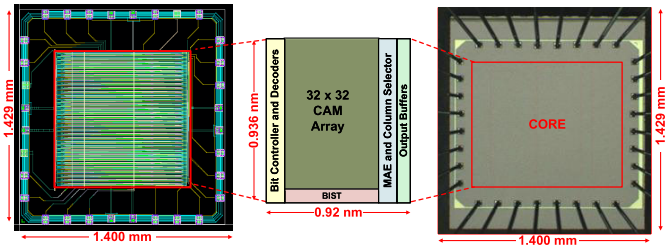


Fig. 13. Layout, floorplan and chip photograph of the proposed CAM Design.

controller, column selector with output buffer, and MAE as shown in Fig. 1.

The precise selection of a column and row in a CAM cell made possible by the column decoder and the row decoder, which maps the 5-bit Word_Addr to 32 column selection signals (WA[31:0]) and 5-bit Bit_Addr to 32 word-line signals (BA[31:0]). The decoded row and column signals are crucial inputs to the bit controller, which uses them in conjunction with control signals to precisely time and coordinate internal operations of the CAM.

1) Bit Controller: As shown in Fig. 10, the bit controller uses the subsequent inputs to provide synchronized control signals for CAM operation: Write Enable (Wr_En), Sense Amplifier Enable (SA_En), Column Select (WA[j]), Row Select (BA[i]), Reset, and Clock (CLK). It generates precharge (PRE[i]), writing header (WH[i]), word line (WL[i]) and Search data (SD[i]) signals with exact timing to coordinate write, search, and standby modes using D flip-flops and combinational logic. This ensures controlled sensing and selective activation of rows. To set up the match lines and allow for safe writing, the precharge and write header signals are precisely synchronized. In the meantime, to reduce power consumption and increase sensing accuracy, the sense amplifier enable signal only activates for the chosen row during evaluation.

2) Match Arbitration Encoder (MAE): The 32-bit match-line outputs, MA[31:0], produced by the CAM array are resolved by the Match Arbitration Encoder (MAE). Instead of using a single high fan-in gate, a hierarchical reduction design is used to lower capacitive loading and propagation latency. NOR aggregation is used to create intermediate indications after the match signals have been gathered and processed through cascaded NAND stages. While high fan-in/out CMOS circuits have poor noise margins and are more sensitive to PVT fluctuations, robustness in low-voltage and subthreshold operation is improved by reducing effective fan-in through hierarchical design.

Only the match result of the chosen row is propagated to the global Match output when the conditioned outputs (MA_W[31:0]) are applied to a 32 × 1 multiplexer under the control of Word_Addr[4:0] as shown in Fig. 11. This address-aware arbitration achieves low-latency and energy-efficient operation appropriate for high-density CAM systems by enabling deterministic resolution under multiple-match scenarios without the need for additional priority encoding.

3) Column Selector With Output Buffer: During read or search operations, the column selector chooses the necessary bit-line that corresponds to the requested word. The 32 column bit-lines, BL[31:0], are firstly applied to a 32 × 1 multiplexer that is managed by the bit-select signals Bit[4:0], producing intermediate data signals d[31:0], as seen in Fig. 12. The final data linked to the addressed word is chosen by a second 32 × 1 multiplexer that is powered by the decoded word-address signals Word_Addr[4:0]. The global data path's parasitic loading and routing complexity are decreased by this two-stage multiplexing configuration. Furthermore, this block drastically lowers dynamic power usage by limiting switching activity to just the chosen columns.

III. Experimental Validation and Performance Evaluation

Fig. 13 illustrates the complete view of the proposed CAM design and implementation using TSMC 40-nm CMOS process. The die area of the manufactured chip, including the

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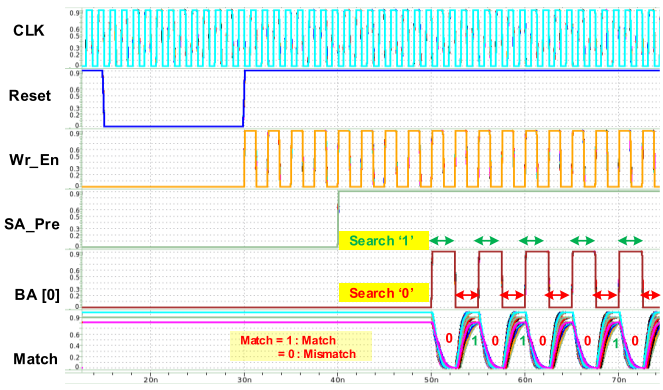


Fig. 14. Post-simulation waveforms of Write '0, Search '1 and Search '0.

pad ring and peripheral circuitry, is 1.400 mm ×1.429 mm (2.0006 mm^2;). The 32×32 CAM array, bit controller, row and column decoders, MAE, output buffers, and built-in self-test (BIST) module are all integrated into the active core, which is 0.92 mm ×0.936 mm (0.8611 mm^2;).

A. Functional Verification

Both write and search patterns were assessed in order to confirm the fundamental functionality of the proposed CAM. The CAM cell's internal storage nodes Q and Qb were specifically examined during simulations to see how the memory behaved. The following is a summary of the assessed search patterns:

- **Testing Pattern (Write 1'):** Search '0' produces a mismatch (Match = 0), while Search '1' produces a match (Match = 1) when SA_Pre is asserted.
- **Testing Pattern (Write 0'):** Search '1' produces a mismatch (Match = 0), while Search'0' produces a match (Match = 1) when SA Pre is asserted as shown in Fig. 14.

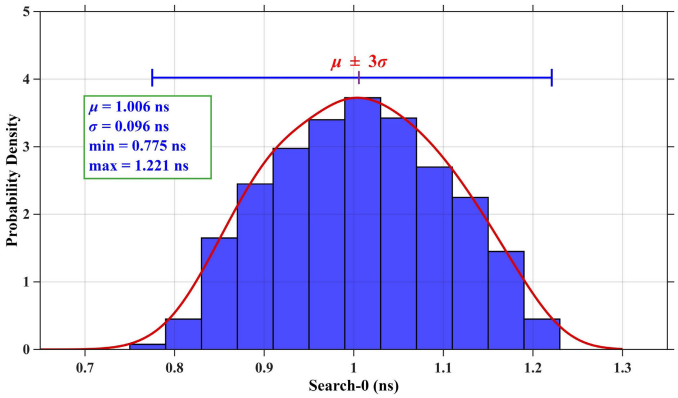
The robustness of the search time under process and circuit variations was assessed using 1000-run Monte Carlo simulations. Search-0 displays a normalized offset with μ = 1.006, σ = 0.096, and a range of 0.775–1.221, as illustrated in Fig. 15(a). The normalized offset with μ = 1.004, σ = 0.065, and a range of 0.825–1.190 for Search-1 as shown in Fig. 15(b).

B. Power Savings by the DVS Controller

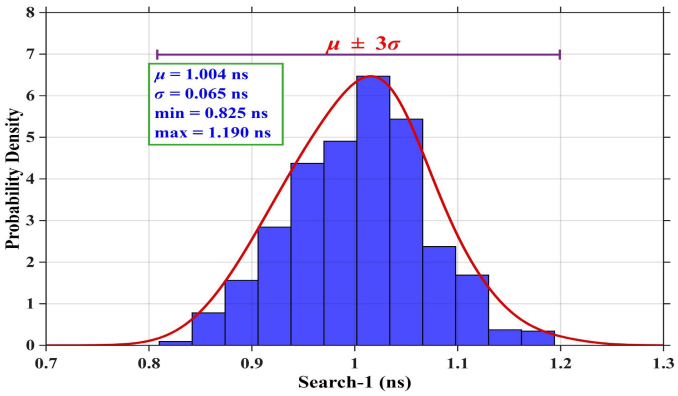
The power consumption of the proposed 10T CAM cell with and without the proposed DVS controller is presented in Fig. 16. The CAM cell without a DVS controller consumes 0.9006 μW. With the integration of the proposed DVS controller, the power consumption of the 10T CAM cell drops to 0.7605 μW in active mode and further decreases to 0.5303 μW in standby mode. Compared to the design without a DVS controller, the proposed design achieves a net power savings of 15.6% and 41.1% in active and standby modes, respectively, validating the effectiveness of the DVS controller.

C. Search Time Analysis Under Various PVT Corners

As shown in Fig. 17, the search-time robustness of the proposed 32×32 CAM was evaluated under different process-voltage-temperature (PVT) corner variations at V_{DD} = 0.9 V.



(a) Search '0'



(b) Search '1'

Fig. 15. Monte Carlo distribution of search time offset (1000 runs).

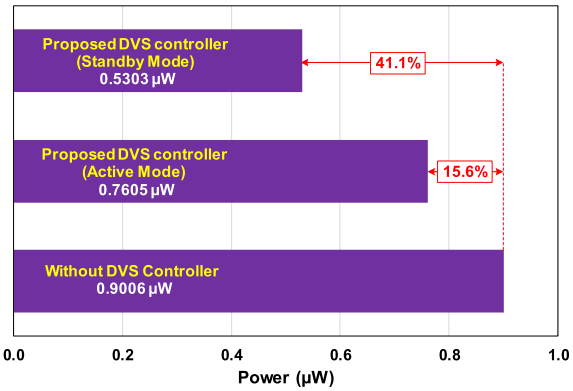


Fig. 16. Power savings by DVS controller.

The analysis considers three PVT corners: FF (0.9 V, 100°C), TT (0.9 V, 25°C), and SS (0.9 V, 0°C), to evaluate the impact of process and temperature variations on search latency.The key observations are summarized as follows:

- Under the FF corner, the proposed CAM achieves the fastest search operation, with search delays of 0.511 ns for searching '0' and 0.488 ns for searching '1'.
- At the TT corner, the search delays slightly increase to 0.592 ns and 0.585 ns for search '0' and search '1', respectively, representing the nominal operating condition.

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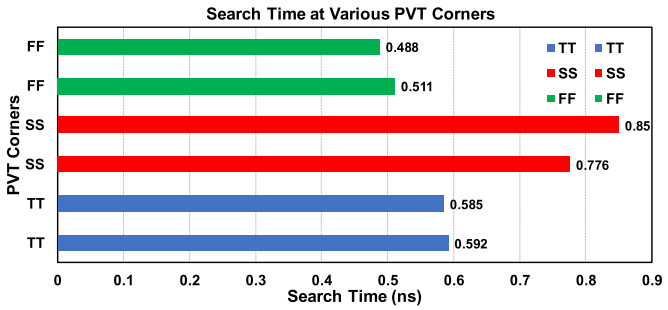


Fig. 17. Search Time analysis at various PVT Corners.

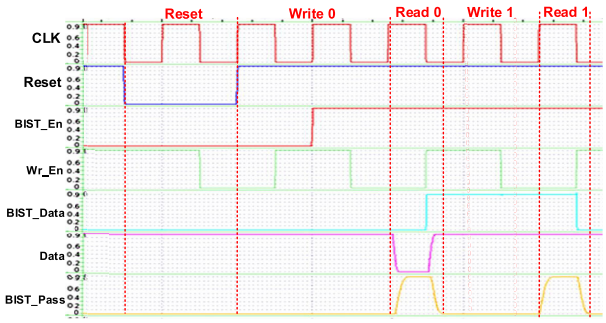


Fig. 18. BIST operation with corresponding BIST_Pass assertions.

- The SS corner exhibits the worst-case performance with search delays increase to 0.776 ns for search '0' and 0.850 ns for search '1'.

Despite PVT-induced variations, the maximum search latency remains below 1 ns under all evaluated conditions, demonstrating the robustness, reliability, and stable search operation of the proposed CAM architecture.

D. Sensing Margin and PVT Robustness Analysis

To evaluate the reliability of the proposed Regenerative Sense Amplifier (Re-SA), over supply-voltage, temperature, and process variations. A ±10% nominal supply voltage variation of 0.90 V is considered, corresponding to V_{DD} = 0.81 V, 0.90 V, and 0.99 V, the temperatures -25^{0}C, 25^{0}C and 125^{0}C, and five process corners (TT, FF, SS, FS and SF), resulting in a total of 45 PVT combinations.

Across these PVT corners, the sensing margin ranges from 0.032 to 0.590 V, with an average value of 0.432 V. The nominal sensing margin is 0.5 V at TT, 0.90 V, and 25^{0}C. The worst-case sensing margin of 0.032 V occurs at SF, 0.99 V, and 125^{0}C, whereas the maximum value of 0.59 V is obtained at SS, 0.99 V, and -25^{0}C. The positive sensing margin across all evaluated PVT combinations confirms the robust sensing operation of the proposed Re-SA.

E. Built-in Self-Test (BIST) Verification

Through supervised write and search operations, the Built-In Self-Test (BIST) on the chip ensures that the CAM is functionally valid. The BIST_En signal is asserted to start the test mode once all registers have been reset; deterministic logic patterns are written into the CAM (Write'0' and Write '1' phases). To verify comparison functionality, subsequent content-based search operations (Read '0' and Read '1') employ the same patterns as search keys. The BIST_Pass indicates that the storage elements and the matching circuitry are working without any issues. The waveforms corresponding to the BIST operation are shown in Fig. 18, indicating that the memory cells and associated control circuits function correctly and can detect operational flaws on their own.

F. Measurement Setup and Search Time Validation

The PCB-mounted 32 × 32 CAM prototype and associated measurement setup are shown in Fig. 19. The chip, which comes in a 32-pin DIP packaging, has distinct V_{DD} and V_{SS} rails for reliable low-voltage operation. V_{DD} and V_{SS} are produced by a controlled supply from an Agilent E3631A, whereas CLK, Reset, Wr_En, SA_En, BIST_En, retention, Bit_Addr(4:0), Word_Addr(4:0)and Bit(4:0) are provided by an Agilent 81250 pattern generator. A Keysight DSAV134A oscilloscope is used to record the output signals Data_out, Match, and BIST_Pass in order to verify functionality and compare simulation results with silicon results.

The measurement result validates the CAM functionality during successive search operations at clock frequency of 20 MHz as shown in Fig. 20. By means of the clock (CLK) running, SA_Pre signal describes the active search window, in which the match output responds to the applied search data (SD [0]). When the SD [0] matches to the stored data, the match signal is high, indicative of a successful match, although a mismatch condition keeps the match output low. The search time reach their least values at a operating frequency of 20 MHz around 2.16 ns as shown in Fig. 20.

G. Performance Comparison and Discussion

Table III provides a thorough performance comparison between the proposed 32 × 32 CAM and existing state-of-the-art designs, with special attention to the silicon-validated works in [19] and [23]. In contrast to a number of other studies [15], [16], [24], [26] that solely present simulation results.

The proposed CAM achieves a simulated search time of 0.47 ns at a 100 MHz clock frequency, while the fabricated chip exhibits a measured search time of 2.16 ns at 20 MHz, corresponding to a 4.60× increase over the simulated value. The lower operating frequency was selected during experimental characterization to ensure clear waveform transitions and minimize signal degradation through the test-board interfaces. The measured search time additionally effected by propagation and settling delays associated with parasitic resistance and capacitance [27], supply variations, package and PCB parasitics, oscilloscope probe loading (≈ 20 pF), and output settling during measurement. These nonideal effects reduce the effective sensing margin of the CAM cell and increase the search time relative to the simulated result.

Despite these effects, the measured search time of 2.16 ns is slightly higher than that reported in [19] (1.16 ns) and substantially lower than that in [23] (8.00 ns). The lower latency in [19] is due to capacitor-divider sensing and RRAM's dual function as a store and switching element. In terms of energy efficiency, the proposed design consumes

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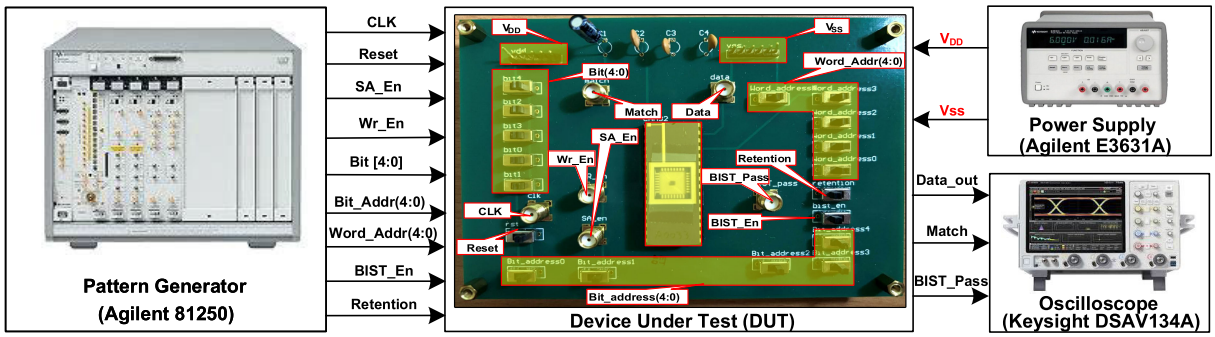


Fig. 19. Measurement Setup.

TABLE III
PERFORMANCE COMPARISON WITH PRIOR CAM DESIGNS

Parameter	TCAS II [16]	TVLSI [26]	TVLSI [15]	TCAS I [19]	JSSC [23]	TETC [24]	Ours
Year	2022	2023	2024	2024	2025	2025	2026
Prototype	No	No	No	Yes	Yes	No	Yes
On-chip BIST	No	No	No	No	No	No	Yes
Technology (nm)	28	28	45	180	65	65	40
Supply Voltage (V)	1.0	1.0	1.0	1.80	1.2	1.2	0.9
CAM Size	128 × 128	64 × 64	256 × 128	64 × 64	64 × 512	NA	32 × 32
Total Bits (N_{bits})	16384	4096	32768	4096	32768	NA	1024
Verification	Sim.	Sim.	Sim.	Meas.	Meas.	Sim.	Sim./Meas.
F_{max} (GHz)	NA	1.18	NA	0.875	0.13	1.00	0.1/0.02
Search Time (ns)	1.5	0.44	0.59	1.16	8.00	1.00	**0.47/2.16**
Energy/Search/Bit (fJ)	0.33	1.28	1.44	4.15	0.19	2.14	**0.94/1.22**
EFS_N (fJ/bit/Search)	0.21	0.80	1.44	5.12	0.19	2.15	**1.30/1.34**
$Delay_N$ (ns)	0.93	0.27	0.59	8.35	13.87	1.73	**0.38/1.73**
EDP_N (fJ·ns)	0.19	0.21	0.84	42.75	2.63	3.71	**0.49/2.32**
FOM	NA	65.30	NA	29.58	66.52	NA	**11.15/4.16**

*Note: EFS_N, $Delay_N$, and EDP_N denotes normalized energy efficiency, delay, and energy-delay product respectively.

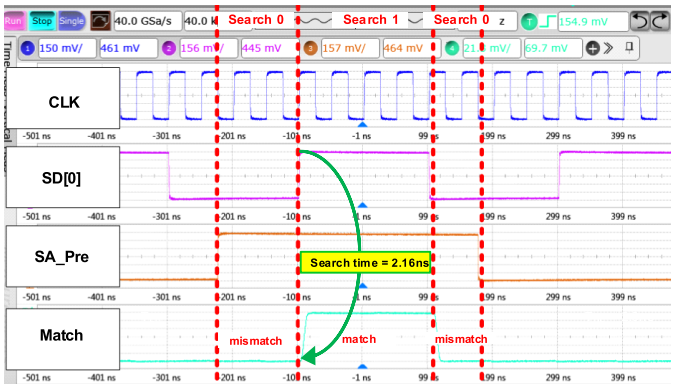


Fig. 20. Measured results at clock frequency of 20 MHz.

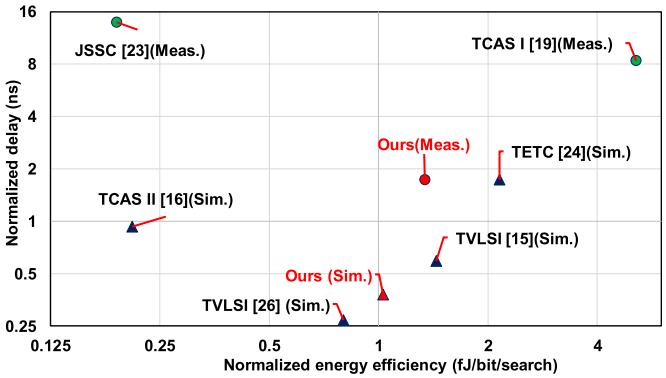


Fig. 21. Normalized energy–delay trade-off of recent CAM Designs.

1.22 fJ/bit/search, corresponding to a normalized energy of 1.34 fJ/bit/search, which represents a significant improvement over [19] (5.12 fJ/bit/search) but it still falls short of [23], which gains from effective approximation matching.

Nevertheless, since exact matching with a deterministic evaluation requires more energy each search, the proposed CAM ensures higher accuracy and dependability.

The normalization methodology in [20] is used to provide a fair comparison as follows

$$\text{Delay}_N = \text{Search Time} \cdot \frac{\text{Technology}}{45\ \text{nm}} \cdot \frac{V_{DD}}{1V} \tag{11}$$

$$\text{Efs}_N = \text{Efs} \cdot \frac{\text{Technology}}{45\ \text{nm}} \cdot \left(\frac{1V}{V_{DD}}\right)^2 \tag{12}$$

The proposed CAM achieves a normalized delay of 1.73 ns by using the normalization approach in Eqn. (11), makes 4.8× faster than [19] and 8× faster than [23]. With a normalized energy efficiency (EFS_N) of 1.34 fJ/bit/search, the design outperforms [19] (5.12 fJ/bit/search) and remains competitive with [23], according to Eqn. (12).

The proposed CAM offers a significantly improved normalized energy-delay tradeoff as illustrated in Fig. 21, especially

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in terms of reduced search time while guaranteeing comparable energy efficiency in contrast to the most recent simulated CAM designs [15], [16], and [24]. Furthermore, the measurement results show a better overall trade-off between normalized energy and delay than the previous measurement reports in [19] and [23], confirming the viability and efficacy of the proposed design. To further quantify this tradeoff, the normalized energy-delay product (EDP_N) is defined as the product of EFS_N and $Delay_N$, as given in Eqn. (13).

$$EDP_N = Efs_N \cdot Delay_N \tag{13}$$

A lower EDP_N indicates a more favorable combined energy-delay characteristic and provides a unified basis for comparison across different technology nodes, supply voltages, and array sizes. The proposed CAM achieves EDP_N values of 0.49 fJ.ns in simulation and 2.32 fJ.ns in measurement. The measured value is lower than those reported for the silicon-validated designs in [19] and [23], which exhibit EDP_N values of 42.75 and 2.64 fJ.ns, respectively. In contrast to the silicon-validated designs in [19] and [23], the proposed design incorporates an on-chip BIST feature in a unique way to enable effective silicon characterization and testing.

A unified figure-of-merit is defined as:

$$FOM = \frac{E_{search/bit} \times \left(\frac{F_{max}}{1\ GHz}\right) \times N_{bits} \times \left(\frac{Search\ time}{1\ ns}\right)}{\left(\frac{V_{DD}}{1\ V}\right)^2 \times \left(\frac{Tech}{1\ nm}\right)} \tag{14}$$

Relying solely on single parameter measures, such as energy per bit or search time, can obscure critical performance trade-offs, such as the notable frequency drop in low power sub threshold circuits, or result in biased comparisons. A comprehensive 6-variable Figure of Merit (FOM) is used to address this problem. It normalizes supply voltage (V_{DD}), process technology node (Tech), Maximum operating frequency (F_{max}), memory capacity (N_{bits}), and search time T_{search}. When compared to previous designs, our prototype achieves an FOM of 4.16 using this evaluation framework, demonstrating improved overall optimization. This finding demonstrates how the proposed design balances optimization in terms of speed, energy efficiency, scalability, technology node, and operating voltage.

IV. Conclusion

A fully integrated 32 × 32 CAM based on single-ended memory cells with a shared BL/SL architecture is presented in this study. The concept overcomes the drawbacks of traditional differential CAM systems by integrating read/write and search functions on a single physical line, greatly lowering routing capacitance, redundant switching, and total power consumption. Measurement results confirm the effectiveness of the proposed single-ended technique. The fabricated 40-nm CMOS CAM prototype operates at a 0.9-V supply voltage and achieves a search time of 2.16 ns with a measured energy efficiency of 1.22 fJ/bit/search, demonstrating its suitability for high-speed and energy-efficient search applications.

Normalized performance analysis highlights both quick search capabilities and energy efficiency, demonstrating significant gains in the energy–delay trade-off. The proposed CAM reduces search latency, achieves the required search throughput at a lower operating frequency, and lowers dynamic power consumption, making it an efficient solution for modern lookup-intensive and energy-constrained applications.

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