

## 7.2-3

# A Transceiver Design for Electronic Control Unit (ECU) Nodes in FlexRay-based Automotive Communication Systems

Chua-Chin Wang, *Senior Member, IEEE*, Gang-Neng Sung, *Student Member, IEEE*,  
and Po-Cheng Chen

**Abstract** – This paper presents a transceiver design compliant with FlexRay standards. An LVDS-like transmitter is proposed to drive the twisted pair of the bus. By contrast, a 3-comparator scheme is used to carry out the required bit-slicing and state recognition at the receiver of the bus.

**Key word:** FlexRay, transceiver, automobile electronics, in-car networking, low power

### I. INTRODUCTION

Car electronic has been deemed as the 4<sup>th</sup> “C” right after Computer, Communication and Consumer electronics. Many novel electronic devices have been introduced and installed in recently publicized cars. Therefore, an in-car network has been proposed to control and supervise all of the automobile electronics. Thanks to the fast evolution of semiconductor technology, devices with an electronic control unit (ECU) have been installed in automobiles. In 1990, the average quantity of ECUs in an automobile was fourteen. By 2000, the number of ECUs reaches forty. Notably, certain luxury automobiles can even have over one hundred ECUs.

The FlexRay standard is designed for an in-car network. It will not replace the existing network, but it can combine and integrate with existing systems, including CAN (Controller Area Network), LIN (Local Interconnection Network), MOST (Media Oriented System Transport) [1] and J1850 protocol etc. FlexRay requires 10 Mbps data rate in either one of the two channel of an ECU. If a single channel is used alone, the speed of the total data rate will reach 20 Mbps. Therefore, even the video signals, multimedia and control signals can communicate via the FlexRay system with a high bandwidth. The ultimate goal is that the automobile is X-by-wire (X = steer, break, accelerate, A/V, safety, etc.). Fig. 1 shows the feature of FlexRay is used (X-by-wire).

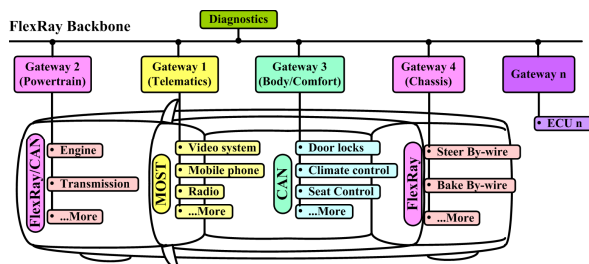


Fig. 1. The feature of FlexRay is used (X-by-wire).

### II. TRANSCIEVER DESIGN FOR FLEXRAY SYSTEM

Fig. 2 shows the block diagram of ECU nodes in a FlexRay system. The component of each node contains a host microcontroller ( $\mu\text{C}$ ), a communication controller (CC), a bus guardian (BG) and two bus drivers (BD). Traditionally, the transceiver in the bus driver should be implemented by a high-voltage silicon process [2]. However, we propose an LVDS-like Tx/Rx design which can be implemented by a typical 0.18  $\mu\text{m}$  mixed-signal CMOS process. Hence, the proposed design can be integrated with other digital blocks easily besides cost down.

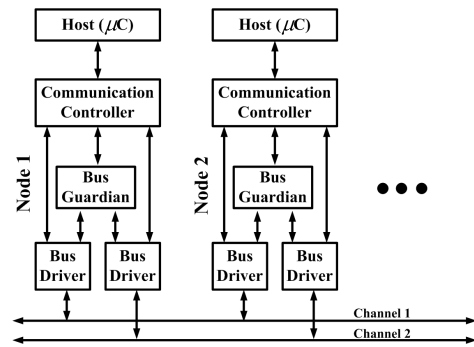


Fig. 2. Block diagram of ECU nodes in a FlexRay system.

According to the FlexRay standards [3], two signals of the bus driver, denoted as BP (Bus Plus) and BM (Bus Minus), are used to convey bit information over a pair of twisted lines. BP and BM in fact are a pair of differential signals. The timing and amplitude characteristics of BP and BM required by the FlexRay standards are shown in Fig. 3.

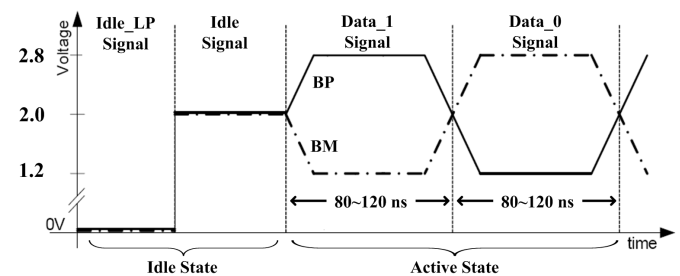


Fig. 3. The characteristics of BP and BM.

#### A. Design of the Transmitter

There are a total of four types of “Signals” in FlexRay systems, which are Data\_1 Signal and Data\_0 Signal in the Active State, and Idle\_LP Signal, Idle Signal in the Idle State. We propose an LVDS-like transmitter design as show on Fig. 4. Data0\_C, Data1\_C, Idle\_C and Idle\_LP\_C are control signals fed into the bus driver. Data0\_C and Data1\_C are a pair of digital differential signals which are generated by Communication Controller (CC) to notify the bit to be

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<sup>1</sup> C.-C. Wang, G.-N. Sung, and P.-C. Chen are with Department of Electrical Engineering, National Sun Yat-Sen University, 80424, Taiwan. (email: ccwang@ee.nsysu.edu.tw)

transmitted over the bus. Idle\_C and Idle\_LP\_C are a pair of idle signals. When the Idle\_C is asserted, BP and BM must be locked on the same Vref, which is 2 V in this work. By contrast, as soon as the Idle\_LP\_C is asserted, indicating that the low power mode is chosen, Both BP and BM are pulled down to GND. Notably, Vdd33V denotes that the supply voltage is 3.3 V. EN and EnB are an enable and a disable signals, respectively, generated by Idle\_C and Idle\_LP\_C to select the gate drives of M101, M102, M103, and M104. For instance, if Data1\_C = 1, Data0\_C = 0, Idle\_C = Idle\_LP\_C = 0, then En = 0 and EnB = 1, such that M103 and M102 are both on, which in turn pull down BM and pull up BP to generate Data\_1 signal. That is, a "1" is transmitted.

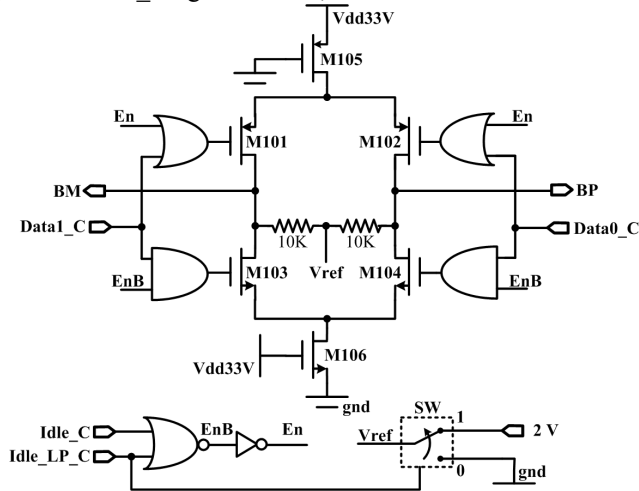


Fig. 4. The schematic of the transmitter.

### B. Design of the Receiver

Different from receivers circuit of traditional buses, the receiver for FlexRay systems must recognize the Idle State besides slicing the received bits. We propose a 3-comparator scheme to achieve the required functions. The Comparator0 is used to determine Data\_0 or Data\_1 in the Active State. The Comparator1 and Comparator2 are used to detect whether the input signals on the bus is in the Idle State or not. Fig. 5 shows the schematic of the proposed receiver.

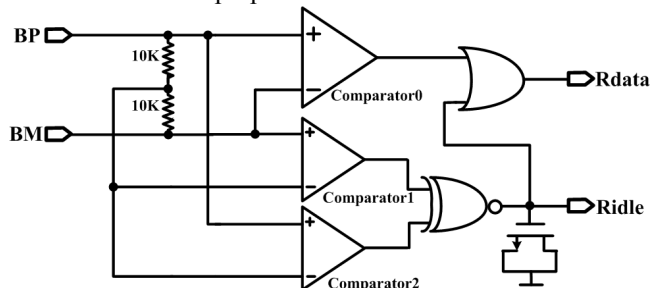


Fig. 5. The schematic of the receiver.

## III. IMPLEMENTATION AND SIMULATION RESULT

The proposed design is carried out by a typical 0.18  $\mu\text{m}$  single-poly six-metal CMOS technology. Verified by all-PVT-corner post-layout simulations, the throughput of the transmitter and the data rate of the receiver can reach 40 Mbps in a single channel. Fig. 6 shows the worst case simulation

waveform given the data rate is 40 Mbps between the output of the transmitter ( $u\text{Bus} = \text{BP} - \text{BM}$ ) and the output of the receiver (Data). Table I and Table II show the comparison between FlexRay specification and our design.

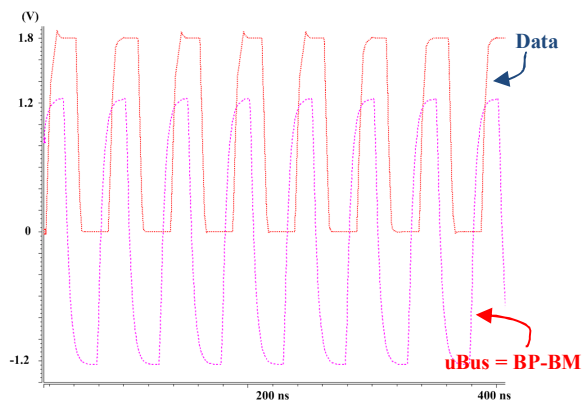


Fig. 6. Post-layout simulation (worst case).

TABLE I  
SPECIFICATIONS OF THE PROPOSED TRANSMITTER

TRANSMITTER SPECIFICATION		Simulation Result
Differential Voltage	600~2000 mV	628~1180 mV
Bias of Idle_LP	0~30 mV	~ 0 V
Slew Rate	< 100 ns	< 10 ns
Delay time	5~25 ns	< 15 ns
Throughput	10 Mbps	$\geq$ 40Mbps

(NOTE: THE LOAD OF THE TWISTED PAIR =  $40 \Omega \times 100 \text{ PF}$ )

TABLE II  
SPECIFICATIONS OF THE PROPOSED RECEIVER

RECEIVER SPECIFICATION		Simulation Result
Receiver Delay	100 ns	< 60 ns
Receiver Mismatch	5 ns	< 3 ns
Idle reaction time	50~400 ns	< 100 ns
Active reaction time	100~450 ns	< 100 ns
Data Rate	10 Mbps	$\geq$ 40Mbps

(NOTE: THE SIMULATION REACTION TIME NOT INCLUDE LOGIC DELAY IN BD)

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