A 4-kHz per °C High Linearity On-chip Temperature Sensor Implemented Using 40-nm CMOS Process

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Abstract—In this research, a standard TSMC 40-nm CMOS process is used to implement a highly linear and high resolution temperature sensor. It is composed of an averaging feedback operational amplifier relaxation oscillator controlled by a PTAT current generator. Post-layout simulations show a detection range of $0°\sim 100°C$ and a 4 kHz per °C resolution. The maximum linearity error is simulated to be 0.15% at the FF corner and 99.85% linear fit. The power consumption of the design is 0.2015 mW at the maximum output frequency = 1.57 MHz, and the area of 5291.5 μm^2.

Index Terms—temperature detection, high linearity, PTAT, current-to-frequency conversion

I. Introduction

In industrial, commercial appliance, and equipment applications, temperature sensing, and security control have grown increasingly important. It's because too much heat can lead to higher energy costs, unreliable system performance, and even equipment damage. To avoid these risks, temperature monitoring systems with temperature sensors as a crucial component are needed [1].

A recent rise in demand for CMOS temperature sensors can be attributed to their small size and low power requirements. It can also be used to monitor temperature in already-existing chips. These temperature sensors deliver outputs that are proportional to or counter-proportional to the temperature being measured in terms of voltage, current, resistance, or frequency [1]–[6]. They commonly include signal conditioning circuitry in on-chip systems.

Utilizing CMOS temperature sensors has a number of benefits, including compatibility, effectiveness, and dependability of temperature monitoring systems. Circuitry for signal filtering is integrated to streamline system design and reduce overall expenses. Consequently, CMOS temperature sensors are swiftly emerging as a preferred substitute for temperature monitoring and control applications in a variety of industries.

This paper is arranged as follows: Section II discusses the architecture of the proposed on-chip temperature sensor, Section III presents the implementation & simulation results. Lastly, the paper is concluded in Section IV.

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II. Temperature Sensor Architecture and Analysis

Fig. 1 shows the architecture of the CMOS-based temperature sensor. It is composed of a voltage averaging circuit that controls the oscillation frequency of the complementary relaxation oscillator based on [7]. Conventional relaxation oscillator offers some drawbacks such as the effects of comparator delay variation, aging currents, and flicker noise. To increase stability and lower power consumption, the averaging feedback circuit is independent of the comparator delay (t_d). The complementary relaxation is a pair of oscillators that oscillates one after the other by means of the SR latch. The circuit is identical on both sides so that the oscillation frequency of the circuits is also identical. The oscillation frequency is dependent on the PTAT current from the load transistors (M_{L101} or M_{L102}).

Referring to Fig. 2, an equivalent circuit of the half of the oscillator is shown. The timing waveform of the oscillator model is shown in Fig. 3. The relaxation oscillator output (V_{osc1} and V_{osc2}) oscillates alternately one after the other. The output oscillation frequency (V_{osc}) is the sum of the complementary oscillations. At low frequency, Vosc is equal to Vref defined by $R_x \times C_{100}$.

The oscillator output can be described using Eqn. (1), provided $R_x \gg r_{o(ML)}$.

$$V_{osc(1,2)}(t,T) = I_{PTAT}(T) \cdot R \left(1 - e^{-1/RCt}\right) \quad (1)$$

Since the feedback voltage equalizes at the DC point of the oscillator output, V_{ref} can be reconstructed as Eqn. (2).

$$V_{ref}(T) = \frac{1}{\tau} \int_\tau V_{ocs(1,2)}(t,T)\partial t \quad (2)$$

In Fig. 3, V_{ref} is a voltage divider output of the supply. Solving Eqn. (2), we get Eqn. (3).

$$\frac{[1 - \alpha(T)]\tau}{RC} = 1 - e^{-\tau/RC} \quad (3)$$

where:

$$R = r_{o(ML)}$$

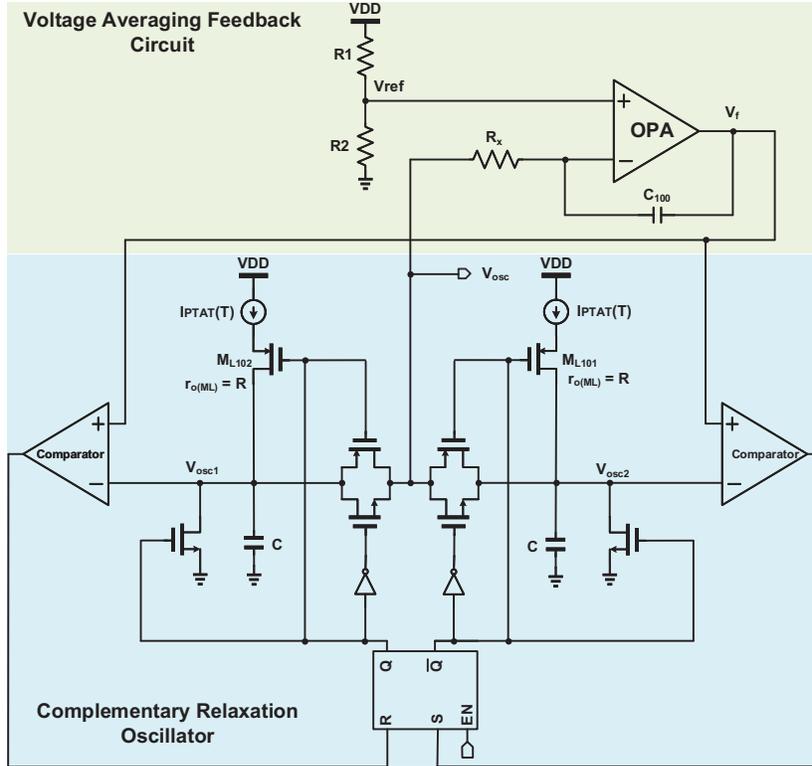$$\alpha(T) = \frac{V_{ref}(T)}{I_{PTAT}(T) \cdot R}$$

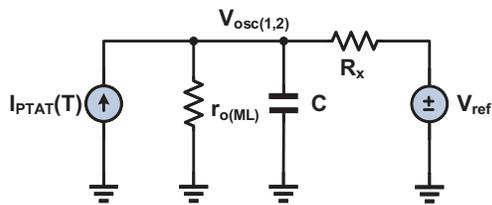Fig. 1. Schematic of the Temperature Sensor

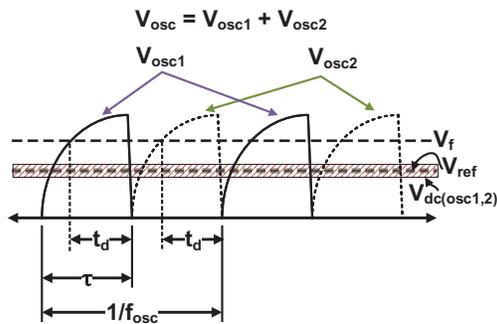Fig. 2. Equivalent circuit of half of the oscillator

Fig. 4. PTAT current generator

Fig. 3. Charge/Discharge cycle of the oscillator
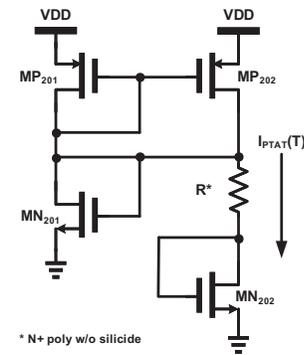
$r_{o(ML)}$ is the output impedance of either transistor M_{L101} or M_{L102}, since they are the same.

The design has the frequency coefficient (α) that is dependent on $I_{PTAT}(T)$. The PTAT current, which is affected by temperature, is generated using the circuit shown in Fig. 4. The resistor in this design is an N+ polysilicon without silicide with a negative thermal coefficient of 1.85e-3 /°C. Eqns. (4-4) shows the derivation of the PTAT current relationship with temperature.
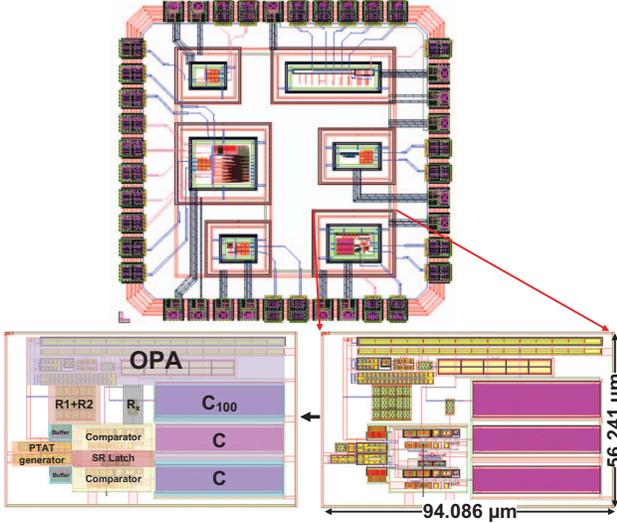
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Fig. 5. Layout of the Temperature Sensor

$$I_{PTAT}(T) = \frac{V_{GS(MN201)}(T) - V_{GS(MN202)}(T)}{R(T)} \quad (4)$$

$$\mu(T) = \frac{1}{I_{PTAT}(T)} \cdot \frac{\partial I_{PTAT}(T)}{\partial T} \quad (5)$$

$$\mu(T) = -\frac{1}{R(T)} \cdot \frac{\partial R(T)}{\partial T} + \frac{1}{R(T)}\left(\frac{\partial V_{GS(MN201)}(T)}{\partial T} - \frac{\partial V_{GS(MN201)}(T)}{\partial T}\right) \quad (6)$$

$$I_{PTAT}(T) = I_{PTAT}(T_0) \cdot [1 + \mu(T - T_0)] \quad (7)$$

where, $\mu(T)$ is the temperature coefficient of the design, and $T_0 = 27°C$.

III. IMPLEMENTATION AND SIMULATION

The temperature sensor is implemented using the TSMC TN40G 40-nm CMOS process. The sensor is part of a larger circuit that detects other chip parameters. The area of the temperature sensor is $94.086 \times 56.241 \ \mu m^2$.

Figure 6 shows the PTAT current post-layout simulation result. It can be seen that the PTAT current is highly linear with respect to temperature. A sample result at three (3) different temperatures at the SS corner is presented in Fig. 7. Referring to Fig. 8, it shows the temperature vs. frequency at all corners. It can be seen that all the plots have a highly linear fit with a worst 0.9985 R^2 fit at the FF corner. The resolution is also seen at the FF corner with 4-kHz per °C.

The performance comparison of several temperature sensors over the course of the past few years is summarized in Table I. The various designs are compared using a FOM that divides the temperature range by the temperature error detection. It can be seen that our design has the lowest linearity error of
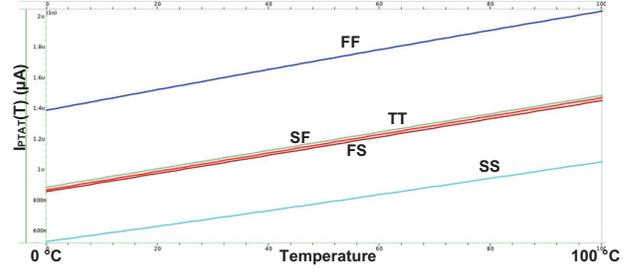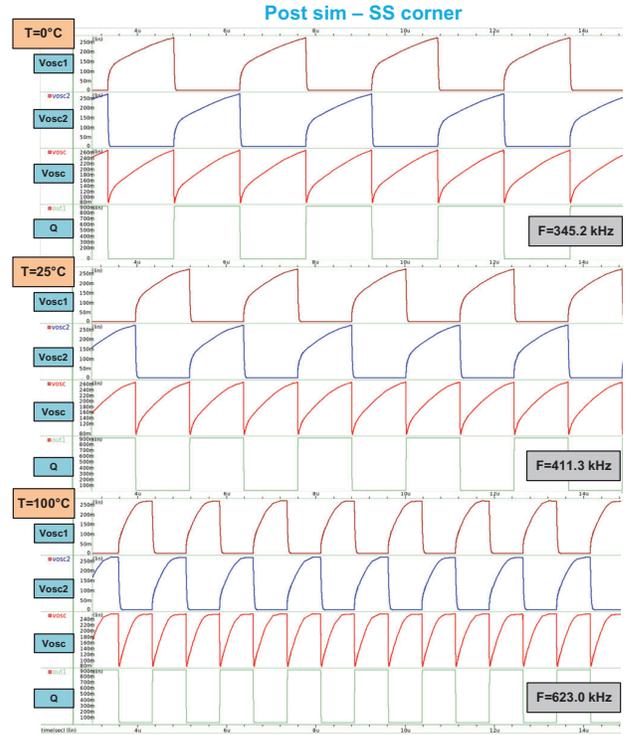

Fig. 6. Post-simulation result of the PTAT current

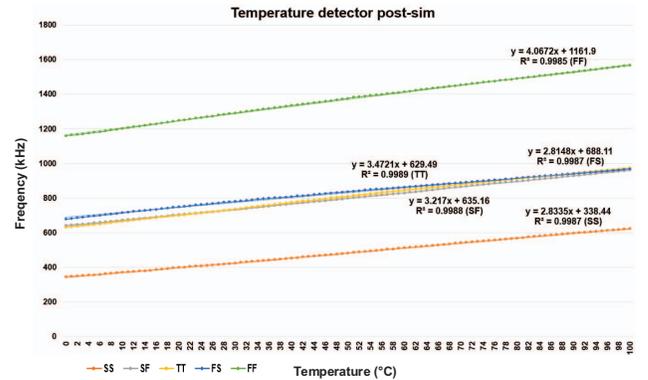Fig. 7. Post-layout simulation result at the SS corner

Fig. 8. Post-layout simulation result at all corners

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|	[8] MWSCAS	[9] TCAS-I	[10] TCAS-I	[11] SensJ	[5] IMCEC	[12] SSC-L	[6] ISOCC	Ours
Year	2017	2017	2018	2019	2019	2020	2021	2023
Process (nm)	180	180	130	50-HV	65	65	180	40
VDD (V)	0.5	0.6	1.5	5.0	0.8	0.9	3.3	0.9
Area (mm^2)	0.02	0.45	0.23	2.39	N/A	0.32	1.64	0.005
Power (W)	0.2μ	75n	1.05μ	11m	0.9μ	6.4n	48.5m	0.2m
f_{out} (kHz)	11 – 50.2	28.5– 29.3	5.3– 31.6	500– 2200	60– 85	N/A	300– 465	320– 1870
Range (°C)	0– 50	0– 100	10 100	-5– 40	0– 80	-30– 70	-40– 80	0– 100
Res. (°C)	0.5	1	0.046	1	1	N/A	3	**1**
Error (°C)	0.2	1.33	1	1.04	-1	-1	0.5	**0.28**
Lin. Err. (%)	N/A	5.5	N/A	1.42	N/A	1.7	0.392	**0.15**
FOM	250	75.18	90	43.69	80	100	240	**357**

FOM = Temp. Range/ Temp. Error
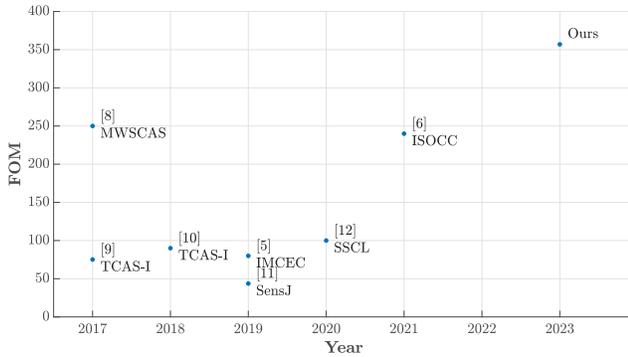
Fig. 9. Technology roadmap of on-chip temperature sensors

0.15% and have the best FOM so far. Our design is the best one yet, according to the technology roadmap in Fig. 9 of several temperature sensors.

IV. CONCLUSION

This research presents a TSMC 40-nm CMOS-implemented extremely linear temperature sensor. It is embedded with other circuit in a single-chip with an area of 5291.5 μm^2. With a resolution of 1 °C and a large detection range of 0 °C to up to 100 °C. Based on the post-layout simulations, our design obtained a high linearity with a little linearity error. Our design had the best performance to date, according to a FOM based on the temperature range and temperature inaccuracy.

ACKNOWLEDGMENT

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