2024 21st International SoC Design Conference (ISOCC) | 979-8-3503-7708-8/24/$31.00 ©2024 IEEE | DOI: 10.1109/ISOCC62682.2024.10762163

A Multi-Level Power Gating Logic Controlled Driver for A 10-V Power Transistor Using 180-nm High Voltage BCD Process

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***Abstract*—Driver designs for power transistors need to consider performance and efficiency simultaneously. This work demonstrated an active gate driver (AGD) that drives the power transistor at multiple voltage levels using a multi-level power gating logic. A power gating mechanism reduces AGD power consumption. AGD's Four-Level Balance Control Circuit ensures that all power MOS devices in the Output Stage's buffer arrays are used. The AGD was implemented using TSMC 180-nm High-Voltage BCD (Bipolar-CMOS-DMOS) technology. AGD design capability was proven using all-PVT-corner post-layout simulations with C_{load} = 2 nF and PWM frequency = 500 kHz. The static and dynamic power dissipation averages 167 mW. Finally, power gating reduces power by 122 mW, according to two cycles with and without it.**

***Index Terms*—driver, BCD, Four-Level Balance Control, multi-level power gating, power MOSFET.**

I. Introduction

Power semiconductor gate drivers must be fine-tuned for optimal switching performance due to their architectures. Tuning is crucial for reducing power losses and managing oscillations during switching events [1]. Monitoring SiC device gate voltage (V_g) is a key function of a dynamic gate driver chip during switching transients. The main goal is to create an optimum dynamic gate resistance (R_g) pattern [2]. This technique precisely locates the Miller plateau termination point to ensure a precise gate driving pattern time interval. Ringing is reduced and switching speed is increased using dynamic gate drive circuitry. However, utilizing an FPGA to enhance gate driver chip timing increases size, complexity, and cost. Hence, a multi-level power gating logic controlled driver is presented to precisely drive a 10-V power transistor from 1 to 5 V. Additionally, the driver's power gating minimizes Output Stage power dissipation.

[1]Both primary authors contributed an equivalent contribution to this work.
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★This research utilized an EDA tool provided by TSRI. Funding for this project was extended by NSTC of Taiwan through specified grant numbers, NSTC 111-2623-E-110-002-, NSTC 110-2623-E-110-001-, NSTC 110-2221-E-110-063-MY2, and NSTC 111-2218-E-002-024-.

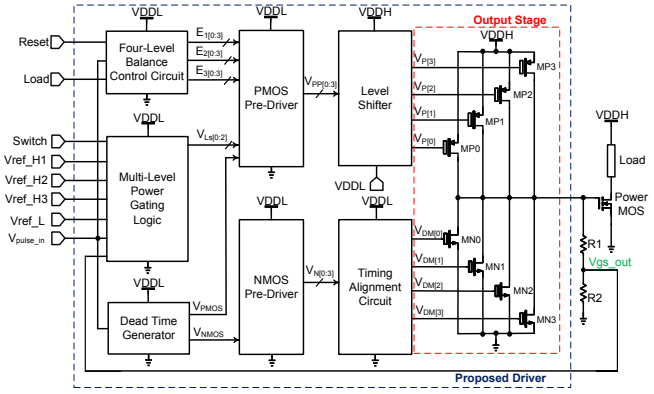

Fig. 1. Block diagram of the proposed Multi-Level Power Gating Logic Controlled driver

II. Multi-Level Power Gating Logic Controlled Driver Design

The proposed Multi-Level Power Gating Logic Controlled Driver, as shown in Fig. 1, consists of the following blocks: Multi-level Power Gating Logic, Four-Level Balance Control Circuit, Dead Time Generator (Adaptive split-path feedback circuit [3]), PMOS and NMOS Pre-Drivers (Switch Selectors [3]), Level Shifter, Timing Alignment Circuit (Delay matching [3]), and Output Stage. Supply voltages are VDDH = 10 V and VDDL = 5 V. Transistors implemented in all the blocks except the Level Shifter and the Output Stage are 5-V low-voltage MOS devices. The proposed AGD's Output Stage comprises 4-PMOS and 4-NMOS arrays, producing current in four cases. Its PMOS (MP0, MP1, MP2, and MP3) and NMOS (MN0, MN1, MN2, and MN3) devices are 12-V $V_{ds\ max}$ HV DMOS. Notably, $V_{P[0:3]}$ can be adjusted by the Level Shifter for its proper driving from 0∼5 V to 5∼10 V [4].

These scenarios consider PMOS Pre-Driver Output condition: In Case 1, with high $V_{P[0:2]}$, one PMOS (MP3) off, and three PMOS (MP0, MP1, MP2) on, 75% of the I_{max} is created, exceeding 60.7%. For Case 2, set I_{max} to 40% when

V_{gs} surpasses 60% of VDD. When $V_{P[0:1]}$ is high, MP0 and MP1 activate. They generate 50% of the I_{max}, exceeding 40%. For Case 3, I_{max} must be 20% when V_{gs} reaches 80% of VDD. Since only $V_{P[0]}$ is high, only MP0 is active. It yields 25% of I_{max}, above the required 20%. Fig. 2 shows the suggested AGD time diagram. During turn-on, V_{gs} rises when V_{pulse_in} is high and $V_{P[0:3]}$ is low. As V_{gs} rises, $V_{P[1]}$, $V_{P[2]}$, and $V_{P[3]}$ reach high levels at t_{11}, t_{12}, and t_{13} intervals. As V_{gs} rises, the power ($P_{VDDL+VDDH}$) diminishes until V_{pulse_in} drops and V_{gs} reaches 100% of VDD. This raises $V_{P[0:3]}$, resulting in $P_{VDDL+VDDH}$ = 0.

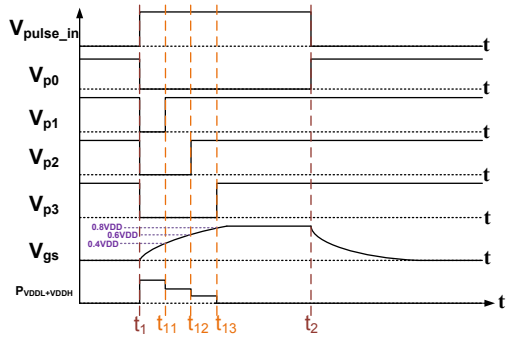

Fig. 2. Timing diagram of the proposed AGD.

One novel block in the circuit is the Four-Level Balance Control Circuit, a modified Equalizer circuit based on Ref. [3] with three PIPO shift registers instead of one. By using the V_{pulse_in} signal as clk, shift registers create different switching points for each PMOS in the Output Stage. Therefore, MOS utilization is equal and no mismatch arises. $E_{1[0:3]}$ shows four PMOS positions per level. Finally, the Multi-Level Power Gating Logic (a modified 2-level Miller detector circuit in Ref. [3]) features a block with three latch detectors for three levels. The latch detector uses two voltage references each case. The latch activates when the V_{gs} signal surpasses the other two voltage references. The latch turns off when the V_{gs} signal falls below the other voltage references. This block generates power-gating signals.

III. All-PVT-Corner Post-Layout Simulations

TSMC 180-nm HV BCD process was used to carry out the proposed AGD. Fig. 3 shows the AGD's layout and floorplan. The all-PVT-corner post-layout simulation results, as shown in Fig. 4, matches with the timing diagram in Fig. 2 at C_{load} = 2 nF and PWM frequency of 500 kHz. Table I shows the comparison of recent power MOS driver performance. Unlike our design, Ref. [2] required FPGA for optimal driver operation. The average power dissipation (P_{dis_total}), including static and dynamic power, is 167 mW with power gating at the worst corner (FF, 1.1·(VDDH, VDDL), and 0°C). Without power gating, it is 289 mW.

IV. Conclusion

An AGD with power gating for power transistors is proposed in this work that reduces power by 122 mW. It will be built and tested on silicon in the future.

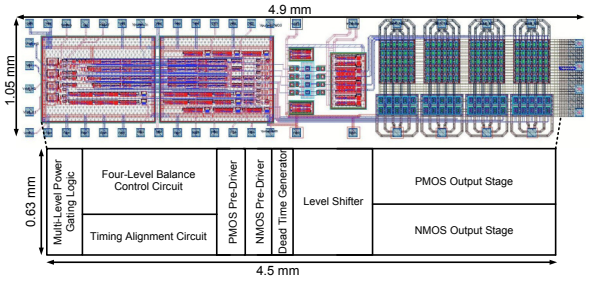

Fig. 3. Proposed AGD's layout and floorplan.

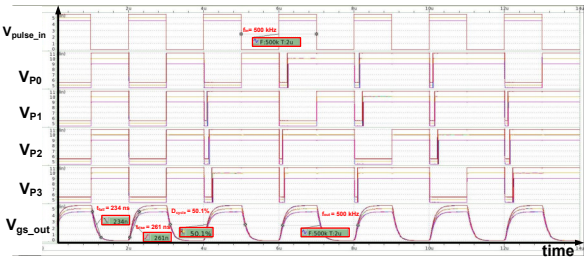

Fig. 4. All-PVT-corner post-layout simulations of the proposed AGD.

TABLE I
Recent Power MOS Drivers' Performance Comparison

	[5]	[2]	This work
Year	2018	2022	2024
Publication	JSSC	ISPSD	ISOCC
Process (nm)	180 BCD	180 BCD + FPGA	180 BCD
Driver type	Passive	Active	Active
Verification	Meas.	Meas.	Post-sim.
VDD (V)	15	1.8, 3.3 & 20	5 & 10
f_{PWM} (kHz)	1000	100	500
C_{load} (nF)	2.7	2	2
Chip area (mm^2)	4.9 x 2.3	2.5 x 2.5	4.9 × 1.05
P_{dis_total} (mW)	—	79.51*	167

*excluding FPGA's power consumption

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