Active Gate Driver Design Using Differential Timing-based Miller Detector for Power MOSFET

Pradyumna Vellanki*, Venkata Naveen Kolakaluri*, Yun-Che Chang*,
L S S Pavan Kumar Chodisetti*, Mitch Ming-Chi Chou† and Chua-Chin Wang*
*Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan 80424
†Department of Materials and Optoelectronic Science, National Sun Yat-sen University, Kaohsiung, Taiwan 80424
Email: ccwang@ee.nsysu.edu.tw

2024 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) | 979-8-3503-7877-1/24/$31.00 ©2024 IEEE | DOI: 10.1109/APCCAS62602.2024.10808912

***Abstract*—A low-power active gate driver (AGD) design becomes critical in battery-based power conversion systems (DC-DC converters) to extend battery life. This paper proposes an integrated active gate driver with a novel differential timing-based detector that detects very narrow Miller regions effectively and also incorporates the voltage mode power-gating circuit that shuts off N-1 PMOS devices in the P-channel MOS array to reduce power loss. A novel current modulation mechanism is employed to further minimize the redundant static power dissipation that occurs in the comparators during steady-state operation in the detector and power-gating circuit. The proposed AGD achieves a 15% power reduction when tested with a capacitor load of 2 nF and an input PWM signal frequency of 500 kHz using power-gating and current modulation.**

***Index Terms*—AGD, Miller region, current modulator, power-gating, P-channel MOS array, power MOSFET**

I. Introduction

A typical gate driver usually uses an open-loop control to improve SiC rising edge di/dt and dv/dt values [2]. A lot of passive and discrete off-the-shelf components make the design bulky. Also, the driver doesn't have any active feedback. Hence, it cannot compensate for variations in voltage and temperature. The active gate drivers based on programmable devices like FPGA and Microcontroller were reported to employ active feedback to determine the response in the Miller region [3]–[5]. Moreover, the feedback also adjusts for voltage and temperature variations. However, external programmable devices lead to an increase in size, power consumption, and overall cost of the AGD. Additionally, they require extensive reprogramming based on the unique characteristics of various power devices (IGBT, MOSFET, and SiC). Nevertheless, these implementations do not offer real-time output data. Another on-chip active gate driver was discussed in [7]. Though the presented AGD design occupies less area compared to prior works, the Miller detection circuit employed is too simple and sensitive to noise fluctuations. Also, the power consumption of this proposed driver is high.

In this work, an AGD design is proposed that uses the differential timing-based Miller detector (DTMD) and voltage mode power-gating circuit (VPGC) to detect the Miller plateau during power MOSFET on and off and help to reduce excess power consumed by the level shifter, respectively. The Miller plateau is detected from the power MOS feedback signals V_{GS_fb} and V_{DS_fb}, improving the detection accuracy. The proposed AGD is implemented in 0.18-μm HV CMOS, eliminating the area limitation of the AGD that uses a microcontroller and FPGA. A novel current modulation circuit is employed to reduce power loss generated by the comparators.

This work was partially funded by NSTC, Taiwan, under NSTC 112-2221-E-110-063-MY3.

II. Differential timing-based Miller detection-based active gate driver design

Fig. 1 shows the block diagram of AGD with the proposed DTMD, VPGC, and Current modulation circuit, and Balancing circuit which alters the sequence of PMOS that are turned off. The Delay optimized split-path feedback circuit detects the P-channel or N-channel MOS with slow rise time/fall time in the respective MOS arrays, and the Buffer strength profile selector determines the number of MOS devices in P and N-channel MOS arrays to be turned off during the Miller plateau transitions. The number of MOS to be turned off is determined using binary bits named, Mode inputs (M_0, M_1). The Buffer state determination circuit consists of four sub-blocks which include a voltage level shifter, a PMOS switch selector, a Delay matching, and a NMOS switch selector which will be introduced later. The P-channel MOS array and the N-channel MOS array provide different drive currents in the Miller plateau. The AGD functional blocks mentioned above are sourced from [8].

A. Differential timing-based Miller detector (DTMD)

The DTMD is depicted in Fig. 2, which uses a novel approach to accurately detect minute variations occurring in the Miller time period (T_{MPD}). T_{MPD} is defined as the phase difference between two Miller component signals, namely V_{Q1} and V_{Q2}, which are generated by the Miller component detectors (MCD) 1 and 2, respectively. The MCD utilizes the comparator pair, C1 and C2, to detect the transitions in the V_{DS_fb} signal and generate a signal whose pulse width is determined by the potential difference between the voltage references V_{H_in} and V_{L_in}. In case of MCD1, the logic gates OR and NAND determine the S_1 and R_1 inputs in the SR_1 latch. It also employs a pair of AND gates that perform the interleaving operation on S_1 and R_1, preventing the SR_1 latch from entering an undefined state. The interleaving procedure is accomplished by sending the signal V_{PWM}

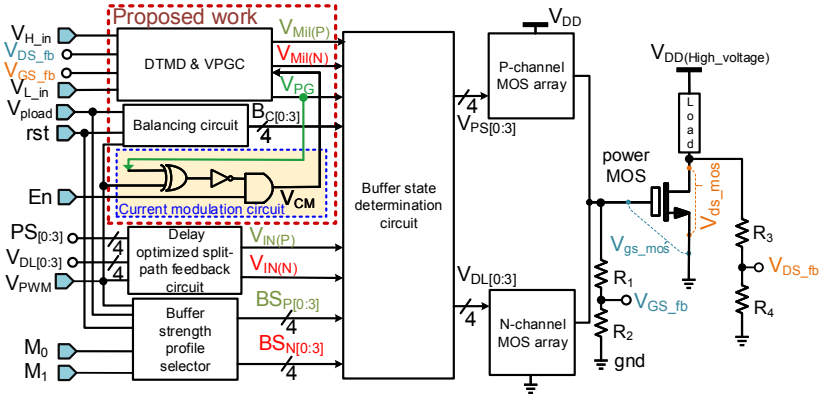

Fig. 1. Block diagram of the proposed AGD

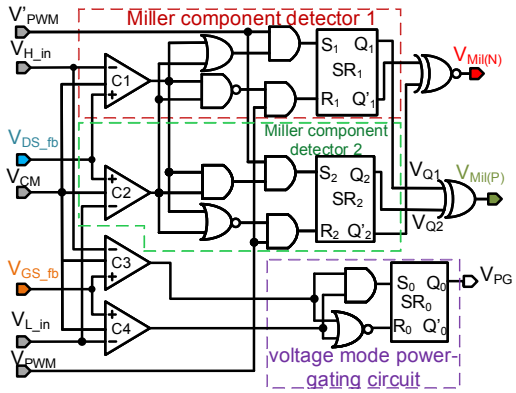

Fig. 2. Differential timing-based Miller detector (DTMD)

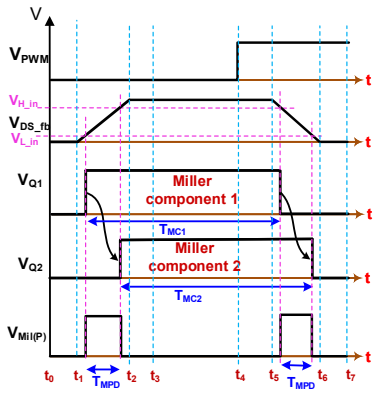

Fig. 3. Timing diagram for Miller component detection

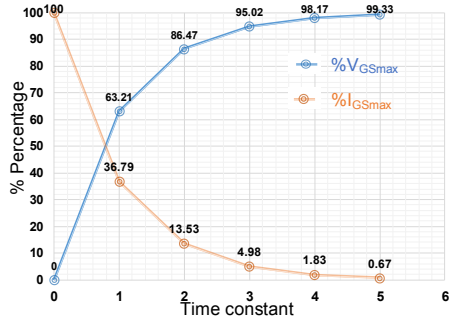

Fig. 4. RC circuit $\%I_{GSmax}$ and $\%V_{GSmax}$

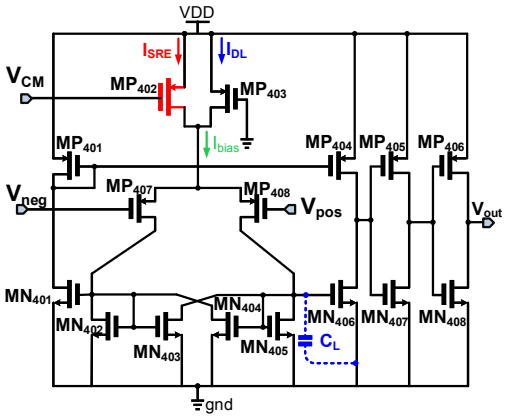

Fig. 5. Modified comparator with V_{CM} control

and its complement V'_{PWM} to the AND gates. V_{Q1} signal goes high when power MOS feedback signal V_{DS_fb} crosses voltage reference V_{L_in}, as shown in the Fig. 3. A similar explanation may be given for MCD2, with the only difference being that the V_{Q2} switches on when the V_{DS_fb} signal is more than V_{H_in} and V_{L_in}, and off when the V_{DS_fb} signal is less than $V_{H_in}$and V_{L_in}. From the timing diagram in Fig. 3, the phase shift observed in the Miller component signals V_{Q1} and V_{Q2} is proportional to the window size between the two reference voltages, V_{H_in} and V_{L_in}. As discussed earlier, the phase difference between the Miller component signals V_{Q1} and V_{Q2} is considered as the Miller time period T_{MPD}. The DTMD employs an XOR gate to generate the Miller time period detection signal for the PMOS named $V_{Mil(P)}$. Similarly, the Miller time period detection signal for the NMOS is generated using XNOR ($V_{Mil(N)}$). Upon careful observation of the timing diagram, it becomes evident that the Miller component signals V_{Q1} and V_{Q2} have a larger time period T_{MC1} and T_{MC2} compared to the Miller time

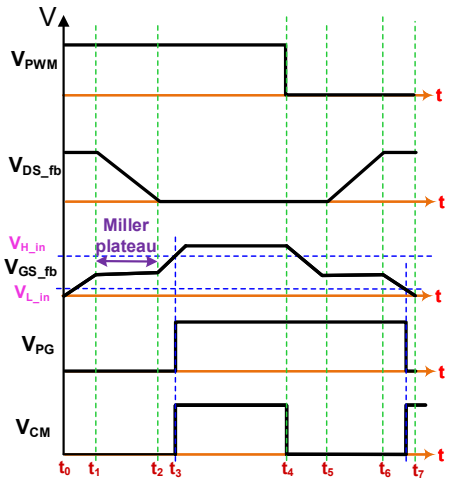

Fig. 6. Current modulation circuit's timing diagram

period T_{MPD}. Also, the variations in the width of the Miller time period don't affect the Miller component signals time period T_{MC1} and T_{MC2}, which are dependent on the V_{DS_fb} and V_{PWM} waveforms. As a result, it can be stated that the DTMD can detect very narrow Miller regions effectively while maintaining setup and hold time margins of the SR latches in the Miller component detectors [11].

B. Voltage mode power-gating circuit (VPGC)

The power-gating signal V_{PG} determines the period when the N-1 PMOS devices are switched off early to conserve power. The SR_0 latch generates the V_{PG} signal from the outputs of comparator pairs (C3 and C4) through logic gates, namely AND and NOR. The comparator pairs generate outputs based on the voltage comparison of voltages V_{GS_fb} and reference voltages V_{H_in} and V_{L_in}. In the current implementation, the SR latch is set when V_{GS_fb} is greater than V_{H_in} = 0.8×VDD and resets when V_{GS_fb} is less than V_{L_in} = 0.2×VDD.

$$\tau = R_G \cdot C_G \tag{1}$$

where R_G is resistance at the buffer output, and C_G is gate capacitance of the power MOS.

Fig. 4 depicts two curves with $\%V_{GSmax}$ and $\%I_{GSmax}$ data points plotted against the time constant (τ) RC circuit. From the graph, it becomes evident about the complementary nature of $\%V_{GSmax}$ and $\%I_{GSmax}$ curves. this complementary behavior can be better understood with the example data points at τ=3, $\%V_{GSmax}$ = 86.47, and $\%I_{GSmax}$ = 13.53 from Fig. 4. The sum of both the variables ($\%V_{GSmax}$ and $\%I_{GSmax}$) is always 100. In general, an observation can be made from the above discussion that as the voltage ($\%V_{GSmax}$) across the capacitor rises, the corresponding current ($\%I_{GSmax}$) required to charge the capacitor decreases. In the given scenario, a single PMOS device may generate 25% of I_{GSmax}, which is sufficient to fully charge C_G once it reaches 0.8VDD (80% of V_{GSmax}). The power-gating shuts off N-1 PMOS devices in the P-channel MOS array when the voltage across Cg = 0.8 VDD to reduce power consumption.

C. Current modulation cicuit

A novel current modulation circuit is employed in the proposed AGD to minimize redundant static power dissipated by the comparator pairs in the DTMD and VPGC. The comparators (C1-C4) used in Fig. 2 are modified version of the basic design referred to in [1], to achieve low static power dissipation, while maintaining a high slew rate. From Eqn. (2), the relation between comparator slew rate and bias current can be identified as proportional [10]. Hence, to achieve higher slew rates, larger bias currents need to be considered during the design of the comparator. The downside of using a larger bias current is increased static power dissipation. The current modulation circuit mitigates the excess power dissipation in the comparator by modulating the bias current when there are no transitions in the power MOS waveforms.

$$\text{slew rate} = \frac{I_{bias}}{C_L} \tag{2}$$

To implement the current modulation technique in the comparator, the bias current needs to be divided into two different components: idle current (I_{DL}) and slew rate enhancement current (I_{SRE}). I_{DL} is the minimum required current value by the cross-coupled comparator structure to maintain the output state. As the name suggests, the slew rate enhancement current I_{SRE} enables the comparator to achieve faster transitions. Based on Eqn. (2), we can conclude that I_{SRE} needs to be much larger compared to I_{DL} to facilitate a high slew rate.

$$I_{bias} = I_{SRE} + I_{DL} \tag{3}$$

$$I_{SRE} \gg I_{DL} \tag{4}$$

where I_{bias} is total bias current in the comparator circuit, I_{SRE} is the current flowing through the transistor MP_{402} and I_{DL} is the current flowing through the transistor MP_{403}. Fig. 5 depicts a detailed circuit of these comparators (C1-C4).

In the proposed design, the currents I_{DL} and I_{SRE} are generated using two PMOS transistors connected in parallel, namely MP_{402} and MP_{403}, as shown in Fig. 5. To generate the larger I_{SRE} current, the width of the PMOS transistor should also grow proportionally. Assuming both the transistors are designed to have the same lengths to maintain symmetry. Therefore, the width of MP_{402} is 20 times wider than that of MP_{403}. While the PMOS transistor MP_{403} is always maintained in the triode region by grounding the gate terminal, the PMOS transistor MP_{402} is controlled by current modulation logic (V_{CM}). The signal V_{CM} is generated by applying XOR logic to the signals V_{PWM} and V_{PG}. The XOR gate detects the transition between V_{GS_fb} and V_{PG}, where the Miller plateau occurs. As illustrated in Fig. 6, the Miller plateau occurs twice in the timing diagram between the regions t_1-t_2 and t_5-t_6. The V_{CM} signal goes high only when the signal V_{PG} and V_{PWM} are maintained in the same state, which signifies that the comparator bias current is reduced to I_{DL} and I_{SRE} switched off through MP_{402}. Since no transitions

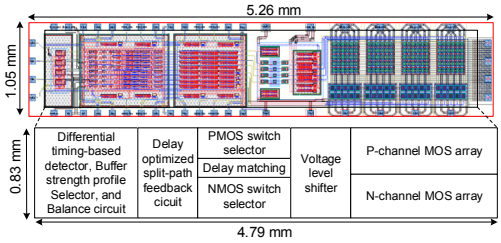

Fig. 7. Layout of proposed AGD

occur in V_{DS_fb} signals, the comparators in the detectors only need to maintain their previous states. Eqn. (5) depicts the logic to generate the V_{CM} signal.

$$V_{CM} = \overline{(V_{PWM} \oplus V_{PG})} \cdot E_n \tag{5}$$

where V_{PWM} is input PWM signal, V_{PG} is power-gating signal from VPGC, E_n is the master enable signal. The minimized current during the period t_3-t_4 in Fig. 6 results in reduced average power dissipation of the proposed AGD.

III. Simulation and Analysis

Fig. 7 shows the layout of the proposed AGD developed with the T18HVG2 process. The chip area is 5.26×1.05 mm^2, and the core area is 4.79×0.83 mm^2. To verify the functionality of the detection and logic blocks, all-PVT-corner post-layout simulation of the proposed AGD is performed, and the Buffer state determination circuit outputs are probed. Additionally, to further assess the detection accuracy of the DTMD, a reference gate-source signal (V_{GS_fb}) from the Infineon datasheet is introduced as a piecewise linear signal [9]. Fig. 8 depicts the post-layout simulation outcome of the Buffer state determination circuit operating at mode input M_1M_0=01. In this mode, only one MOS in the P and N channel MOS array turns off during the Miller plateau. The Balancing circuit pattern is highlighted in Fig. 8 which depicts an altering sequence of MOS that turns off during the Miller plateau over four cycles of V_{PWM}. Fig. 9 shows the plot of power consumed in all-PVT-corner simulations when V_{CM} Enable is on and off. From the plot, it can be said that the power consumed by the AGD varies concerning the corner parameters. Also, lower power consumption is observed across all the corner parameters when current modulation is enabled. At corner FF, 25°C, 5.5 V, 11 V, the highest power consumption (P_{avg}) averaged over 6 cycles of V_{PWM} occurs, which reaches 280 mW and 221 mW with the current modulation disabled and enabled, respectively. The comparison with prior works is shown in Table I.

IV. Conclusion

This work investigates an AGD design for power MOS developed in the T18HVG2 process. The TMDC can detect minute differences in the Miller region accurately without having any effect on SR latch setup and hold margins. The VPGC reduces the power dissipated by the voltage level shifter. The novel Current modulation circuit further reduces

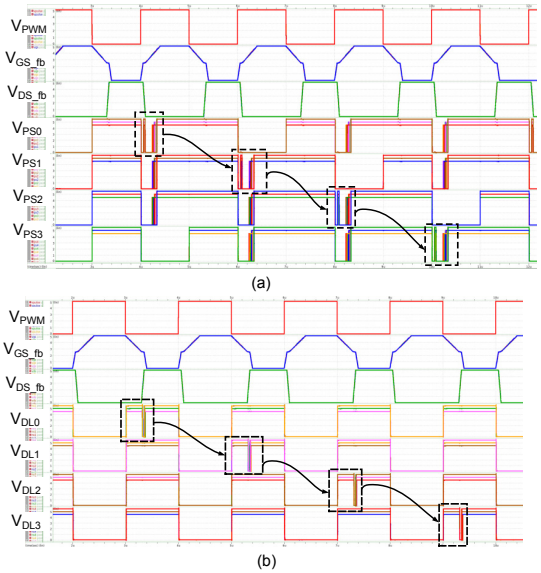

Fig. 8. All-PVT-corners post-layout simulation of Buffer determination circuit (Mode:01), (a) V_{PS} (PMOS control signal) ; (b)V_{DL} (NMOS control signal)

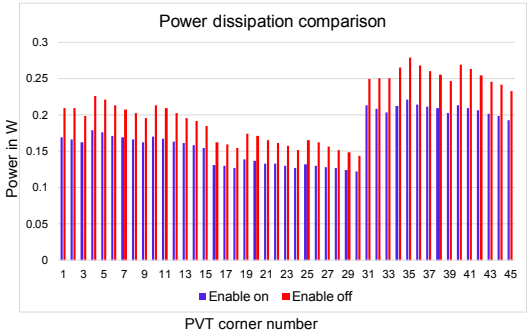

Fig. 9. Power consumption comparison data across all PVT corners

TABLE I
Performance Comparison

	[6]	[7]	This work
Year	2022	2023	2024
Publication	ISPSD	MWCAS	
Technology (μm)	0.18 BCD + FPGA	0.18 T18HVG2	0.18 T18HVG2
Driver type	Active	Active	Active
Verification	Meas.	Post-sim.	Post-sim.
VDD(V)	1.8, 3.3 & 20	12	5 & 10
f_{PWM} (MHz)	0.1	0.5	0.5
t_{rise} (ns)	—	153 at 12V	28.4 at 10 V
t_{fall} (ns)	—	187 at 12V	36.1 at 10 V
C_{load} (nF)	2	2	2
Chip area (mm^2)	2.5 x 2.5	4.5 x 3.2	5.26 × 1.05
P_{dis_total} (W)	0.079*	32.7	0.21

*not including FPGA power

the power dissipated by the comparators in the DTMD and VPGC. A guaranteed power reduction of 15% is achieved by the proposed AGD tested with capacitor load C_{load}=2 nF and input PWM signal frequency F_{PWM}=500 kHz through power-gating and current modulation.

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