A 5 V_{pp} 10-bit 100 MS/s Current-Steering DAC As MZM Drivers of PNN Systems

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***Abstract*—Photonic neural networks (PNNs) mark a significant leap forward for future AI systems. The efficacy of PNNs is significantly dependent on their supporting driving electronics, especially digital-to-analog converters (DACs) to drive optical modulators. In this investigation, we present a 10-bit current-steering DAC with a high voltage range of 5.54V and operates at 100 MHz, designed using TSMC's T18HVG2 process technology, an ideal choice for this application. The DAC's core area measures 345 μm $\times$ 1400 μm, while the overall chip area is 833 μm $\times$ 2068 μm. Our design achieves a maximum integral nonlinearity (INL) of 0.422 LSB and a maximum differential nonlinearity (DNL) of 0.145 LSB. The DAC demonstrates strong spectral performance with a spurious-free dynamic range (SFDR) of 66.5 dB.**

***Index Terms*—PNN, MZM, Current-Steering DAC, INL, DNL, SFDR**

I. Introduction

Photonic neural networks (PNNs) have emerged as a promising solution for next-generation AI systems [1]. However, the realization of PNNs requires sophisticated analog-to-digital (ADC) and digital-to-analog conversion (DAC) technologies that can interface effectively with both the digital and photonic components of the system. A key component of PNN is the Mach-Zehnder Modulator (MZM), which converts electrical signals into optical signals and enables critical operations like matrix-vector multiplications. The performance of MZMs heavily relies on their driving electronics, particularly digital-to-analog converters (DACs) [2]. The Current-Steering DAC (CS-DAC) architecture is well-suited for this task due to its speed and scalability. However, challenges arise in adapting it to meet the demands of MZMs used in PNNs. A PNN prototype realized by our team is demonstrated in Fig. 1. This research is focused on designing a wide-range CS-DAC with reasonable speed trade-offs and high current cell impedance to minimize the effect of the finite impedance of conventional CS-DACs.

There are two popular types of CS-DACs: binary-weighted and thermometer-coded. The binary-weighted CS-DAC is prone to surges during switching and timing errors [3]. However, the thermometer-coded CS-DAC requires a thermometer-decoded circuit, which occupies more area than the current sources as the number of bits increases [4]. However, this architecture switches only one current source one by one, resulting in better integral non-linearity (INL) and differential non-linearity (DNL). In this work, a hybrid architecture is used to achieve better performance in INL, DNL, glitch, monotonicity, area, and complexity.

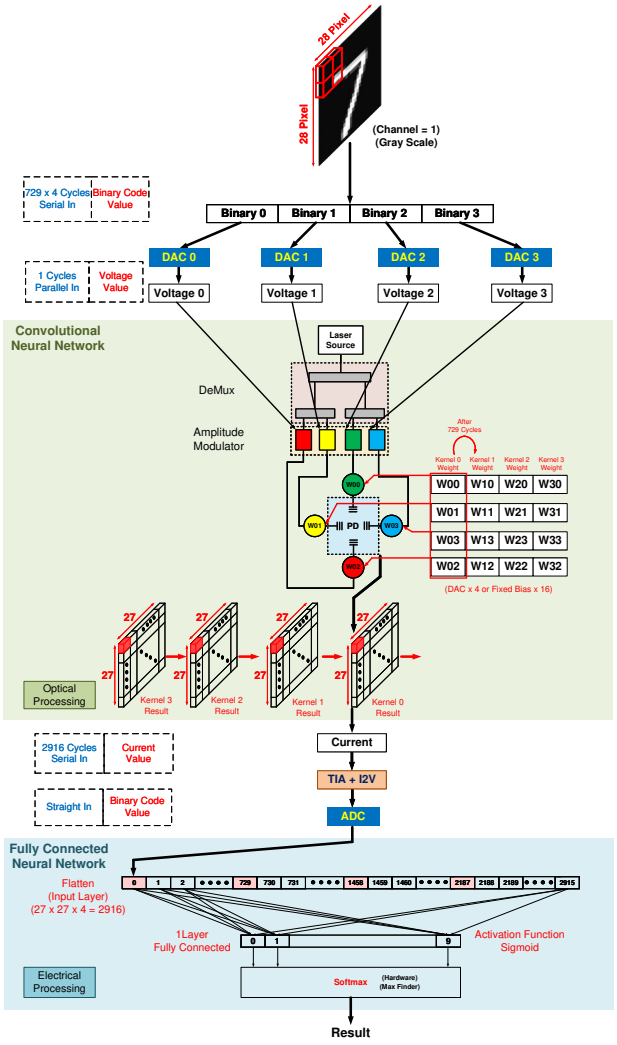

Fig. 1. The prototype of the PNN system

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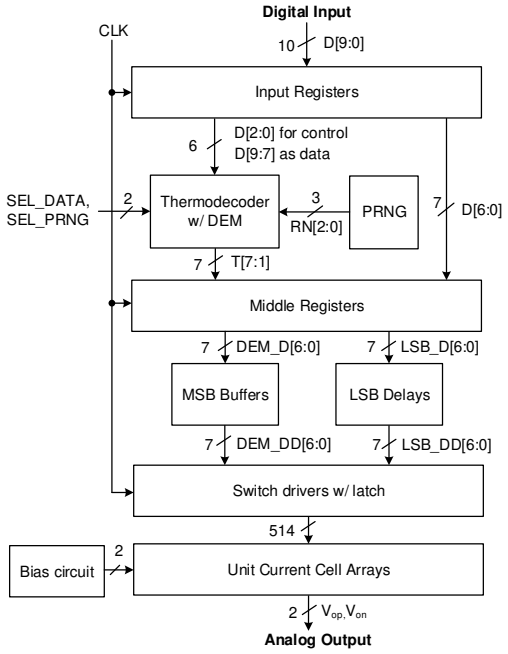

Fig. 2. Proposed 10-bit current-steering DAC architecture

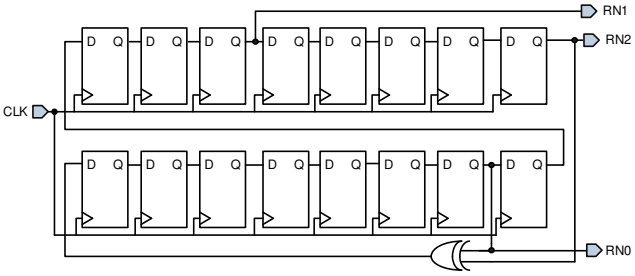

Fig. 3. Schematic of the PRNG

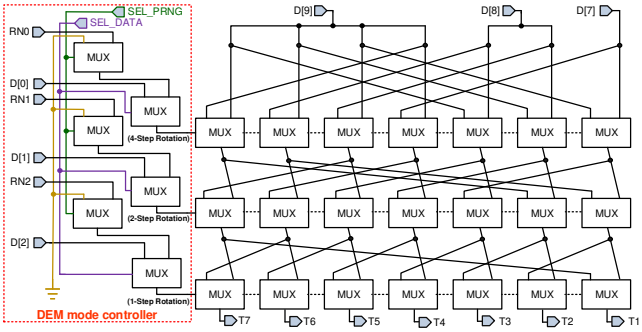

Fig. 4. Schematic of the Thermodecoder with DEM

The dynamic performance of the CS-DAC is primarily influenced by mismatch-induced non-linearity and finite output impedance. In this work, Dynamic Element Matching (DEM) and a High Voltage MOSFET (HV MOS) designed to operate in the saturation mode, are employed to mitigate amplitude and timing mismatches, code-dependent impedance variations, and fabrication gradients. These enhancements significantly improve the overall performance. The objective is to develop a DAC with high precision, a wide output range of 5 V_{pp}, and excellent linearity, optimized for the PNN applications.

II. Proposed 10-bit Current-Steering DAC

Fig. 2 illustrates the architecture of proposed 10-bit current-steering DAC. The 10-bit input digital signals D[9:0] are applied to Input Registers. The three most significant bits (MSB), D[9:7], and the three least significant bits (LSB), D[2:0], are directed to the thermometer-code decoder (Thermodecoder). The output of the Thermodecoder with DEM, T[7:1], can be controlled through pseudo random number generator (PRNG) randomization. The Middle Registers are filled with T[7:1] and D[6:0]. From Middle Registers, Thermodecoder bits, DEM_D[6:0], and binary-weighted, LSB_D[6:0], bits are forwarded to the MSB Buffers and LSB Delays, respectively. These MSB buffering, and LSB delay mechanisms are introduced at the middle stage to ensure signal synchronization and reduce timing errors caused by variations in signal arrival times at the Switch drivers. In addition, to ensure an equal load across all Switch drivers, each driver is connected to four Unit Current Cells. Dummy Unit Current Cells are added for the two LSB bits to achieve uniform loading among the Switch drivers, aligning with timing requirements and the intended voltage levels at the crosspoint. The Switch drivers are designed with a high crosspoint voltage, which is essential for preventing the interruption of current flow and enabling make-before-break operations. The global bias to supply the necessary voltages for the circuit's operation is generated by the Bias circuit [5].

A. PRNG

Fig. 3 shows the schematic of PRNG, utilizes a 16-stage TSPC flip-flop chain with a single XOR gate as a feedback. The prime polynomial of the PRNG is given in Eqn. 1. The circuit generates three pseudo-random outputs, labeled RN0, RN1, and RN2. These outputs controls the Thermodecoder to perform DEM, thereby improving the circuit's overall dynamic performance.

$$f(x) = x^{16} + x^7 + 1 \quad (1)$$

B. Thermodecoder with DEM

Fig. 4 shows the schematic of Thermodecoder with DEM. The DEM mode controller, enclosed within the dashed red line, can randomize its operation using either the outputs of the PRNG or D[2:0], selectable via external control lines. The right side of the circuit is a rotator called Random Rotation-Based Binary Weighted Selection (RRBS) [6]. Each stage of the MUX represents a different degree of rotation. Specifically, the MUX stages shift the output by 4, 2, and 1, respectively. The operational principle involves using pseudo-random numbers to randomly shift the current sources, ensuring that the digital code switches to a different current source with each operation. This approach helps to attenuate mismatch-induced

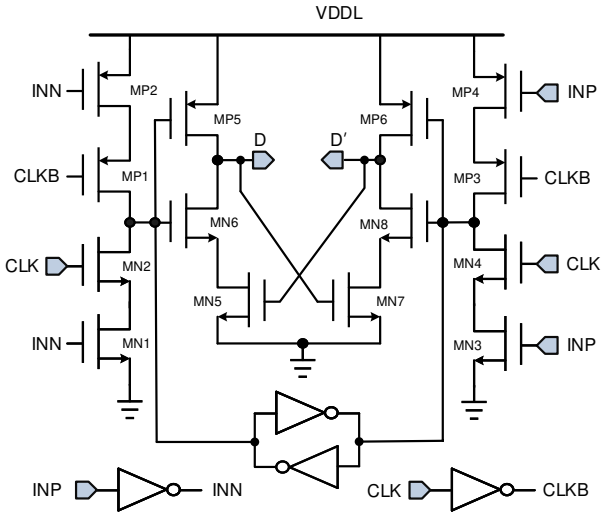

Fig. 5. Schematic of the Switch driver

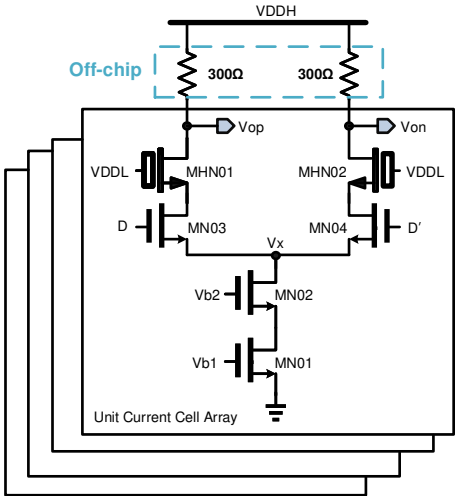

Fig. 6. Schematic of the UCC

third harmonic tones at the expense of a slightly elevated noise floor. As a result, both the dynamic performance and the overall static performance (INL and DNL) are significantly improved.

C. Switch driver

Fig. 5 shows the schematic of Switch driver, is designed in such a way that the signal interchange point is set to be higher than VDDL/2. This Switch driver circuit resolves the voltage drop that might occur when switching the circuit. Instead of using pass-transistor type latch, a CMOS type (MN1∼4, MP1∼4) is used to speed up the operation and minimize the effect of clock feed-through.

D. Unit Current Cell (UCC)

Fig. 6 shows the schematic of UCC. Cascaded current sources (MN01, MN02) are utilized in the proposed design to

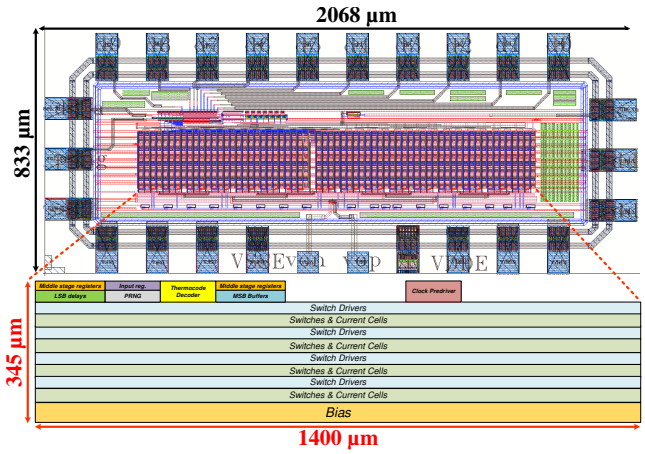

Fig. 7. Layout and floor plan of the proposed DAC

enhance the current source output impedance. These current sources are designed with careful consideration between area and precision using the Mismatch model [7]. The switches MN03 and MN04 are connected to the output of the Switch driver with a make-before-break signal transition. MN03 and MN04 are designed with a minimum transistor size to reduce the switching parasitic on node Vx. On top of the UCC is the HV MOSFETS (MHN01, MHN02), biased with VDDL, which is 1.8V in this design. The HV MOSFET is placed in between to make sure that the lower operating voltage part wouldn't be accessed by the VDDH, leveraging the advantage of a high drain-source breakdown voltage. Also HV MOSFET can protect the circuit getting breakdown from VDDH. It is also designed to be operating in the saturation mode, given extra impedance to the current sources, and attenuates the effect of finite impedance, since both INL and SFDR can be significantly affected by lack of impedance compared to the load resistor [8].

III. Post-Layout Simulations

The proposed 10-bit CS-DAC is realized using the TSMC T18HVG2 process, operating at a clock frequency (F_s) of 100 MHz. The area of the core circuit is 1400 × 345 μm^2. The layout and floor plan are shown in Fig. 7. The supply voltages used for VDDH and VDDL are 5 V and 1.8 V, respectively. The two off-chip load resistors of 300 Ω each are used, and the full-scale current is 9.5 mA in this design. The peak-to-peak output voltage is 5.54 V, is shown in Fig. 8. Static performance results, including INL and DNL are presented in Fig. 9. The maximum value of INL is 0.422 LSB, while the maximum value of DNL is 0.145 LSB. For dynamic performance, the SFDR spectrum is analyzed for F_{in} = 292 kHz (DC) and F_{in} = 49.2 MHz (almost 0.5 F_s) are depicted in Fig. 10 and Fig. 11, respectively. The SFDR at DC ($SFDR_{DC}$) is 66.5 dB, and the SFDR near Nyquist ($SFDR_{NYQ}$) is 64.2 dB. Across the first Nyquist zone, the SFDR drops only by 2.3 dB, and the consumed power is 50.5 mW.

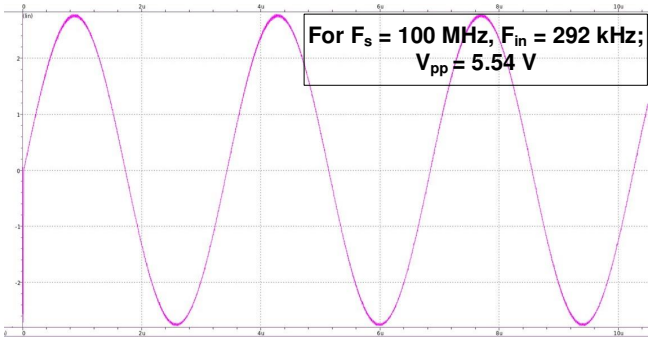

Fig. 8. The output voltage waveform of the DAC

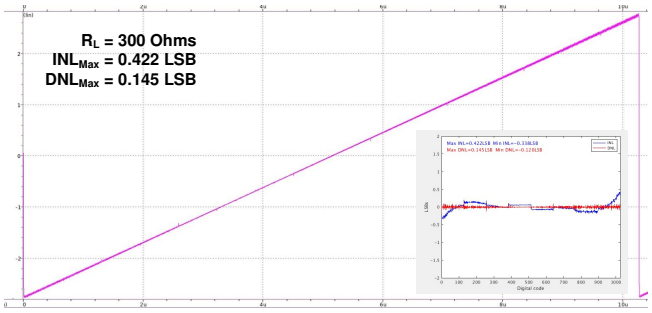

Fig. 9. Static performance simulation results along with MATLAB plot

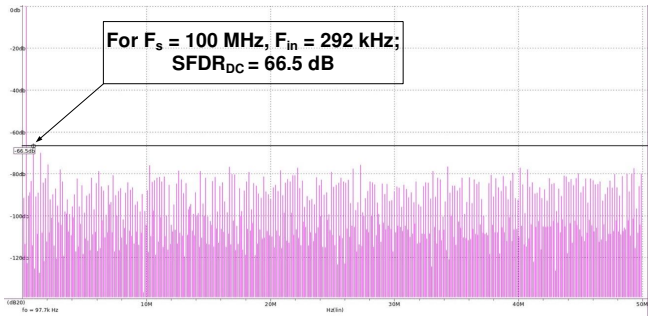

Fig. 10. The SFDR spectrum at DC input

A summary of the performance comparison between our work and earlier DAC studies is illustrated in Table I. Our DAC is the only solution realized using HV CMOS to meet the demand of MZM driver used in the PNN systems.

IV. Conclusion

This study demonstrates the successful design of a 10-bit current-steering DAC with a wide voltage range, achieving enhanced static and dynamic performance. The DAC's suitability for photonic neural network (PNN) applications highlights its potential to advance AI hardware technologies. Notably, the design maintains robust performance, with only a 2.3 dB drop observed in the Nyquist region, underscoring its efficiency and reliability. These results contribute to the development of high-performance DACs tailored for cutting-edge photonic computing systems.

TABLE I
Performance Comparison

Parameter	[8]	[9]	[10]	Our work
Technology	180 nm	180 nm	180 nm	180 nm
CMOS	Normal	Normal	Normal	HV CMOS
Resolution	10 bits	10 bits	14 bits	10 bits
Sampling Rate (MS/s)	400	500	3000	100
Supply Voltage (V)	1.8	1.8	1.8	1.8/5
$SFDR_{DC}$ (dB)	58	68.7	60	66.5
$SFDR_{NYQ}$ (dB)	49	56	52	64.2
INL_{Max} (LSB)	1.5	1.26	NA	0.422
DNL_{Max} (LSB)	2.6	1.22	NA	0.145
Power (mW)	20.7	42	600	50.5
V_{pp}(V)	0.575	0.5	1	5.54

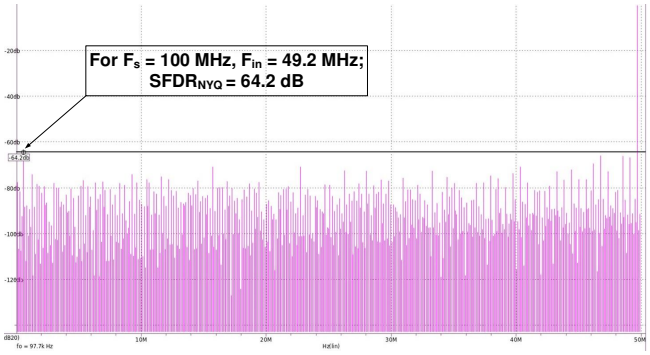

Fig. 11. The SFDR spectrum at near Nyquist input

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