A 10-bit 100 MS/s V_{CM}-based Switching Analog-to-Digital Converter for PNN systems

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***Abstract*—This paper presents the design of a 10-bit, 100 MS/s V_{CM}-based switching Analog-to-Digital Converter (ADC) using the TSMC 40 nm process as a crucial component of the optical-electrical (O-E) interface in photonic neural networks (PNNs), an emerging technology in next-generation AI. A successive approximation register (SAR) architecture is employed, incorporating a fully custom unit capacitor design in the capacitor array of the digital-to-analog converter. This design minimizes parasitic effects and enhances precision, ensuring efficient signal sampling. The proposed design features a compact core area of 117.84 μm $\times$ 162.225 μm and a total chip area of 381.245 μm $\times$ 713.61 μm. It achieves an $SFDR_{DC}$ = 67.9209 dB, an $SNDR_{DC}$ = 55.5257 dB, and an ENOB = 8.9312 when tested with a DC frequency input of 2.25 MHz. At an input frequency close to the Nyquist frequency (43.85 MHz), the ADC attains an $SFDR_{NYQ}$ = 61.6105 dB, an $SNDR_{NYQ}$ = 51.1768 dB, and an ENOB = 8.2088. The ADC demonstrates a power consumption of 896 μW at 2.25 MHz input frequency.**

***Index Terms*—V_{CM}-based, CDAC, CMP, SAR ADC, SFDR, SNDR, ENOB**

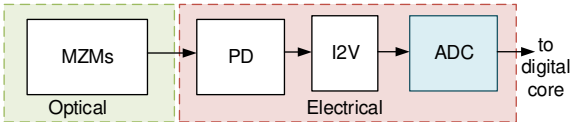

Fig. 1. O-E interface in PNN system

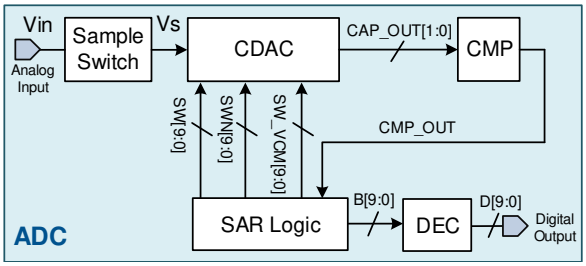

Fig. 2. Proposed 10-bit SAR ADC

I. Introduction

Photonic neural networks (PNNs) have emerged as a promising solution for next-generation AI systems [1]. However, the realization of PNNs requires sophisticated analog-to-digital (ADC) and digital-to-analog conversion (DAC) technologies that can interface effectively with both the digital and photonic components of the system. A key component of PNN is the Mach-Zehnder Modulator (MZM), which converts electrical signals into optical signals and enables critical operations like matrix-vector multiplications. The MZM optical output needs to be converted into an electrical signal according to the light intensity. A photodetector (PD) and a Transimpedence Amplifier (TIA) generate current relative to the light intensity. The optical-electrical (O-E) interface in the PNNs is illustrated as shown in Fig. 1. The current is converted to voltage using I2V circuitry. Finally, the analog voltage signal is converted to the digital signal using an analog-to-digital converter (ADC). The most popular ADC architectures are pipeline [2], delta-sigma, flash, and successive approximation (SAR) [3]–[7]. The SAR ADC architecture is well-suited for this task due to low power requirements. However, challenges arise in adapting ADCs to meet the demands of MZMs used in PNNs.

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II. Proposed 10-bit V_{CM}-based Switching Analog-to-Digital Converter

As shown in Fig. 2, the Analog Input signal (Vin) passes through a Sample Switch, which transmits the sampled voltage (Vs) to the capacitor digital-to-analog converter (CDAC). The Sample Switch used in this design is a bootstrapped switch, performs the S/H function [3]. The comparator (CMP) compares the voltage outputs of the CDAC, and the comparison result is sent to the SAR logic circuit. Based on the comparison results, the SAR logic circuit adjusts the switches in the CDAC accordingly. Finally, the results of ten comparisons are then sent to the digital error correction logic circuit (DEC) for final correction, generating a 10-bit Digital Output (D[9:0]).

A. CDAC

1) V_{CM}-based switching and Capacitor Array: This circuit employs V_{CM}-based capacitor switching. In the sampling phase, all capacitor switches are connected to the common-mode voltage V_{CM}, as shown in Fig. 3. Once sampling is completed, the Sample Switch is dissociated, and the CMP performs the primary comparison without any energy loss. Based on the comparison result, the bottom plate of the MSB capacitor in the Capacitor array corresponding to the larger

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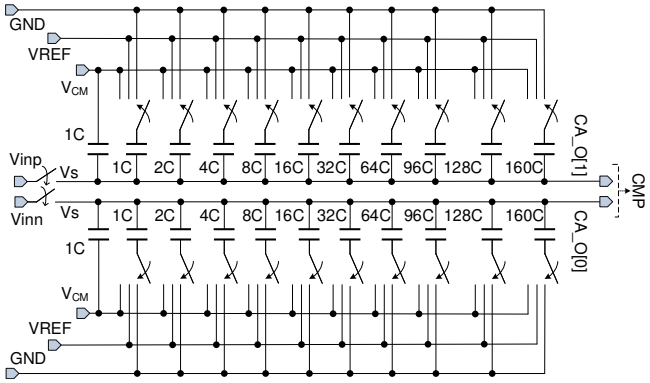

Fig. 3. Capacitor array

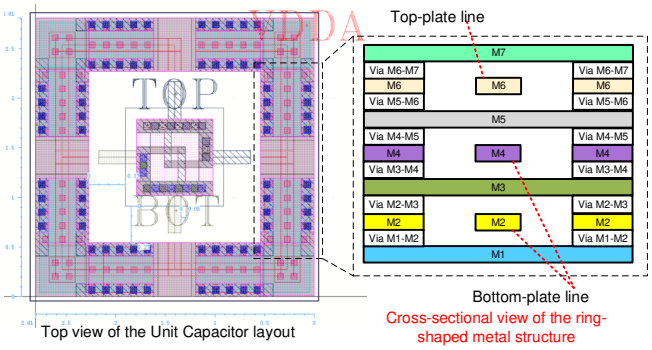

Fig. 4. Unit capacitor layout and ring metal wiring cross-sectional view

comparator input signal is switched to GND. Conversely, the bottom plate of the MSB capacitor on the other side is switched to VREF. Compared to monotonic capacitor switching, this technique reduces energy consumption by approximately 50% per switching operation [4]. The Capacitor array adopts the sub-radix-2 algorithm. Unlike a traditional binary array, the largest 256C capacitor in this design is split into a 160C capacitor and a 96C capacitor, such that the ratios between adjacent capacitors are no longer integer multiples of 2. While this approach may introduce comparison errors, it offers greater tolerance for such errors [5]. The trade-off is an additional comparison step and the need for a DEC to adjust the comparison results, which is considered an affordable tradeoff.

2) Unit capacitor: The capacitor utilized in this circuit is a fully custom-designed component meticulously designed to meet the requirements. In this design, the Capacitor array employs a top-plate sampling technique, wherein the metal layer M7 and the metal layer M3 serve to enclose the intermediate metal layers (M4, M5, and M6) within the capacitor's framework. M3 and M7 are linked to the bottom plate, ensuring that the bottom plate envelopes the top plate, thereby mitigating parasitic effects on the top plate during the sampling process. This design strategy significantly enhances the precision of the sampled analog signal and maximizes capacitance per unit area, thereby optimizing spatial efficiency.

TABLE I
CHARACTERISTICS OF DIFFERENT CAPACITORS

cap	ideal (Cu)	Ratio (%)	Practical (fF)	Ratio2 (%)	Diff (%)
160C	160	31.25	65.7627	31.2562727	0.0062727
128C	128	25	52.5053	24.9551794	-0.044820
96C	96	18.75	39.4041	18.7283262	-0.021673
64C	64	12.5	26.2572	12.4797522	-0.020247
32C	32	6.25	13.1514	6.25071272	0.0007127
16C	16	3.125	6.58408	3.12933928	0.0043392
8C	8	1.5625	3.33756	1.58630478	0.0238047
4C	4	0.78125	1.67209	0.79472559	0.013475
2C	2	0.390625	0.863384	0.41035671	0.0197317
1C	1	0.1953125	0.45379	0.21568129	0.0203687
1C	1	0.1953125	0.406803	0.19334889	-0.001963
Ctotal	512		210.398407		

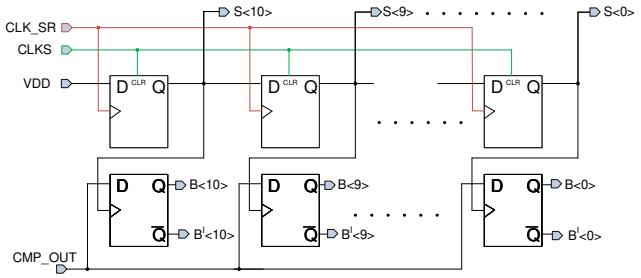

Fig. 5. Shift register and data register schematic

Furthermore, each unit capacitor is encircled by a protective ring-shaped metal structure, which connects to the VDD voltage and comprises all metal layers M1 through M7. The metals M2 and M4 allocate spaces for routing the bottom plate between unit capacitors, while M6 is designated for top-plate routing. The remaining layers (Metals M1, M3, M5, and M7) are also connected to VDD to mitigate coupling parasitics and shield against external noise interference within the routing pathways.

The layout of the unit capacitor design, along with the internal routing of the ring metal, is illustrated in Fig. 4. After extraction, it measures that the capacitance of the unit capacitor is 0.4 fF, and the layout method mentioned above allows this capacitor array to use such a small unit capacitance while still ensuring that the ratio between the capacitances meets the design. The ratios and error values between capacitances obtained from extraction, as shown in Table I.

B. CMP

The CMP circuit used in this circuit is a dynamic voltage comparator. It utilizes the control signal (CLK) to determine when to perform the comparison. This approach can effectively reduce the risk of the comparator not working. It also effectively reduces the risk of comparator malfunction while optimizing timing and power consumption to minimize overall circuit power consumption [8].

C. SAR logic

1) Shift Register & Data Register : Fig. 5 illustrates the Shift Register and Data Register circuit integrated into the

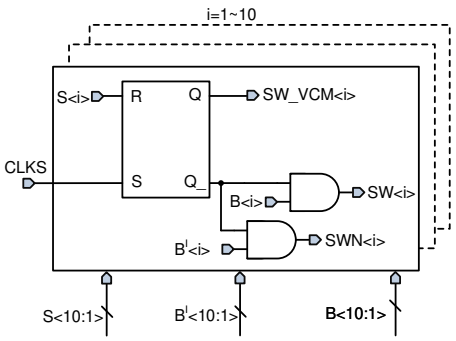

Fig. 6. Switch Control circuit

SAR Logic. A D flip-flop (DFF) is employed to track the current stage of the conversion process and store the results of each comparison.

The upper row of DFFs functions as a shift register, controlled by a dedicated control signal (CLK_SR). This row is reset when the sampling control signal (CLKS) transitions from 0 to 1. With each comparison, a high level is sequentially passed to the next flip-flop.

The lower row of DFFs serves as the data register, storing the results of the current comparison. Each DFF in this row is controlled by the output signal (S<n>) of the corresponding DFF in the upper row of the shift register. When (S<n>) transitions from 0 to 1, it indicates that the bit comparison has been completed. Consequently, the corresponding DFF stores the comparison result and outputs the data to the next-level Switch Control circuit, enabling the capacitor array switch to be adjusted in preparation for the next comparison.

2) Switch Control: Fig. 6 illustrates the Switch Control circuit designed to implement V_{CM}-based switching. The RS latch controls the switch, initially connecting it to the VCM potential until the corresponding bit comparison is completed. It then switches to either the reference voltage (VREF) or ground (GND), depending on the comparison result. At the start of the next sampling phase (CLKS = 1), all VCM control signals (SW_VCM<n>) are set to 1, ensuring that all switches are reconnected to the VCM potential.

3) Synchronous Clock: The control signal (CLK_SR) used by the SAR Control of this circuit and the control signal (CLKC) used by the comparator are both generated inside the circuit so that the entire circuit only needs one sampling signal (CLKS) as the control input. The circuit used to generate these control signals is shown in Fig. 7. It is composed of an AND gate and many specially designed inverters as delays.

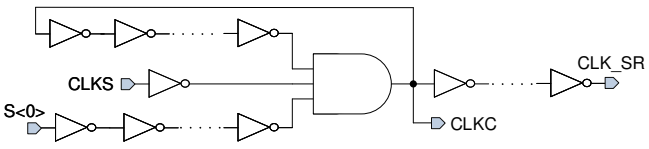

Fig. 7. Synchronous clock

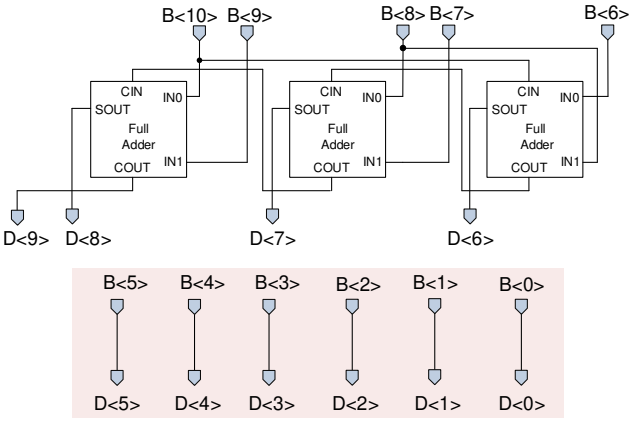

Fig. 8. Digital error correction

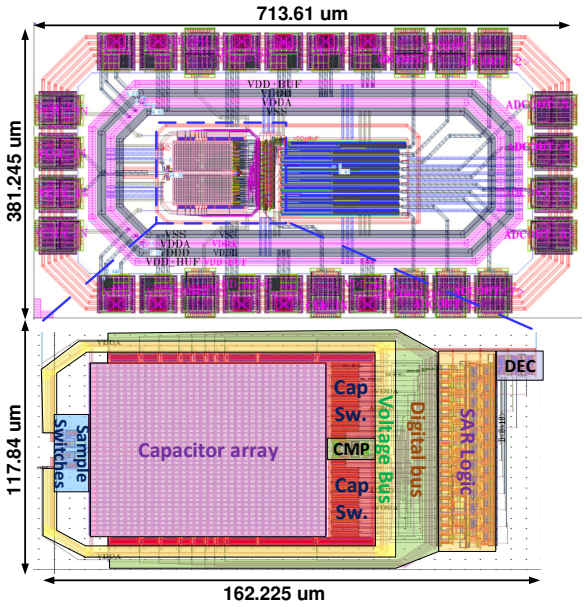

Fig. 9. Layout and floor plan

The duty cycle, frequency, and other characteristics of these control signals can be finely tuned by adjusting the number of inverters and the size of their internal transistors. Specifically, CLK_SR is derived from CLKC after a carefully designed delay time. The delay time has been adjusted to ensure that the overall control circuit will not cause errors during any operation.

D. Digital Error Correction (DEC)

Since the capacitor array of this circuit adopts the sub-radix-2 algorithm, it means that the capacitance ratio of this array is not arranged in a binary order. Therefore, the result of each comparison must be corrected by a circuit to obtain the correct output result. Fig. 8 depicts the DEC circuit used for correction. It mainly uses three comparators to re-calculate the output of each bit according to its corresponding capacitance size, and re-calculate the correct 10-bit digital output.

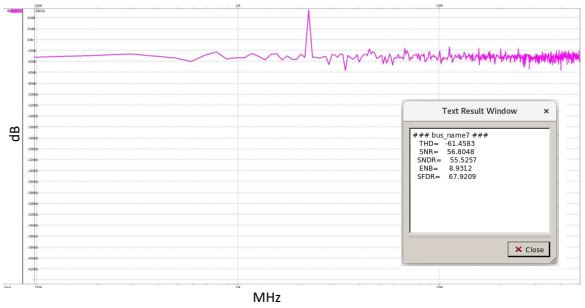

Fig. 10. TT with DC input

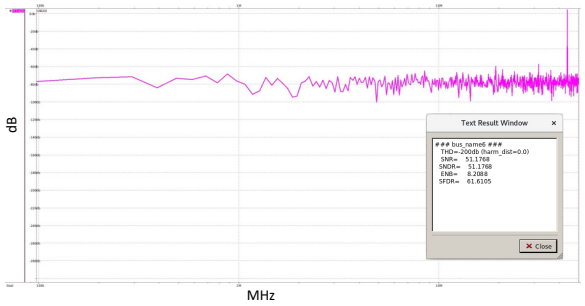

Fig. 11. TT with Nyquist input

III. Post-Layout Simulations

The proposed ADC is implemented using the TSMC 40 nm CMOS process. The layout design and floor plan are shown in Fig. 9, respectively. A Fast Fourier Transform (FFT) is performed on the digital output of the proposed design when an input sine wave with a DC frequency of approximately 2.25 MHz and another signal close to the Nyquist frequency (43.85 MHz) is applied. The corresponding frequency spectra are shown in Fig. 10 and Fig. 11, respectively. For a DC frequency input in the TT corner (25 °C, 1 V), the ADC achieves: $SFDR_{DC}$ = 67.9209 dB, $SNDR_{DC}$ = 55.5257 dB, and ENOB = 8.9312. Similarly, when the input is close to the Nyquist frequency, the ADC achieves: $SFDR_{NYQ}$ = 61.6105 dB, $SNDR_{NYQ}$ = 51.1768 dB and ENOB = 8.2088.

Further simulations at 2.25 MHz frequency across all PVT (process, voltage, and temperature) corners are summarized in Table II. The $SFDR_{DC}$ varies from 63.0192 dB (FS corner) to 67.9209 dB (TT corner), indicating effective suppression of spurious signals. The $SNDR_{DC}$ ranges from 51.3377 dB (FF corner) to 55.8824 dB (SS corner), demonstrating robust noise and distortion performance. Despite variations in process, voltage, and temperature, the ADC exhibits stable performance across all PVT corners, with the ENOB consistently exceeding 8 bits, ensuring high-resolution and reliable data conversion. A comparative performance analysis with previous ADC designs is provided in Table III. Notably, none of any prior ADC was designed particularly for PNNs O-E interface.

TABLE II
Post-Layout Simulation Performance in 5 PVT Corners

Parameter	FF	FS	SF	SS	TT
Supply Voltage (V)	1.1	1	1	0.9	1
Temperature (°C)	–40	25	25	85	25
$SFDR_{DC}$ (dB)	65.6324	63.0192	65.086	67.7442	67.9209
$SNDR_{DC}$ (dB)	51.3377	54.1697	52.979	55.8824	55.5257
ENB	8.2355	8.7089	8.5082	8.6582	8.9312

TABLE III
Performance Comparison

Parameter	[2]	[6]	[7]	Our work
Technology	90 nm	40 nm	180 nm	40 nm
Structure	Pipeline	SAR	SAR	SAR
Resolution	12 bits	10 bits	10 bits	10 bits
Sampling Rate (MS/s)	40	100	0.005	100
Supply Voltage (V)	1.2	1.1/1.3	1.8	1
$SFDR_{DC}$(dB)	NA	NA	73.19	67.9209
$SNDR_{DC}$ (dB)	71.22	57.9	61.36	55.5257
Power (mW)	47.3	1.4	1.43	0.896
FoM (fJ/step)	397.61	21.8	143.08	18.36

FOM = Power / (2^{ENOB} x Sample Rate)

IV. Conclusion

This paper presents a 10-bit, 100 MS/s V_{CM}-based Switching ADC designed using the TSMC 40 nm process. The ADC achieves high dynamic performance, power efficiency, and signal integrity, making it suitable for energy-sensitive applications. The custom unit capacitor used in the Capacitor array of the CDAC minimizes parasitics and enhances precision, enabling efficient signal sampling. This design is particularly beneficial for photonic neural networks (PNNs), ensuring accurate and seamless O-E to digital signal conversion for high-speed computing and signal processing.

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