A Dual-Loop Clock and Data Recovery System with HLD for Extended Lock-in Range Demand

L S S Pavan Kumar Chodisetti, Wei-Cheng Cheng, Tzung-Je Lee and Chua-Chin Wang
Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan 80424
Email: ccwang@ee.nsysu.edu.tw

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***Abstract*—This paper presents a dual-loop Clock and Data Recovery (CDR) circuit designed to retrieve digital data over a range of 0.5 to 5 Gbps. The proposed method for frequency acquisition is founded on a full-rate clock architecture. To enhance the lock-in range, the design incorporates a Hysteresis Lock Detector (HLD), a Frequency Rise/Fall Control circuit, and a Modified Digital Quadri-correlator Frequency Detector (DQFD). The architecture employs two control lines for Coarse and Fine Tuning of the Voltage-Controlled Oscillator (VCO), facilitating distinct loop filters in each of the dual loops, thereby effectively reducing jitter and noise. The circuit has been fabricated using advanced 40-nm CMOS technology, and post-layout simulation outcomes at 5 Gbps demonstrate performance metrics, including a peak-to-peak jitter of 12.7 ps and an RMS jitter of 2.23 ps for the recovered clock signal.**

***Index Terms*—Jitter, DQFD, Hysteresis Lock Detector, Lock-in range**

I. Introduction

In a communication system, the receiver must extract the clock signal from the incoming data stream. This process is significantly aided by the Clock and Data Recovery (CDR) circuit [1], [2]. A large lock-in range is necessary for CDR circuits to support different data rate needs. Additionally, minimizing jitter is essential for maintaining high-quality signal transmission. Because of its simple construction, the dual-loop control technique is frequently used in CDR circuits [1]–[3].

However, once the system reaches lock, interference and undesired fluctuations in the control signal may occur when the two control signals from the dual-loop system are combined into a single input for the Voltage-Controlled Oscillator (VCO) via a shared loop filter. This interference leads to increased jitter and longer lock-in times [1]–[3]. Dual-loop CDR systems can benefit from the Digital Quadri-correlator Frequency Detector (DQFD), which stops control pulses from being generated while the system is locked [3]. However, when a substantial frequency offset is present, its operational stability may be affected, thereby limiting the lock-in range [4].

This study proposes the integration of the Hysteresis Lock Detector (HLD), a Frequency Rise/Fall Control circuit, and a Modified DQFD to expand the lock-in range. Additionally, a Coarse and Fine Tuning VCO is introduced to mitigate interference between the dual loops and reduce jitter. Simulation results indicate a lock-in range from 0.5 to 5.5 Gbps, with a peak-to-peak jitter of 12.7 ps and a root-mean-square jitter of 2.23 ps.

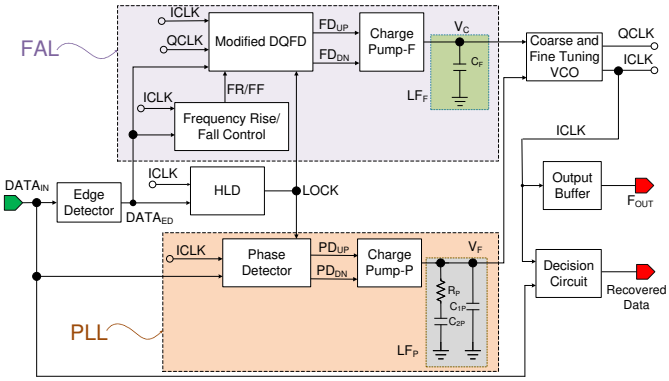

Fig. 1. The proposed dual-loop CDR system

II. Proposed Architecture

Fig. 1 presents the proposed CDR architecture, which comprises multiple functional blocks. These include a Phase Detector [5], 2 Charge Pumps (Charge Pump-F, P), a Modified DQFD, a Coarse and Fine Tuning VCO, LF_F and LF_P as off-chip Loop Filters, an Edge Detector, an Output Buffer, a Decision Circuit, a Frequency Rise/Fall Control circuit, and a HLD.

The proposed system integrates a Frequency Acquisition Loop (FAL) and a Phase-Lock Loop (PLL). The VCO generates two signals of digital quadrature signals, ICLK and QCLK. In instances when a significant initial frequency discrepancy exists between the $DATA_{IN}$ (input) and ICLK, the HLD outputs a logic 0 for the LOCK signal. This disables the PLL and activates the FAL. At this stage, the Frequency Rise/Fall Control Circuit detects the frequency difference between $DATA_{IN}$ and ICLK and subsequently generates the FR/FF signal to modify the VCO frequency accordingly. The direct comparison between $DATA_{IN}$ and ICLK results in two control signals, FD_{UP} and FD_{DN}.

Once the VCO frequency approaches that of $DATA_{IN}$, the LOCK switches to 1, enabling the CDR to function with both the Phase Detector and the Modified DQFD. Under this condition, the Charge Pump-F and DQFD generate V_C

Chua-Chin Wang is also with Institute of Integrated Circuit Design, and Institute of Undersea Teachnology, National Sun Yat-sen University, Kaohsiung, Taiwan 80424.

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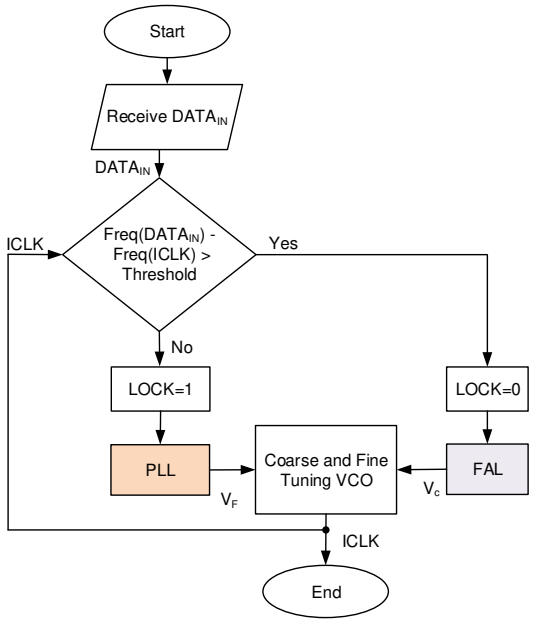

Fig. 2. Flowchart of the proposed dual-loop CDR

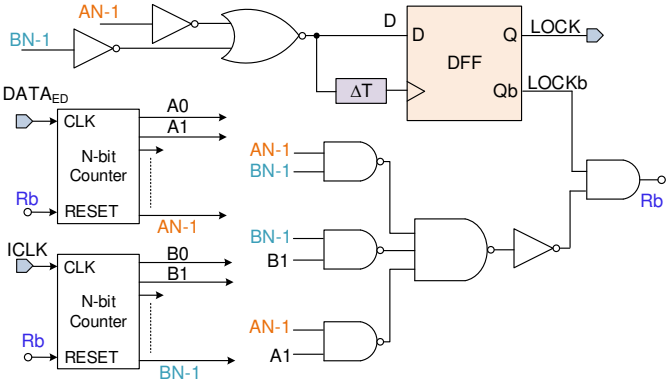

Fig. 3. Schematic of the HLD

(coarse control signal) for the VCO, while V_F (fine control signal) is derived from the Charge Pump-P and Phase Detector. The VCO independently gets both V_C and V_F to ensure precise frequency and phase alignment for ICLK (in-phase) and QCLK (quadrature). Lastly, the output buffer, which is powered by ICLK, can manage loads with high capacitance up to 20 pF. Fig. 2 provides an overview of these operations.

A. HLD

In a dual-loop CDR circuit, the lock detector serves a vital function, primarily for switching between the PLL and the FAL. Fig. 3 illustrates the HLD, as presented in Fig. 1. The counter is responsible for monitoring the cycle count of both $DATA_{ED}$ and ICLK. When one counter hits the threshold of 2^{N-1}+2 while the other remains below 2^{N-1}, it indicates that the VCO frequency remains beyond the acceptable error range. This triggers R_b (reset signal), which resets the counters and generates a signal to activate the DFF, resulting in a logic 0

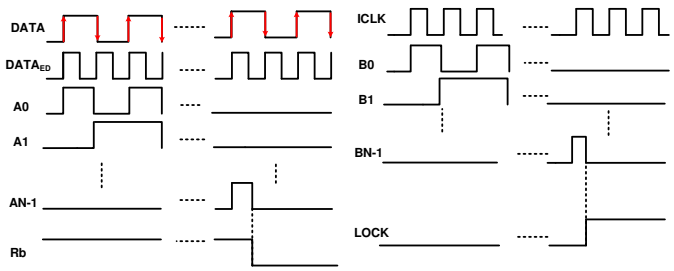

Fig. 4. Timing diagrams of HLD, when both $DATA_{ED}$ and ICLK have a close frequency

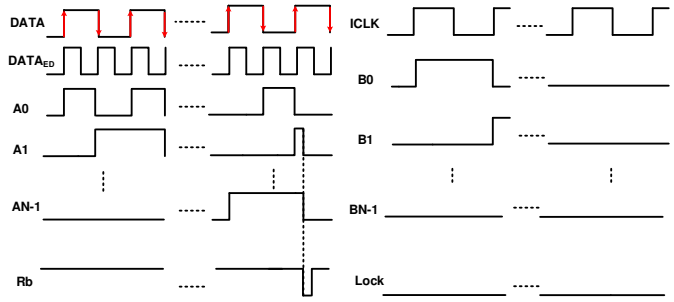

Fig. 5. Timing diagrams of HLD, when both $DATA_{ED}$ and ICLK have a huge frequency difference

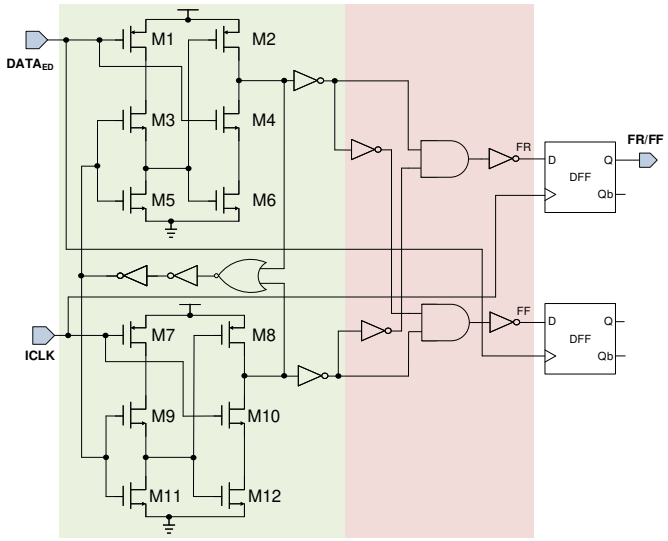

Fig. 6. Frequency Rise/Fall Control circuit

LOCK signal. This process continues until the other counter reaches a value of at least 2^{N-1}. Once this condition is met, the NOR gate outputs signal D for the DFF. The LOCK signal will be pulled high, while the LOCKb signal drops to zero, terminating the process.

Fig. 4 shows the timing diagrams of the HLD when $DATA_{ED}$ and ICLK have similar frequencies. In contrast, Fig. 5 presents the timing diagrams when $DATA_{ED}$ and ICLK exhibit a significant frequency difference.

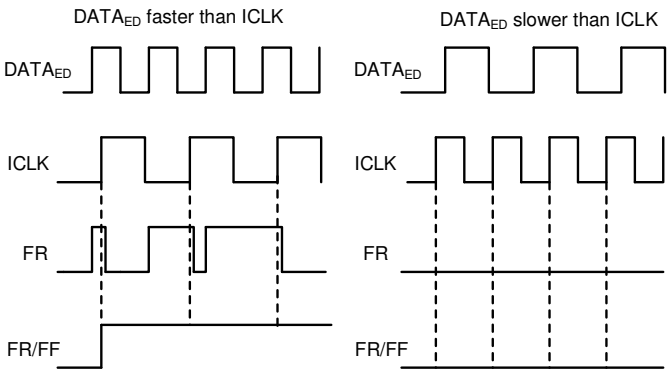

Fig. 7. Illustrative waveforms of Frequency Rise/Fall Control circuit

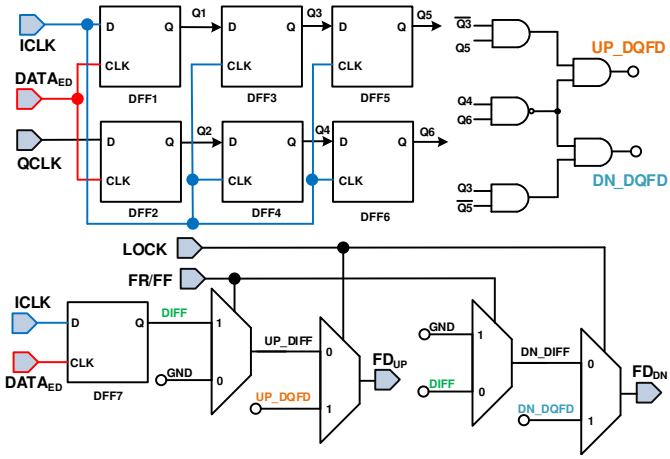

Fig. 8. Circuit logic of the Modified DQFD [7]

B. Frequency Rise/Fall Control circuit

Fig. 6 depicts the Frequency Rise/Fall Control circuit in Fig. 1. The circuit inside the green box is frequency comparator [6] and the circuit inside the red box is used for surge elimination. Based on the frequency difference between $\mathrm{DATA_{ED}}$ and ICLK, this circuit produces a logic high on FR/FF to increase the output frequency of VCO or a logic low on FR/FF to decrease the output frequency of VCO. Fig. 7 shows the timing diagram of this circuit.

C. Modified DQFD

Fig. 8 depicts schematic of the Modified DQFD in Fig. 1. QCLK, and ICLK will be compared with the $\mathrm{DATA_{ED}}$. This comparison makes it possible to identify the four operational states of the DQFD: state A, B, C, and D. The ICLK and QCLK values, which are 00, 01, 11, and 10, respectively, correlate to these states. Variations in the input $\mathrm{DATA_{ED}}$ and VCO frequencies ICLK and QCLK will cause corresponding changes in the states. It will generate the two control signals UP_DQFD and DN_DQFD using the Shift Register's output values, Q3, Q4, Q5, and Q6, as well as their complements. For ICLK (QCLK) and $\mathrm{DATA_{ED}}$, the high frequency difference is indicated when LOCK is logic 0. In this case, the control signal is selected straight from the DIFF. UP_DQFD and DN_DQFD can be applied to the output control signals $\mathrm{FD_{UP}}$ and $\mathrm{FD_{DOWN}}$, respectively, whenever the LOCK is logic 1, indicates frequency difference is low.

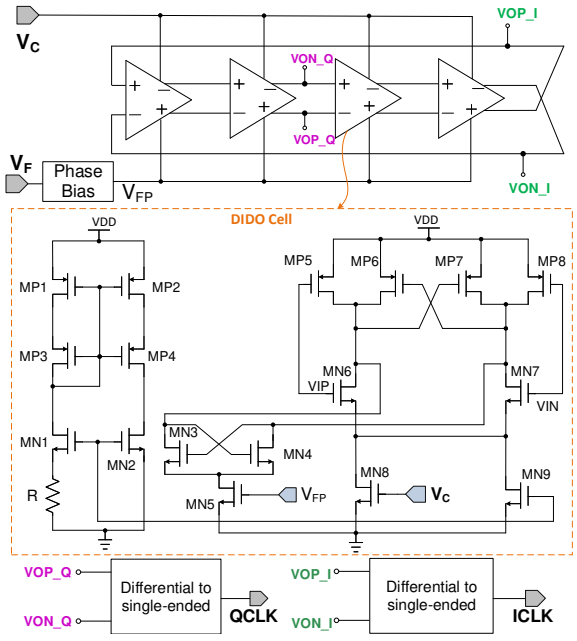

Fig. 9. Schmetic of the VCO

D. Coarse-Fine Tuning VCO

Fig. 9 illustrates the schematic of Coarse-Fine Tuning VCO in Fig. 1. This VCO consists of four Differential Input Differential Output (DIDO) delay cell blocks [8]. To produce ICLK and QCLK, two Differential to Single-ended circuits are utilized. This VCO features two distinct frequency modulation techniques. A broad frequency modulation range is made possible by the coarse-tuning process, where the oscillation frequency is managed by varying the MN8 gate voltage, which is influenced by the output of the FAL. In contrast, the fine-tuning mechanism offers a narrower modulation range and is adjusted via the PLL, where the gate voltage of MN5 regulates the oscillation frequency. MN9 drives the DIDO delay cell, supplying the required tail current to sustain the intended free-running frequency. Furthermore, Providing the finely tuned voltage $\mathrm{V_{FP}}$ is the responsibility of the Phase Bias circuit, which is inversely related to $\mathrm{V_F}$. A differential to single-ended converter circuit is required at the output of this oscillator because its output voltage does not reach full swing. This will transform the oscillator's output voltage into a full-range digital signal suitable for use by other digital circuits.

III. Implementation and Simulations

The proposed CDR system has been realized utilizing a 40-nm CMOS node. The layout of the chip is illustrated in Fig. 10. With a 20 pF load capacitance, the circuit operates at 5 Gb/s while consuming 64.03 mW of power from a 0.9

TABLE I
PERFORMANCE COMPARISON

Parameter	[2]	[9]	[10]	Our work
Year	2020	2021	2023	2024
Technology (nm)	180	180	40	40
VDD (V)	1.8	1.8	1.2	0.9
Data Rate Range (Gb/s)	0.42∼3.45	0.32∼2.7	7∼10.5	0.5∼5
Lock-in Range (Gb/s)	3.03	2.38	3.5	**4.5**
P2P Jitter (ps)	19.4 @3.45 Gb/s	59 @2.7 Gb/s	33.1 @1.31 Gb/s	12.7 @5 Gb/s
RMS Jitter (ps)	2.25 @3.45 Gb/s	NA	4.75 @1.31 Gb/s	2.23 @5 Gb/s
Core area (mm^2)	0.442	NA	0.102	0.018
Power (mW)	20.3 @3.45 Gb/s	62 @2.7 Gb/s	39.6 @10.5 Gb/s	64.03 @5 Gb/s
FOM[1]	0.307	0.060	0.925	**1.968**

[1] $\text{FOM} = \left(\frac{\text{Lock}-\text{inRange}}{\text{VDD}*\frac{\text{P2PJitter}}{\text{Max.Gb/s}}}\right)$

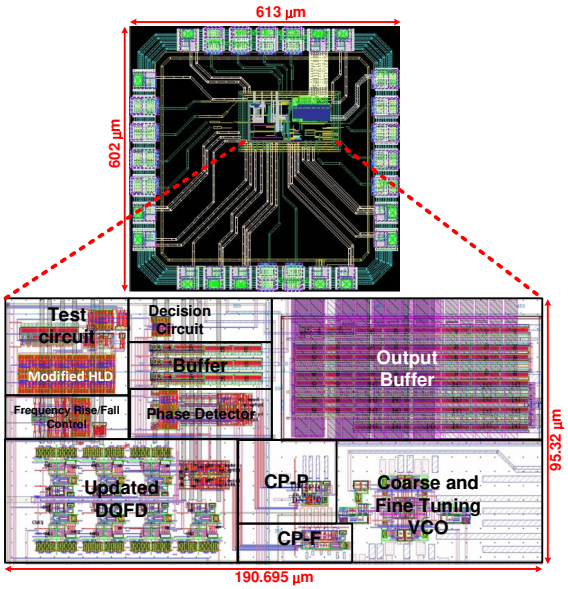

Fig. 10. Layout of the proposed CDR

V supply. Notably, the Output Buffer accounts for 49.108 mW, making up 76.69% of the total power consumption. Simulation results for a 5 Gb/s data input are presented in Fig. 11, showing that the frequency acquisition loop locks the frequency within 10 ns using the Modified DQFD, with the LOCK signal transitioning to logic high to activate the phase-locked loop. The eye diagram of the recovered clock at 5 Gb/s is shown in Fig. 12, where the peak-to-peak jitter and RMS jitter are measured at 12.7 ps and 2.23 ps, respectively. A performance comparison between this work and previous CDR designs is summarized in Table I.

IV. CONCLUSION

This work presents the design and development of a reference-less dual-loop CDR circuit utilizing a 40-nm CMOS node that operates between 0.5 and 5 Gbps. The proposed

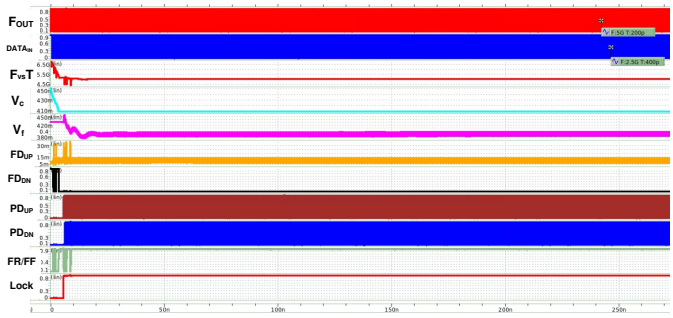

Fig. 11. Simulation results for 5 Gb/s data input

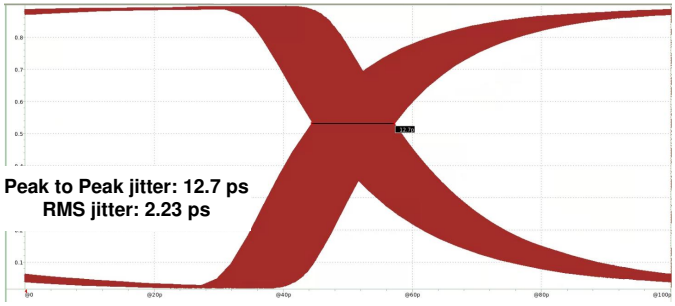

Fig. 12. Eye diagram of the restored clock for 5 Gb/s data input

architecture incorporates a Hysteresis Lock Detector (HLD), a Frequency Rise/Fall Control circuit, and a Modified DQFD. Results from post-layout simulations show that the design maintains a low RMS jitter of 2.23 ps for the recovered clock signal while achieving a wide capture range.

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