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12-bit 100 MS/s Time-Relaxed Interleaved Randomly Selected DAC for Real-time FOG Systems

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***Abstract*—This article presents a 12-bit time-relaxed interleaved randomly selected Digital-to-Analog Converter (DAC) implemented using the TSMC TN40G process technology. The DAC operates at a clock frequency of 100 MHz with a core circuit area of 248 $\times$ 203 μm^2 and a supply voltage of 0.9 V. The design features two sets of stacked current source arrays, arranged in a staggered manner to optimize switching performance. Simulation results demonstrate that the proposed DAC achieves an SFDR of 61.2 dB at DC (Fin = 9 MHz) and 71.9 dB near Nyquist (Fin = 49 MHz, 0.5 Fs), with a total power consumption of 26.9 mW. The proposed DAC design highlights dynamic performance, power efficiency, and mismatch error reduction, making it a promising solution for fiber optic gyroscope (FOG) systems.**

***Index Terms*—DAC, SFDR, FOG, Switch Driver, Interleaved random selection**

I. Introduction

In recent advancements in fiber optic gyroscope (FOG) systems, these devices have been fully solid-state fabricated. Compared to ring laser gyroscopes (RLGs), FOGs offer advantages such as lower cost, smaller size, longer operational lifespan, and higher production yield due to simpler manufacturing processes [1]–[3]. FOG systems operate by splitting a laser beam into two paths traveling in opposite directions (clockwise and counterclockwise) within a fiber loop. The Sagnac effect causes a slight difference in the path length for the beam traveling against the rotation, resulting in a phase shift proportional to the rotation angle. Unlike traditional spinning-mass or mechanical gyroscopes, FOGs lack moving parts, minimizing noise and interference between successive measurements. This characteristic ensures high correlation between consecutive samples. The phase shift caused by the Sagnac effect is processed as shown in Fig. 1.

The baseband integrated circuit is central to FOG operation. The SAR-ADC digitizes the amplified signal from the photodetector and sends it to the "Logic Core" for computational processing. The Logic Core also manages adaptive resets when needed. The input voltage signal from the photodetector, resembles an impulse train.

While significant focus has been placed on designing high-speed ADCs for real-time optoelectronic applications [4], [5], the digital-to-analog converter (DAC) in Fig. 1 remains a critical but often overlooked component. The DAC ensures accurate phase feedback for modulators, necessitating high speed and precision. Integration with other FOG components also requires the DAC to support differential signal processing and manage voltage level conversions for amplification and output translation, as shown in Fig. 2. Despite numerous DAC designs reported in the literature [6]–[8], none have been tailored specifically for FOG systems or similar real-time applications.

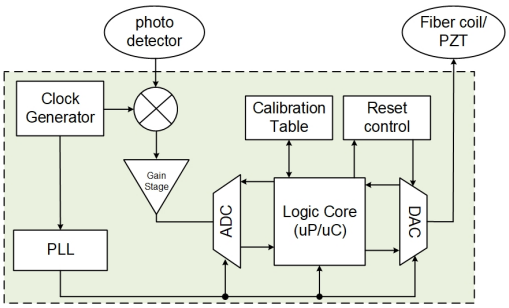

Fig. 1. FOG baseband system

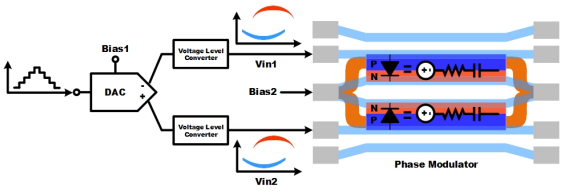

Fig. 2. Integration of DAC in the FOG system

II. Proposed 12-bit 100 MS/s Time-Relaxed Interleaved Randomly Selected Current DAC

In this study, we present an interleaved randomly selected current DAC architecture, as illustrated in Fig. 3. The proposed architecture comprises two sets of Cascode Current Steering Arrays, a Switch Driver, a Swapper, and control mechanisms for return-to-zero (RZ) and non return-to-zero (NRZ) operations.

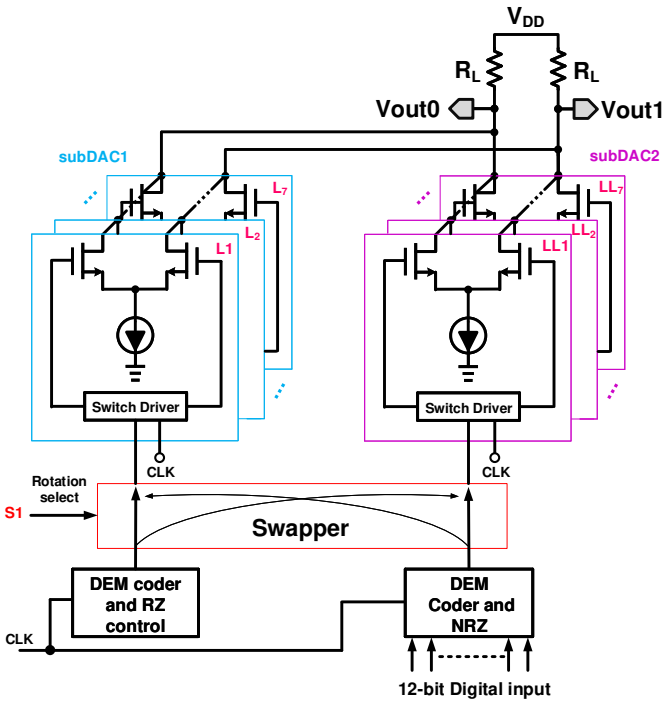

Fig. 3. Interleaved random current DAC system architecture

The fundamental principle of this design involves two stacked current source arrays that form two sub-DACs. These sub-DACs operate concurrently, executing both digital input encoding and digital zeroing control. By dynamically switching between encoding and zeroing operations through a controlled switching mechanism, the proposed approach effectively reduces signal dependence. Furthermore, this control methodology significantly minimizes settling time, defined as the duration required for the output signal to reach a stable state, thereby improving overall dynamic performance. A comparative analysis between the proposed technique and conventional methods is provided in the following discussion.

Fig. 4 illustrates the conventional interleaved random selection control method, which employs Digital Random Return to Zero (DRRZ) along with a DRRZ signal delayed by half a frame period in parallel. By superimposing the two resulting waveforms, it is evident that the benefits of the RZ technique can be achieved without the need for a visible RZ signal at the output of the interleaved random selection method. Similarly, the advantages of the zeroing technique can be realized without directly observing the zeroed signal at the output.

Fig. 5 presents the Time-Relaxed Interleaving DRRZ (TRI-DRRZ) technique, which employs two identical sub-DACs: one dedicated to digital input code processing and the other to zeroing operations. Both sub-DACs initiate operation simultaneously upon the detection of a pulse edge trigger. Compared to the conventional approach, which requires two reset operations within a single clock cycle, the proposed method performs only one reset operation per clock cycle.

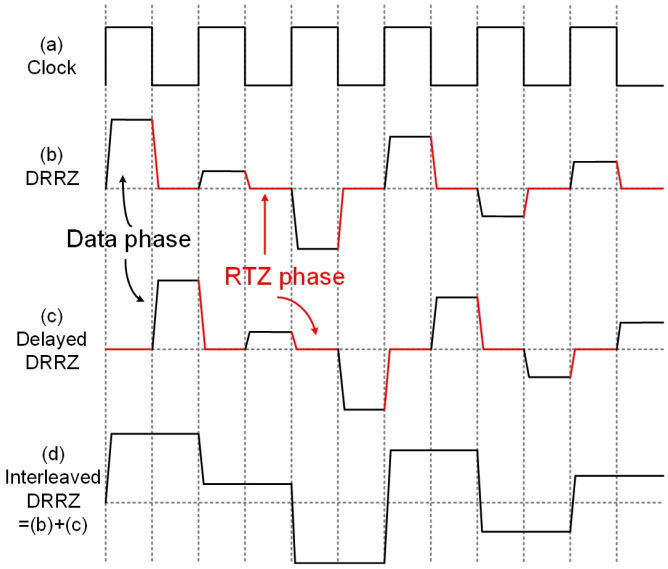

Fig. 4. Timing waveform of traditional interleaved random selection control method

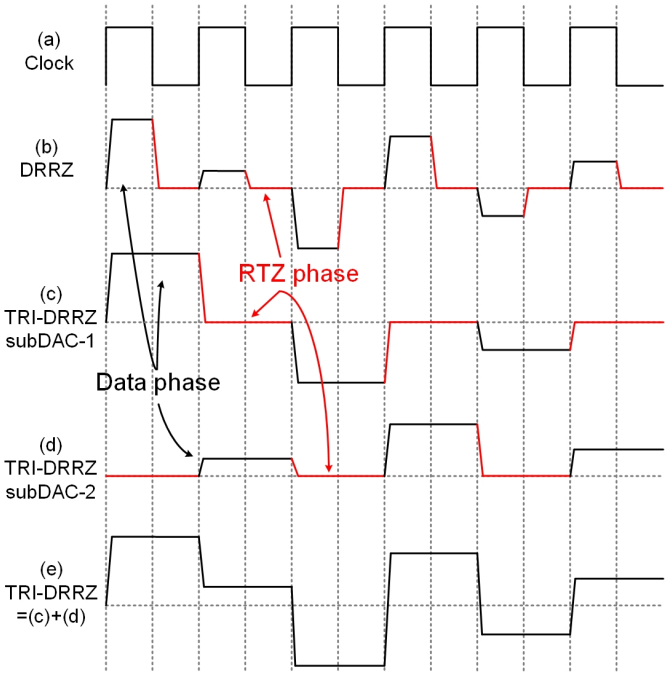

Fig. 5. Time-Relaxed Interleaving DRRZ technique in the proposed DAC

This reduction in reset operations leads to a shorter stabilization time, thereby facilitating higher operational speeds and improved overall performance.

A. Switch driver

Fig. 6 presents the schematic of the Switch driver, designed to ensure that the signal interchange point is positioned above VDD/2. This design effectively mitigates voltage drops that may occur during switching operations. To enhance switching speed and reduce the impact of clock feedthrough, the

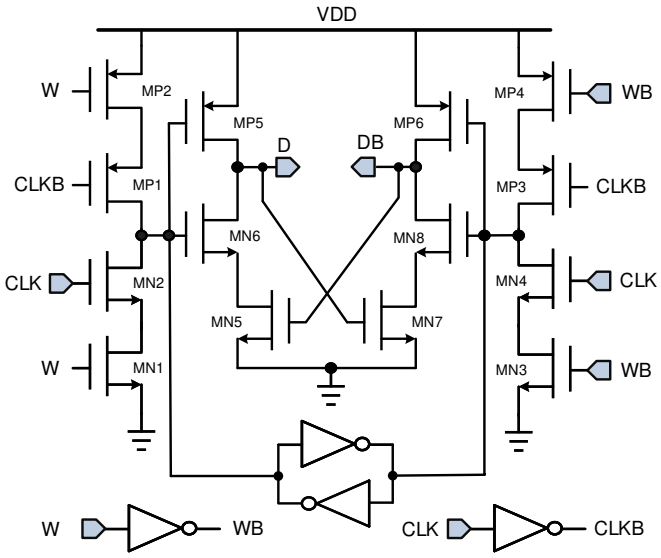

Fig. 6. Switch driver

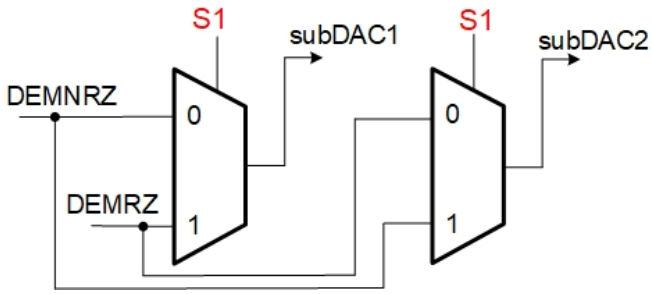

Fig. 7. Swapper

proposed Switch driver employs a CMOS-based architecture (MN1–MN4, MP1–MP4) instead of a conventional pass-transistor latch. This CMOS implementation improves circuit performance by minimizing propagation delay and enhancing signal integrity.

Furthermore, the inverted signals WB and CLKB are locally generated within each Switch driver, ensuring optimal layout considerations to reduce parasitic effects. The outputs, D and DB, serve as differential control signals for the current steering switches, ensuring precise and reliable switching operation.

B. Swapper

The Swapper circuit, illustrated in Fig. 3, is composed of two two-to-one multiplexers, as depicted in Fig. 7. Its primary function is to interchange the NRZ control signal and the RZ control signal, directing them to the Switch driver circuit of the two sub-DACs. This configuration ensures that one sub-DAC operates in NRZ mode, while the other operates in RZ mode, thereby optimizing signal integrity and reducing distortion.

The control switching signal for the Swapper circuit is a random number (S1), generated by the pseudo-random number generator (PRNG) within the dynamic element coder (DEM). This randomization enhances the dynamic performance of the

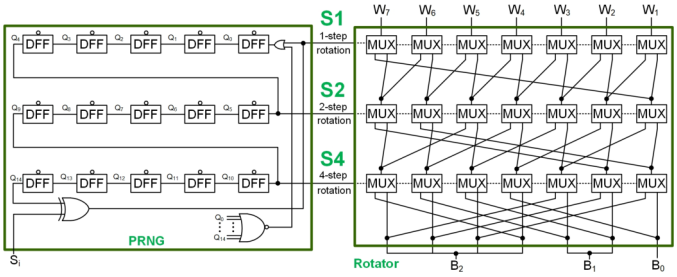

Fig. 8. DEM coder

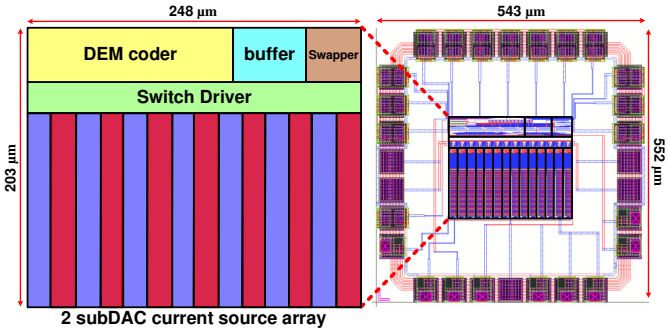

Fig. 9. Layout and floor plan

system by mitigating mismatch errors and improving overall conversion accuracy.

C. DEM coder and control

A major challenge in conventional current-steering DACs is the current source mismatch, which degrades SFDR due to fabrication-induced variations. To address this, the proposed design integrates a DEM coder with a PRNG and Rotator, utilizing random rotation-based binary weighted selection technique to minimize mismatch errors and enhance SFDR. The schematic of DEM coder is shown in Fig. 8, where S_i is sourced from 1-bit RNG circuit, which is from our previous work [9]. By dynamically varying the selection of current sources in each conversion cycle, mismatch-induced errors are equalized, improving linearity and overall performance. This approach effectively reduces systematic mismatches, making it a robust solution for high-precision DACs.

III. Post-Layout Simulations

The proposed 12-bit Interleaved randomly selected DAC is realized using the TSMC TN40G process, operating at a clock frequency (F_s) of 100 MHz. The area of the core circuit is 248 $\times$ 203 μm^2. The layout and floor plan are shown in Fig. 9. The supply voltages used for VDD is 0.9 V. Two sets of stacked current source arrays are arranged in a staggered manner and are distinguished by purple and red in the Fig. 9. The simulation results of DEM coder are shown in Fig. 10. For dynamic performance, the SFDR spectrum is analyzed for F_{in} = 9 MHz (DC) and F_{in} = 49 MHz (almost 0.5 F_s) are depicted in Fig. 11 and Fig. 12, respectively. The SFDR at DC ($SFDR_{DC}$) is 61.2 dB, and the SFDR near Nyquist

TABLE I
PERFORMANCE COMPARISON

Parameter	[10]	[11]	[12]	Our work
Technology	180 nm	180 nm	180 nm	40 nm
Resolution	10 bits	10 bits	14 bits	12 bits
Sampling Rate (MS/s)	400	500	3000	100
Supply Voltage (V)	1.8	1.8	1.8	0.9
SFDR_{DC} (dB)	58	68.7	60	61.2
SFDR_{NYQ} (dB)	49	56	52	71.9
Power (mW)	20.7	42	600	26.9

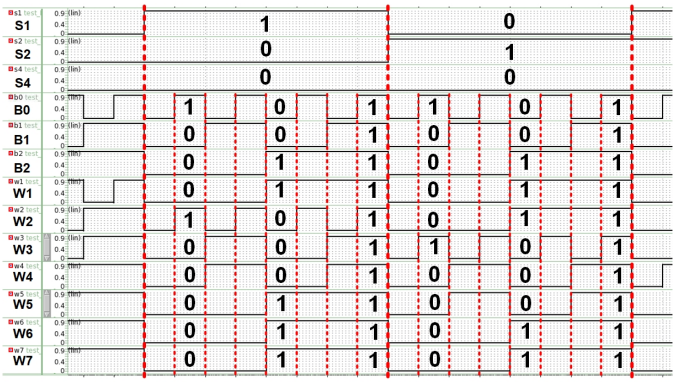

Fig. 10. Simulation results of DEM coder

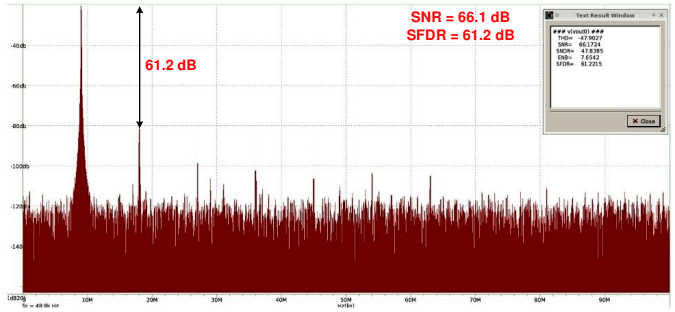

Fig. 11. The SFDR spectrum at DC input

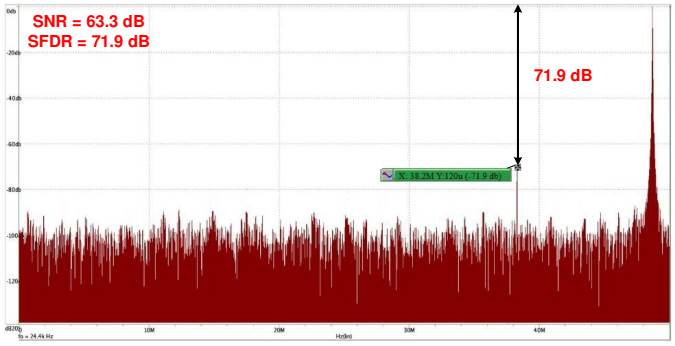

Fig. 12. The SFDR spectrum at near Nyquist input

(SFDR_{NYQ}) is 71.9 dB, and the consumed power is 26.9 mW. A summary of the performance comparison between our work and earlier DAC studies is illustrated in Table I.

IV. Conclusion

In this work, a 12-bit time-relaxed interleaved randomly selected DAC with two sets of stacked current source arrays was successfully designed and simulated using the TSMC TN40G process. The integration of a PRNG and a rotator in the DEM Coder effectively improves dynamic performance by introducing a randomized current source selection, reducing systematic mismatch errors. The simulation results confirm that the proposed design achieves an SFDR of 61.2 dB at DC and 71.9 dB near Nyquist, with a power consumption of 26.9 mW, demonstrating its suitability for FOG systems.

V. Acknowledgement

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