A 12-bit Current-Steering DAC with Output Impedance Compensation for PNN Prototyping

Pradyumna Vellanki*, Jun-Yu Chang*, Friedel Gerfers†, Yung-Jr Hung‡, Chewn-Pu Jou§, and Chua-Chin Wang*
*Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan 80424
†Technische Universität Berlin, Berlin, Germany 10623
‡Department of Photonics, National Sun Yat-sen University, Kaohsiung, Taiwan 80424
§Taiwan Semiconductor Manufacturing Company, Hsinchu Science Park, Hsinchu, Taiwan 30075
Email: ccwang@ee.nsysu.edu.tw

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***Abstract*—This article presents the design and implementation of a highly linear and output impedance compensated digital-to-analog converter (DAC). The proposed architecture minimizes layout area while maintaining high linearity and optimized output impedance. The DAC comprises several key functional blocks, including a Stacked current steering array, a Dynamic Element Matching Coder (DEM), a Splitting Decoder, a Dynamic Element Matching and Full Differential Current Return-to-Zero Logic Controller (DEMRTZ Control), a Switch Driver Array, a Bias Circuit, and an Output Impedance Compensation (OIC) module. Each component plays a crucial role in improving the overall performance of the DAC in terms of linearity and impedance characteristics. The proposed DAC is designed using TSMC TN40G process technology with a core circuit area of 242.555 $\times$ 166.2 μm^2. Post-layout simulations show that at an input frequency of 0.56 MHz, the DAC achieves an ENOB of 11.68 bits and an SFDR of 84.17 dB. At 48.65 MHz, the DAC maintains an ENOB of 10.78 bits and an SFDR of 76.77 dB.**

***Index Terms*—PNN, MZM, DAC, DEMRTZ, SFDR, OIC**

I. Introduction

Photonic neural networks (PNNs) have emerged as a promising solution for next-generation AI systems [1]. However, the realization of PNNs requires sophisticated analog-to-digital (ADC) and digital-to-analog conversion (DAC) technologies that can interface effectively with both the digital and photonic components of the system. A key component of PNN is the Mach-Zehnder Modulator (MZM), which converts electrical signals into optical signals and enables critical operations like matrix-vector multiplications. The performance of MZMs heavily relies on their driving electronics, particularly digital-to-analog converters (DACs) [2]. The Current-Steering DAC (CS-DAC) architecture is well-suited for this task due to its speed and scalability [3]–[6]. However, challenges arise in adapting it to meet the interface demands of MZMs used in PNNs. The basic requirements of MZMs are tabulated in Table. I. A PNN prototype realized by our team is demonstrated in Fig. 1. This research is focused on designing a wide-range CS-DAC with reasonable speed trade-offs and high current cell impedance to minimize the effect of the finite impedance of conventional CS-DACs. This work presents an advanced CS-DAC architecture that incorporates output impedance compensation and dynamic element matching techniques to enhance performance and minimize layout area.

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TABLE I
MZM BASIC REQUIREMENTS

Parameters	Value
V_{in} (V)	0.03 to 3
Speed (Hz)	100 M to 1 G
Impedance (Ω)	50

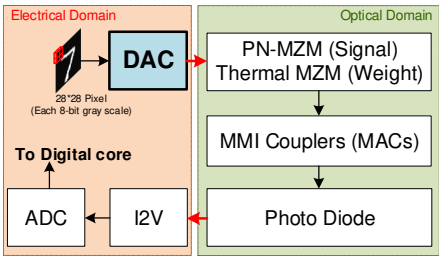

Fig. 1. The prototype of the PNN system

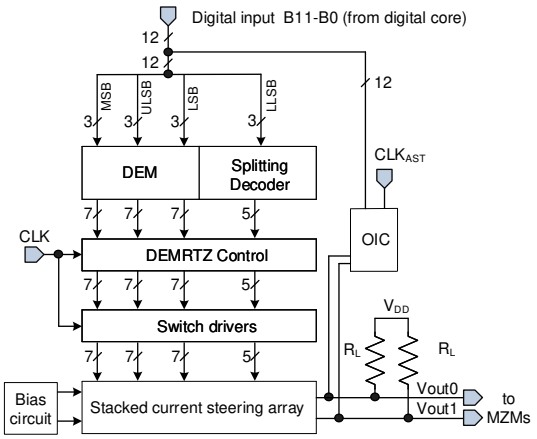

Fig. 2. Block diagram of 12-bit CS-DAC with output impedance compensation

II. Proposed 12-bit CS-DAC with Output Impedance Compensation

The proposed DAC architecture consists of multiple functional blocks that collectively improve linearity and output

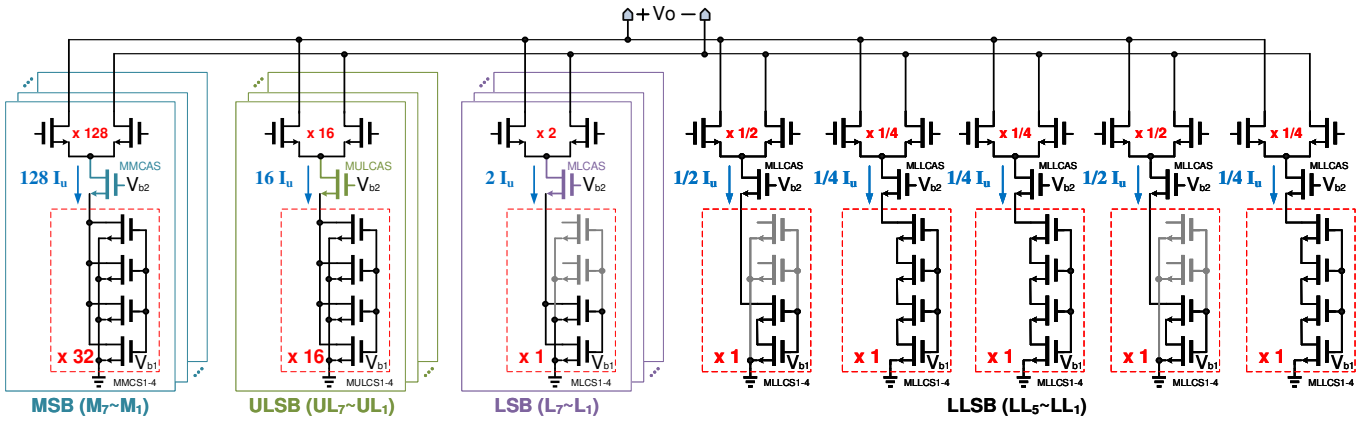

Fig. 3. Schematic of Stacked current steering array

impedance stability as shown in Fig. 2: a Stacked current steering array, Bias Circuit, a Dynamic Element Matching Coder (DEM), a Dynamic Element Matching and Full Differential Current Return-to-Zero Logic Controller (DEMRTZ Control), Switch drivers array, and an Output Impedance Compensation (OIC) circuit.

The digital input B11-B0 is segmented into three unary MSB bits, three unary ULSB bits, three unary LSB bits, and three binary LLSB bits. The operating principle involves processing the upper 9 bits and the lower 3 bits separately through the DEM Coder and the Splitting Decoder, respectively. The DEM Coder encodes the input signal to generate a control signal, while the Splitting Decoder decodes the input signal to produce a split code, which is then sent to the DEMRTZ Control circuit. The DEM Coder is sourced from our previous work [7]. Based on the DEMRTZ output, the Switch driver circuit manipulates the switch pairs of the current source to generate a return-to-zero (RTZ) differential DAC output, given by VDAC = Vout1 – Vout0 = 0. Additionally, an OIC circuit is incorporated between Vout1 and Vout0 to compensate for the Spurious-Free Dynamic Range (SFDR) attenuation caused by limited output impedance.

A. Current sources schematic of the Stacked current steering array

Fig. 3 illustrates the Current sources schematic of the Stacked current steering array, where Cascode transistors MMCAS, MULCAS, MLCAS, and MLLCAS mitigate output impedance limitations by operating in the saturation region. Each current source MMCS1 – MMCS4, MULCS1 – MULCS4, MLCS1 – MLCS4, and MLLCS1 – MLLCS4 is divided into four transistors to minimize mismatches from etching variations and enhance performance.

Differences in transistor count within current source switch pairs lead to parasitic capacitance variations. A Compensation capacitor is introduced between the switch driver circuit and the current source switch pair to reduce timing skew, ensuring uniform signal timing and improved DAC performance. Fig. 4 shows the compensation capacitor positioning.

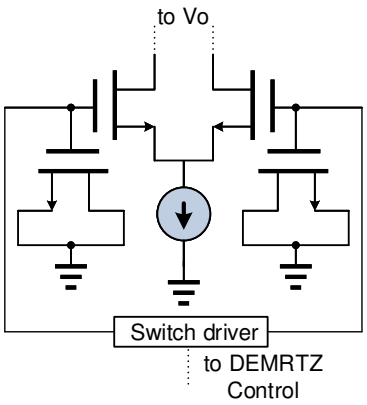

Fig. 4. Compensation capacitor

B. Splitting Decoder

Fig. 5 illustrates the Splitting Decoder, which converts a three-bit input into five outputs, as detailed in Table II. Its simplified Boolean algebra representation is provided in Eqn. (1). The logic is implemented using transmission gates, NMOS, and PMOS transistors, resulting in a more area-efficient design compared to traditional logic gate-based implementations.

$$\begin{aligned} &Y4 = B2 + B1; Y3 = B2 + B0; Y2 = B2; \\ &Y1 = B2 \cdot B1; Y0 = B2 \cdot B0 \end{aligned} \tag{1}$$

To mitigate nonlinearities caused by binary current source switching during intermediate code transitions, the lowest three bits (LLSB), B2–B0, are encoded into a five-bit split code, Y4–Y0. The current weights are redistributed from 4Iu, 2Iu, Iu to 2Iu, Iu, Iu, 2Iu, Iu, effectively reducing current variations during switching. This approach minimizes abrupt changes in the current, thereby improving linearity. For instance, during the transition of B2–B0 from 011 to 100, only Y2 switches from 0 to 1, requiring the activation of just one Iu switch. Compared to conventional binary-weighted current source switching, this method significantly reduces transient current variations and mitigates differential nonlinearity (DNL) errors.

TABLE II
SPLITTING DECODER TRUTH TABLE

Binary input			Splitting Decoder output				
B2	B1	B0	Y4	Y3	Y2	Y1	Y0
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	1	0	0	0
1	0	0	1	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	1

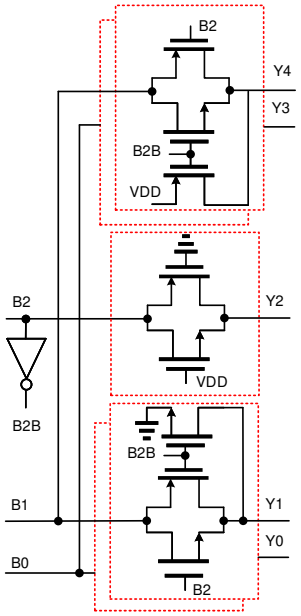

Fig. 5. Splitting Decoder

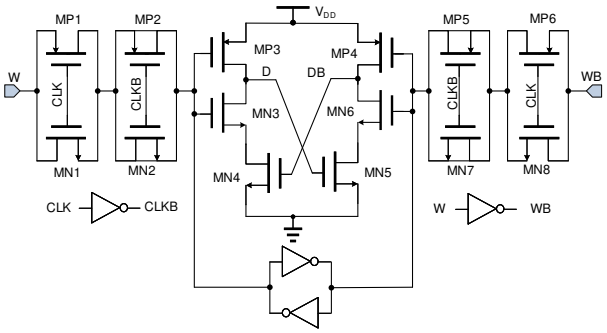

Fig. 6. Schematic of the Switch driver

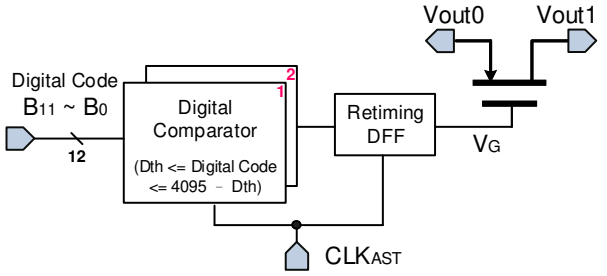

Fig. 7. Output Impedance Compensation

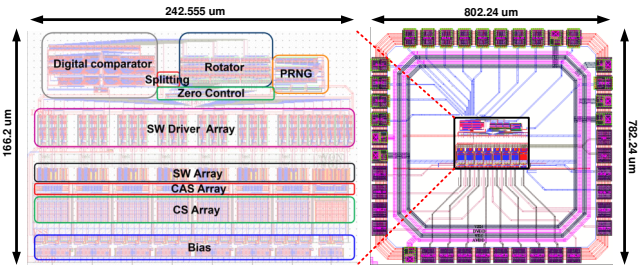

Fig. 8. Floor plan and layout

C. Switch driver circuit

To synchronize the input signal in high-speed circuits, a Switch Driver is used to compensate for delays between the DEM and DEMRTZ Control, as shown in Fig. 6. When the signal crossover point is at $(V_{DD}/2)$, insufficient bias voltage can simultaneously turn off the current sources, causing surges. The circuit raises the crossover point to prevent this issue. Additionally, to minimize surges from channel charge injection and clock feedthrough, a dummy switch is incorporated to stabilize the control signal during transitions.

D. Output impedance compensation (OIC)

Fig. 7 illustrates the OIC implementation, which comprises a Digital Comparator, Retiming DFF, and PMOS. In a two-stage VG generator, the compensation strategy is most effective when the digital input code is at the lower and upper extremes, as these regions exhibit greater imbalance in the scale [8]. Simulations were conducted with 128, 256, 512, and 1024 digital input values to determine the optimal compensation point. The results indicated that setting the compensation at 256 and 512 yielded the best performance, with both values producing nearly identical outcomes. Ultimately, 256 was selected as the final setting. Consequently, when the Digital Code is below 256 or above 3839 (where 3839 originates from 4095 - 256 in a 12-bit system spanning 0 to 4095), the PMOS operates in the cut-off region with high resistance to reduce approximation errors. Between 256 and 3839, it functions in the linear region to approximate the ideal resistance. Additionally, the assistant clock (CLK_{AST}) ensures proper V_G switching timing during the RTZ phase, minimizing nonlinear effects and improving SFDR by 7 dB.

III. POST LAYOUT SIMULATIONS

The proposed work is designed using TSMC TN40G process with a core circuit area of 242.555 $\times$ 166.2 μm^2 and a full-chip layout area of 802.24 $\times$ 782.24 μm^2, as shown in Fig. 8. It operates at 100 MHz with a power dissipation of 9.51 mW. Fig. 9 shows the simulated waveform diagram of the DEM Coder circuit. Fig. 10 shows the post-layout simulation, which verifies the Splitting Decoder circuit functioning and its truth table. When the digital input codes B2∼B0 switch from

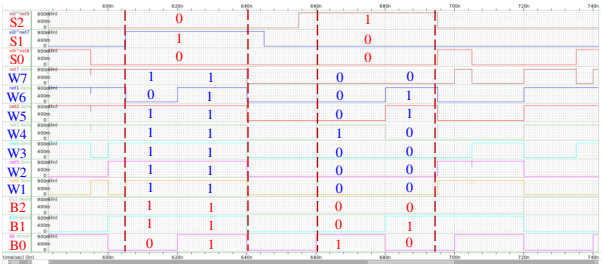

Fig. 9. DEM output waveforms

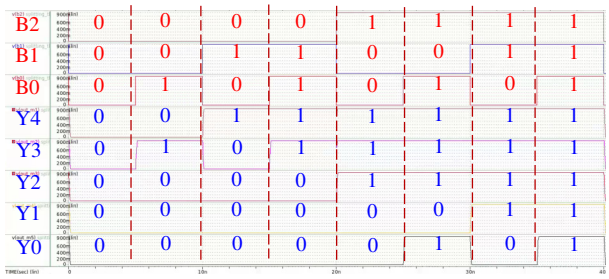

Fig. 10. Splitting encoder waveform

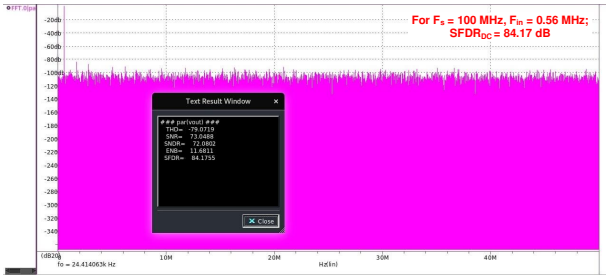

Fig. 11. TT, 25, 0.9 V, 0.56 MHz

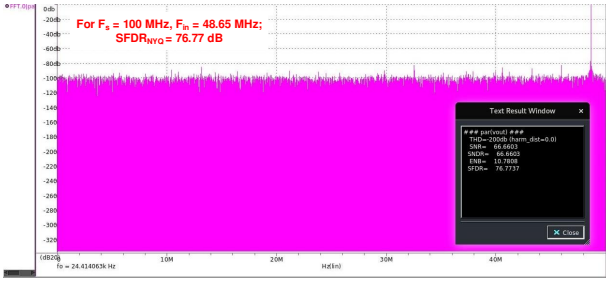

Fig. 12. TT, 25, 0.9 V, 48.65 MHz

011 to 100, the output will only turn on the Y2 current source, effectively reducing the generation of glitches and suppressing DNL. In the post-layout simulations, the worst DNL and INL at the 4096 sampling points are 0.7628 LSB and 0.5175 LSB, respectively. At 0.56 MHz, the DAC achieves an ENOB of 11.68 bits and SFDR of 84.17 dB, as shown in Fig. 11 and Fig. 12 illustrates the SFDR performance at a higher input frequency of 48.65 MHz, where the DAC achieves an ENOB of 10.78 bits and an SFDR of 76.77 dB. Our work is compared with previous designs, as summarized in Table III.

TABLE III
PERFORMANCE COMPARISON

Parameter	[3]	[4]	[5]	[6]	Our work
Technology	130 nm	180 nm	180 nm	28 nm	40 nm
Resolution	12 bits	10 bits	12 bits	12 bits	12 bits
f_s (MS/s)	100	500	500	1000	100
Supply Voltage (V)	1.5/1.2	1.8	1.8/1.2	1.5/0.9	0.9
Area (mm^2)	0.21	0.33	0.18	0.26	0.0403
$SFDR_{DC}$ (dB)	68.3	72.8	68.8	81	84.18
$SFDR_{NYQ}$ (dB)	62	70.12	62.1	65	76.77
I_{load} (mA)	16	10	6	8	8
P_{total} (mW)	18	30.24	17.2	33	9.51
FOM	0.49	3.9	2.8	5.5	140

$$FOM = \frac{2^{\frac{(SFDR_{NYQ}-1.76)}{6.02}} \cdot f_s}{Area} \times 10^{-6}$$

IV. CONCLUSION

This paper presents a highly linear and output impedance compensated current steering DAC with an efficient layout and enhanced dynamic performance. The integration of DEM, DEMRTZ control, and OIC significantly improves linearity and impedance characteristics, making it a suitable solution for high-speed and high-resolution applications like PNN systems. Post-layout simulations confirm the effectiveness of the design, demonstrating an ENOB of 11.68 bits and an SFDR of 84.17 dB at 0.56 MHz, and an ENOB of 10.78 bits and an SFDR of 76.77 dB at 48.65 MHz. These results validate the proposed techniques in achieving high performance. High SFDR is crucial for minimizing distortion in optical modulation, making the DAC well-suited for driving MZM. Future work will focus on further optimizing power efficiency and exploring advanced compensation techniques for improved performance.

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