Fully On-chip Isolated Gate Driver IC for Efficient Power Control

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***Abstract*—A high-efficiency and high-isolation power device driver system is disclosed in this investigation featuring an on-chip coil coupler to carry out high-speed digital signal transmission from the primary side to the secondary side, such that power MOSFETs in robotic systems, e.g., GaN and SiC devices, will be driven reliably and effectively. The proposed design is realized using a typical HV CMOS process and verified by on-silicon measurement to demonstrate 148 mW at 1 MHz data rate and 5 V power supply voltage.**

***Index Terms*—Gate driver, IGD, on-chip coil coupler, data transmission, HV CMOS**

I. Introduction

Modern mechanical systems like unmanned underwater vehicles (UUV), drones, and robots require converting low-voltage control signals into high-power outputs for actuators [1]. To meet portability demands, compact semiconductor solutions are preferred over bulky coil-based methods. While on-chip coils offer a lightweight option, they alone can't provide both isolation and data conversion. Modulation techniques like on-off keying help improve transmission [2] [3]. Despite prior discrete solutions, a fully integrated silicon-based driver is still missing. This work presents a miniaturized single-chip solution for robotic and motor control. The definition as well as the application scenario is disclosed in Fig. 1.

II. Design of the Single-chip Driver System

To ensure robustness and reliability, simplicity is prioritized in the system design. As shown in Fig. 2, the driver operates by receiving a 5 V digital input (V_{source}), which passes through a current-limiting resistor (R_{LIM}) for surge protection. The resulting signal (V_{PVDD}) is coupled through an on-chip transformer to generate V_{SVDD} on the high side. This voltage is then boosted and shaped into a square wave by a Schmitt trigger. The high-side control circuit outputs either a unipolar 5 V or bipolar 10 V digital signal, which drives the external power devices and load via split-path buffers and I/O pads. The single-chip driver includes four main blocks: Transformer, Level Shifter, Control, and Split Buffers.

A. Transformer

With advancements in semiconductor technology, the HV CMOS process (TSMC T18HVG2) offers six metal layers.

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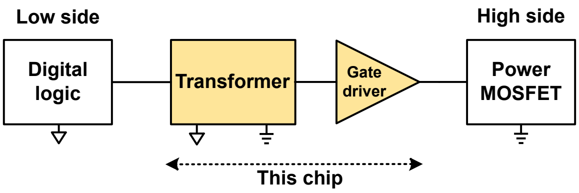

Fig. 1. Overview of the power driver system

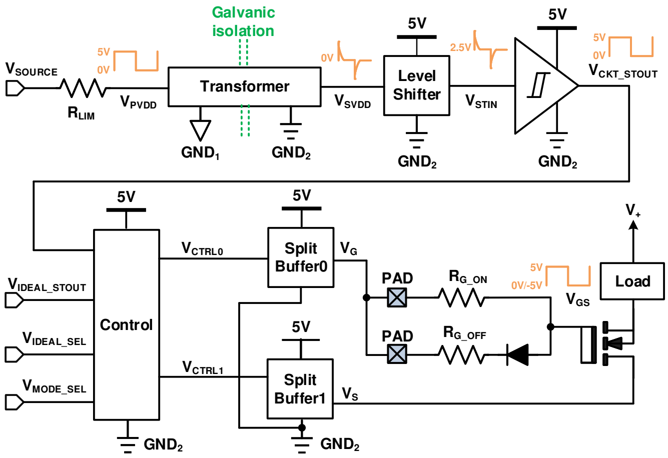

Fig. 2. Simplified view of the proposed power driver system

We utilize these layers efficiently: metals 2, 4, and 6 on the primary side, and metals 1, 3, and 5 on the secondary side. This interleaved structure maximizes inductance and achieves a high Q factor. Even- and odd-numbered layers are shorted via inter-layer connections. Several on-silicon coil layout styles—square, octagonal, and octagonal symmetric—have been reported. To determine the optimal transformer layout, we ran simulations using a fixed area of 525 × 525 μm^2, 20 μm trace width, and 2 μm spacing. Results are shown in Table I. The square style provides the highest inductance, making it the preferred choice for quality transmission. The structure of the transformer is shown in in Fig. 3(a).

B. Level Shifter

The Level Shifter in Fig. 2 is shown in Fig. 3(b), where C_0 is a 1 pF capacitor, R_2 and R_3 are 10 kΩ resistors.These passive elements are used to elevate the ground level of V_{SVDD} to 2.5

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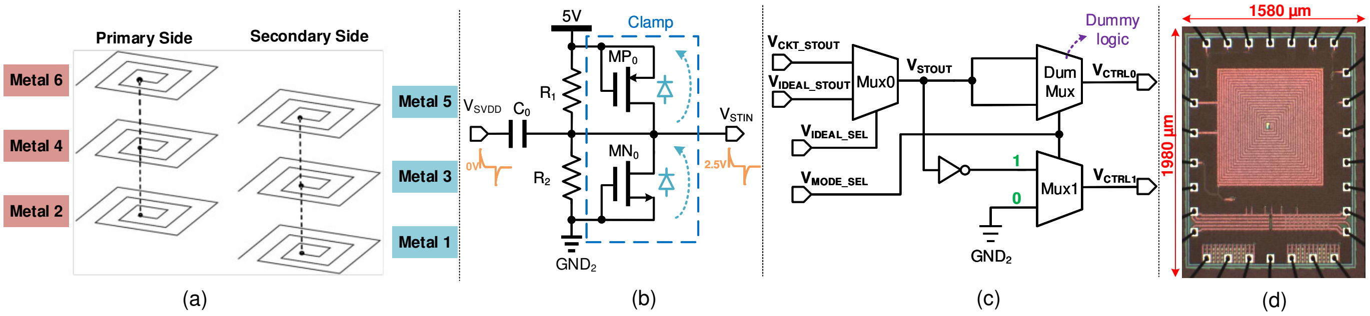

Fig. 3. (a) Metal layers to realize the coil pairs for the Transformer; (b) Schematic of Level Shifter; (c) Control circuit at the secondary side; (d) Die photo of the proposed design.

TABLE I
CHARACTERISTICS OF 3 ON-CHIP COIL LAYOUTS

	(a) square	(b) octagonal	(c) octagonal symmetric
Inductance (nH)	10.4	4.13	3.63
Resistance (Ω)	16.79	12.92	9.92
Capacitance (pF)	1.18	0.79	0.89

V in the secondary side. MP_0 and MN_0 are clamping diodes. Thus, the generated V_{STIN} coupled to the following Schmitt trigger will be effectively determined based on the relative negative voltage.

C. Control Logic and Split Buffers

The control logic on the secondary side, detailed in Fig. 3(c) (from Fig. 2), manages output signal generation. V_{CKT_STOUT} comes from the Schmitt trigger, while V_{IDEAL_STOUT}, selected by V_{IDEAL_SEL}, is for direct testing. V_{MODE_SEL} sets V_{CTRL1} to either GND (for V_{GS} of 10 V) or the inverse of V_{STOUT} (for V_{GS} of 5 V). V_{CTRL0} and V_{CTRL1} drive cross-coupled inverter chains, with a dummy multiplexer delaying V_{CTRL0} to match Mux1, ensuring synchronized outputs. The split buffers in Fig. 2 used to generate V_G and V_S are based on our previous work [4]–[6]. Each Split Buffer, is mainly composed of a pair of cross-coupled inverter chains, driving PMOS buffer array and NMOS buffer array, respectively.

III. ON-SILICON MEASUREMENT

To validate the proposed driver, simulations and on-chip measurements were performed. Fabricated using the TSMC T18HVG2 process. The overall chip area is 1580×1980 μm^2 and the core area is 1205×1515 μm^2. Fig. 3(d) shows the die photo, while Fig. 4(a) and Fig. 4(b) present bipolar and uni-phase outputs at 1 MHz and 5 V. The results confirm the expected single-chip performance.

IV. CONCLUSION

A total of six chips were tested, each measured over 30 times, confirming the design's credibility and robustness for robotic and motor driver applications. Future work will integrate the entire low-side digital signal processing unit into the same chip, potentially eliminating the need for external microprocessors.

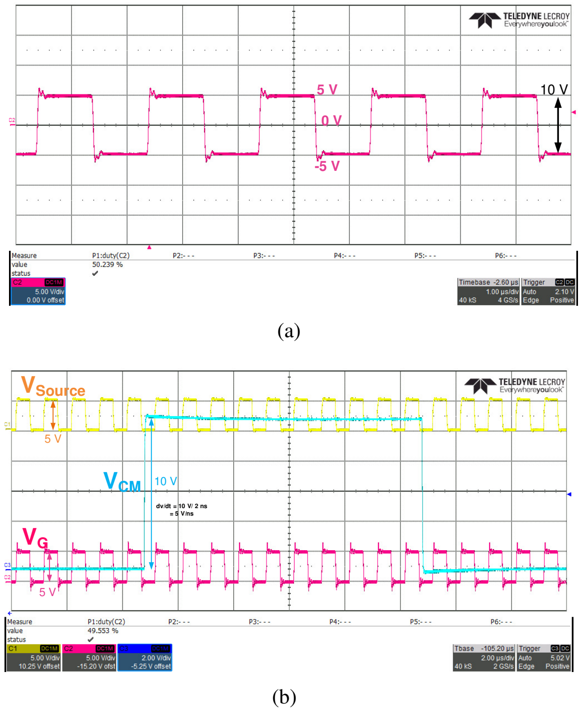

Fig. 4. (a) Measured waveforms of uni-phase output (0 to 5 V); (b) Measured waveforms of bi-phase output (-5 to +5 V).

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