A Wide Bandwidth TIA with Low Power Consumption for PNN Prototyping

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***Abstract*—This paper presents a high-speed, low-power transimpedance amplifier (TIA) designed for integration within photonic neural networks (PNNs). The proposed architecture, implemented using the TSMC TN40G process, incorporates an active-feedback TIA core, an inductor-less Balun, a digital DC Offset Calibration (DCOC) loop, and a combination of variable and fixed gain amplifier stages. The design addresses critical challenges in PNN systems, including wide bandwidth, low power consumption and offset sensitivity caused by analog front-end mismatches. Post-layout simulations demonstrate a gain tuning range of 33.2 dBΩ to 70.3 dBΩ and a bandwidth of 4.08 GHz, with consistent performance across all PVT corners. The proposed TIA design highlights enhanced bandwidth, power efficiency and enhanced signal fidelity, making it suitable for the PNN system realization.**

***Index Terms*—TIA, Digital DCOC, PNN, MZM, Balun, Gain, Bandwidth.**

I. Introduction

Photonic neural networks (PNNs) are gaining traction as a viable pathway for advancing future AI technologies [1], [2]. However, the realization of PNNs requires sophisticated digital-to-analog conversion (DAC) technology to convert the image information into voltage signals [3]. The key component of PNN architecture is the Mach-Zehnder Modulator (MZM), which converts electrical signals into optical signals and facilitates essential operations like matrix-vector multiplications (MVM) through appropriate biasing [4]. The summation of the optical power across various wavelength paths must be converted back into an electrical signal using a photo diode [5]. Following this, a reliable Transimpedance Amplifier (TIA) is needed to recover the convolution outcome as an electrical signal suitable for further processing by following digital systems. A PNN prototype realized by our team is demonstrated in Fig. 1. Though numerous TIA designs have been previously reported, many suffered from limited bandwidth and high power consumption [6]–[9]. While some TIAs have been proposed specifically for optical communication applications, they also tend to exhibit trade-offs between bandwidth and power efficiency [10], [11]. This research is focused on the design of a TIA that achieves wide bandwidth and low power consumption, tailored to meet the stringent performance requirements of PNN systems.

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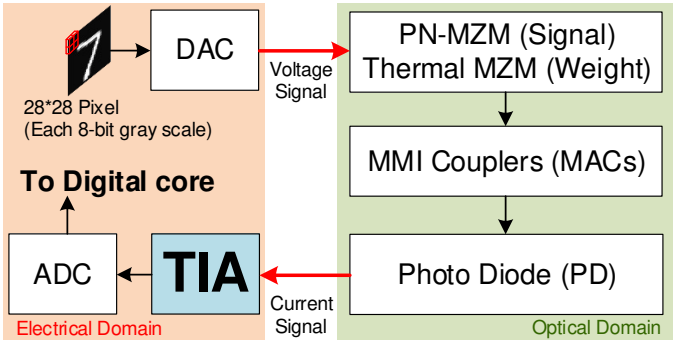

Fig. 1. The prototype of the PNN system

II. Architecture of the Proposed TIA

The TIA in Fig. 1 is disclosed as system architecture in Fig. 2. The TIA system architecture integrates several functional blocks, including a photo detector equivalent circuit, TIA-core, Balun, a two-stage variable-gain amplifier (VGA), dual-level fixed gain amplifiers (FGA), Bias circuit, a novel digital DC Offset Calibration (DCOC) feedback loop and a Buffer circuit from our previous works [12]–[14]. These blocks work together to enhance bandwidth and reduce power dissipation.

The TIA system architecture, begins with a TIA-Core that provides low input impedance. This prevents the large input capacitance of the photo detector from limiting the overall system bandwidth. The TIA-Core also delivers primary gain, which helps to reduce input-referred noise. The output of TIA-Core (TIA_{OUT}) is fed to the Balun, which converts single-ended into a differential signal. Compared to dual-PD designs, this approach avoids mismatch errors but introduces new challenges, such as phase and gain errors due to the Balun. The proposed TIA incorporates two stages of VGA for variable gain control and dual-level FGAs to provide additional fixed gain. To manage DC offset, a digital DCOC loop is implemented. Unlike conventional analog RC feedback systems, which risk instability, this digital calibration approach avoids oscillation and yields a low-pass Bode plot rather than a band-pass response.

A. TIA-Core

The schematic of the TIA-Core is shown in Fig. 3. Unlike traditional common-gate circuits or regulated cascode topolo-

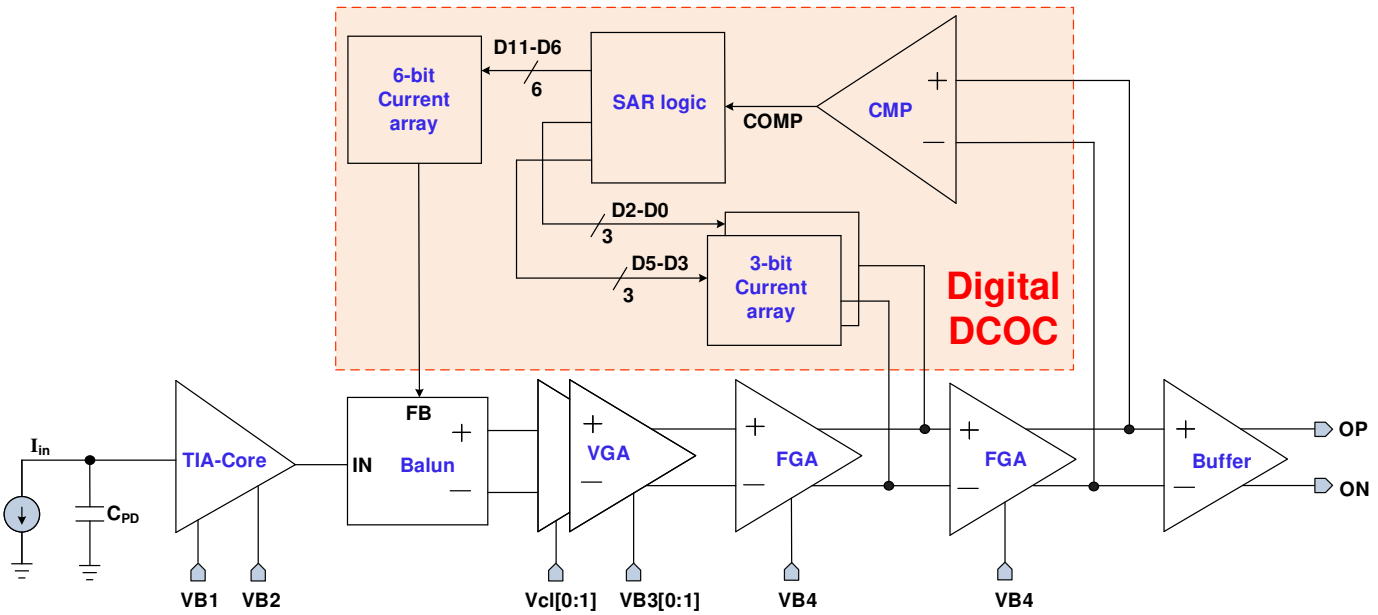

Fig. 2. System architecture of the proposed TIA

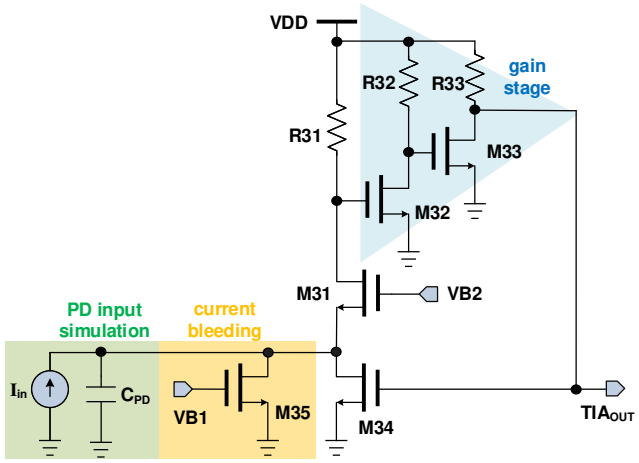

Fig. 3. Schematic of the TIA-Core [11]

gies, this topology employs active feedback combined with a current bleeding circuit to enhance gain while supporting low-voltage operation. The two stages of common-source amplifiers in the feedback will reduce the input resistance (R_{input}) of the TIA. This reduction in (R_{input}) improves the bandwidth without affecting the gain. The expressions for R_{input} and gain are given in the Eqn. (1) and (2), respectively.

$$R_{input} \approx \frac{1}{g_{m31}(1 + g_{m32}g_{m33}g_{m34} \cdot R_{31}R_{32}R_{33})} \quad (1)$$

$$gain \approx \frac{g_{m32}g_{m33} \cdot R_{31}R_{32}R_{33}}{1 + g_{m32}g_{m33}g_{m34} \cdot R_{31}R_{32}R_{33}} \approx \frac{1}{g_{m34}} \quad (2)$$

B. Balun

The Balun implemented in this design is an inductor-less active Balun, and its schematic is shown in Fig. 4. To correct phase and gain errors, the design employs the magnitude and phase concurrent correction technique (MPCCT), which utilizes both positive and negative feedback paths [15]. A = Z_L represents an open-loop transimpedance gain. The terms $\beta_p^{\pm}$ and $\beta_n^{\pm}$ represent feedback factors of the positive and negative feedback at the plus and minus sides of Balun-A, respectively. The resulting output voltages V_1 and V_2 are expressed by Eqn. (3) and (4), respectively [16].

$$V_1 = \frac{1}{\delta}\left[\left(\frac{1}{A} + \beta_n^-\right)I_1 - \left(\beta_p^-\right)I_2\right] \quad (3)$$

$$V_2 = -\frac{1}{\delta}\left[\left(\beta_p^+\right)I_1 - \left(\frac{1}{A} + \beta_n^+\right)I_2\right] \quad (4)$$

The expression for the δ is given in the Eqn. (5). Eqn. (6) presents the condition under which the coefficients on the right-hand sides of Eqn. (3) and (4) become equal.

$$\delta = \left(\frac{1}{A} + \beta_n^-\right)\left(\frac{1}{A} + \beta_n^+\right) - \beta_p^- \cdot \beta_p^+ \quad (5)$$

$$\frac{1}{A} + \beta_n^{\pm} = \beta_p^{\mp} \quad (6)$$

When Eqn. (6) is satisfied, V_1 and V_2 differ only in sign, indicating that the output achieves perfect differential voltage. By assuming $\beta_p^{\pm} = \beta_p$, $\beta_n^{\pm} = \beta_n$ and G_A is the output conductance of Balun-A, the expressions for β_p and β_n are given in Eqn. (7) and (8), respectively.

$$\beta_p = \frac{G_A \cdot g_{m8}}{G_A + g_{m8}} \quad (7)$$

$$\beta_n = \frac{g_{m8}g_{m4}g_{m6} \cdot R_p}{(G_A + g_{m8})(1 + R_p)} \quad (8)$$

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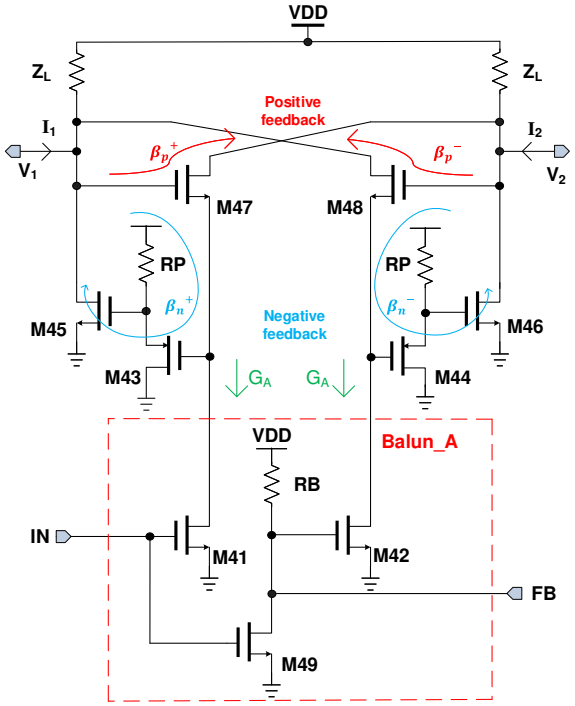

Fig. 4. Schematic of the Balun

C. VGA & FGA

The VGA in Fig. 2 adopts a classic Gilbert cell configuration to enable a wide range of gain adjustment [17]. By efficiently utilizing a differential pair for the gain control, the design reduces the number of required control voltages from two to one. This simplification streamlines the control interface while maintaining gain tunability.

The FGA incorporates both resistive and capacitive degeneration techniques [17]. Resistive degeneration improves linearity, enhances stability, and mitigates process variation, though the cost of reduced gain is an issue. Capacitive degeneration provides a low-impedance bypass path, which increases the high-frequency gain by minimizing the impact of the degeneration resistor at high frequencies, thereby extending bandwidth.

D. Digital DCOC

In a single-stage differential amplifiers with low-gain, minor layout asymmetries often introduce small offsets. In multi-stage high-gain designs, these offsets can accumulate, resulting in a significant offset in the final output stage. To mitigate this, DCOC circuits are commonly employed. Conventional analog DCOCs use RC filters to separate DC and AC components, along with the comparators to detect the offset magnitude and feed it back to an adjustable DC bias point. This approach enables accurate offset cancellation during signal operation. However, analog DCOCs require large-area RC filters for high-frequency signals and typically produce a band-pass Bode plot, as the low-frequency (DC) signal suppressed along with offset.

TABLE I
POST-LAYOUT SIMULATION RESULTS AT 5 EXTREME PVT CORNERS

Parameter	Value	Value	Value	Value	Value
Process Corner	TT	FF	SS	SF	FS
Power Supply (V)	0.9	0.99	0.81	0.9	0.9
Temperature (°C)	25	0	80	25	25
C_{PD} (pF)	1	1	1	1	1
Gain (dBΩ)	70.3	63.5	66.4	61.3	68.7
Bandwidth (GHz)	4.08	4.32	4.02	4.28	4.22
Gain variation range (dBΩ)	33.2∼ 70.3	28.1∼ 63.5	30.4∼ 66.4	28.7∼ 61.3	32.9∼ 68.7
Input-referred Noise (pA/$\sqrt{Hz}$)	24.64	33.2	26.4	27.6	25.9
DC Offset (mV)	2.2	3.4	1.3	1.8	2.1
Phase error (°)	0.766	0.322	0.003	0.259	0.268
Total Power dissipation (mW)	16.7	25.7	8.64	12.18	19.45
Power dissipation w/o Buffer (mW)	7.4	12.7	3.69	7.02	7.65

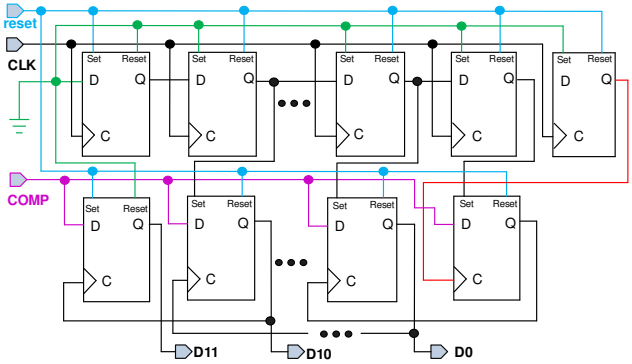

Fig. 5. Schematic of the SAR logic in digital DCOC

The proposed TIA design implements a novel digital DCOC that performs calibration prior to applying input signal using a clocked comparator (CMP). The CMP gives logic '1' as output, if the potential at the differential positive terminal is higher than the negative terminal; otherwise, it outputs logic '0'. This binary result is processed by clocked SAR logic, which controls the Current array, thereby balancing the DC levels of the differential pair to minimize offset. The schematic of the SAR logic is shown in Fig. 5. The CMP and SAR logic are clocked out-of-phase using inverters to avoid metastability.

The Current array is divided into three sub-arrays: 6-bit, 3-bit and 3-bit, each with binary-weighted current steps, like 2^1 μA, 2^2 μA, ..., 2^6 μA. These sub-arrays are distributed across the Balun and FGA outputs to form feedback paths. The higher-resolution (6-bit) array output is applied as input to the FB terminal of Balun, because any available offset is magnified by the downstream amplifiers. The latter stages require few bits due to the diminishing influence of their offsets.

III. VERIFICATION BY POST-LAYOUT SIMULATIONS

The proposed work is designed using TSMC TN40G process with a core circuit area of 174.295 × 35.74 μm^2 and a full-chip layout area of 561.81 × 465.56 μm^2, as shown in Fig. 6. The functionality is verified through various all-

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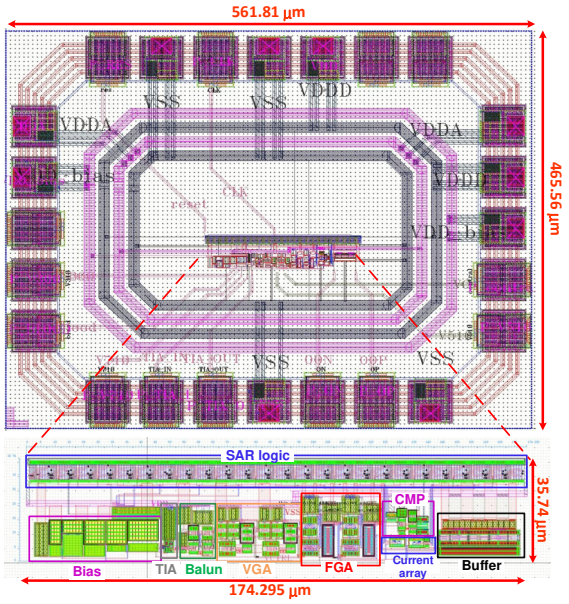

Fig. 6. Chip layout of the proposed TIA design

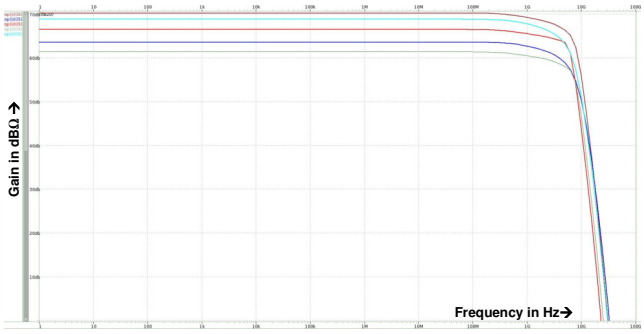

Fig. 7. Post-layout simulations at 5 extreme PVT corners: Gain-bandwidth characteristics

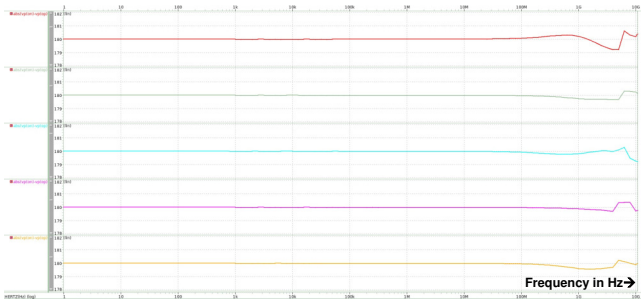

Fig. 8. Post-layout simulations at 5 extreme PVT corners: phase error

PVT-corner (Process, Voltage, Temperature) post-layout simulations. The Gain-Bandwidth characteristics and phase error across 5 extreme PVT corners are shown in Fig. 7 and 8, respectively, with corresponding data summarized in Table. I. At [TT, 25°C, VDD] corner, the variable gain control range is 33.2 dBΩ to 70.3 dBΩ, and is shown in Fig. 9. A performance comparison between this work and previously reported TIA designs is presented in Table II, highlighting the proposed

TABLE II
PERFORMANCE COMPARISON

Parameter	[6]	[7]	[8]	[9]	Ours
Technology (nm)	110	110	28	180	40
Power Supply (V)	3.3	1.8	1.8	3.3	0.9
Output signal type	Diff.	Diff.	Diff.	Sing.	Diff.
C_{PD} (pF)	0.35	1	N.A.	1.5	1
Gain (dBΩ)	80	99	74	100	70.3
Bandwidth (GHz)	2.4	0.34	0.5	0.26	**4.08**
Input-referred Noise (pA/$\sqrt{Hz}$)	3.6	3.67	N.A.	3.3	24.64
Total Power dissipation (mW)	158.4	41	59	29.4	16.7 (Core:**7.4**)
FOM	151.5	739	42.4	884.3	**1804.8**

FOM= (Gain(Ω) × Bandwidth (GHz)) / (Power dissipation (mW))

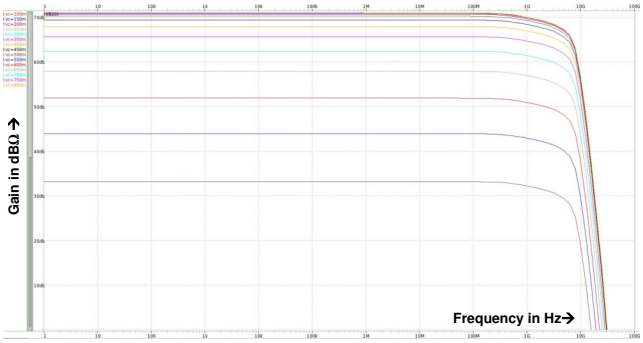

Fig. 9. Variable gain control range at [TT, 25°C, VDD] corner

TIA's advantages in terms of bandwidth, gain tunability, and power efficiency.

IV. Conclusion

This paper presents the design and post-layout verification of a high-performance TIA tailored for PNN systems. The proposed TIA architecture integrates a low input-impedance TIA-Core with an active feedback, a digital DC Offset Calibration feedback loop, and a combination of variable and fixed gain amplifier stages to achieve both wide bandwidth and low power consumption. Implemented in the TSMC TN40G process, the design demonstrates strong performance across process corners, with a variable gain range from 33.2 dBΩ to 70.3 dBΩ and a bandwidth of 4.08 GHz. The use of a digital DCOC loop eliminates large analog RC components and supports a low-pass system response, making it highly suitable for modern high-speed, low-power optical systems. Simulation results confirm that the proposed design achieves a favorable balance between bandwidth, gain flexibility, and power efficiency, making it a strong candidate for integration in future optical and hybrid AI computing platforms.

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