A Digital PWM of 10-bit With Clock Gating Technique and Conditional Capture MS-DFFs

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***Abstract*—This study presents a high-resolution (N=10) Digital Pulse Width Modulation (DPWM) with redundant clock activity using the clock gating technique based on conditional capture logic to the master-slave D flop-flops in the clock counter. This design also uses a very small number of D flip-flops (DFFs) that is far less than the theoretical number, 2^N. Our design uses a single clock to achieve high clock frequency and synchronization. The proposed DPWM design is implemented in the 40-nm CMOS process. The core area of the design is 229.13 $\times$ 290.24 μm^2. The DPWM functionality is verified through 45-PVT-corner post-layout simulations. The range of duty cycle obtained is from 0.1% to 99.9% at an operating frequency of 500 MHz with a load 30 pF and 5.12 mW is the power dissipation at the highest clock frequency.**

***Index Terms*—DPWM, clock activity, conditional capture, clock gating, master-slave D flip-flops, 10-bit Magnitude Detector**

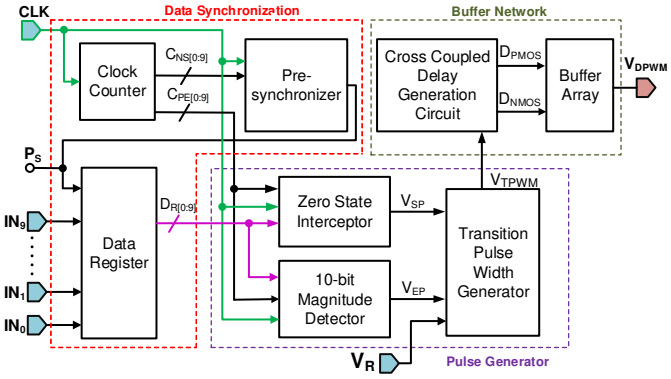

Fig. 1. Proposed Digital PWM using clock gating technique

I. Introduction

Integrated dc-dc converters are vital in power management systems, necessitating high efficiency, ease of adjustment, and effective control [1]. When contrasted with analog systems, digital control presents considerable benefits for power DC-DC regulation. One specific type of digital controller, Digital PWM (DPWM), operates effectively at low voltage supplies while maintaining a low quiescent current, making it particularly suitable for low-power functions [2], [3]. A DPWM designed in 40-nm CMOS employed an extensive series of D flip-flops (DFFs) for low-power PWM buck converters, as documented [4]. This controller enhances the power efficiency of the buck converter by automatically selecting between discontinuous conduction mode and continuous conduction mode. Nevertheless, it features three clock inputs, which complicates synchronization and operation at varying frequencies.

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In our prior design [5], a DPWM is implemented utilizing a singular clock alongside a matrix shift array, which facilitates scalability to various frequencies while mitigating the impact of clock skew. Even though the design uses a single clock, its highest duty cycle achieved is only 90%, and the number of DFFs required for high resolution increases rapidly. In our prior succeeding design [6], a DPWM technique employs a reconfigurable decoder, necessitating only a minimal quantity of DFFs, but suffers with redundant clock activity.

The proposed DPWM design utilizes Conditional Capture Master-Slave DFFs (CCMS-DFFs) to minimize the redundant clock activity. A 10-bit resolution is implemented in this design to prove functionally applicable to a higher resolution with a maximum achievable duty cycle of 99.9%.

II. Clock Gating Technique based DPWM

Fig. 1 illustrates the proposed DPWM architecture, which contains three main blocks, namely Data Synchronization, Pulse Generator, and Buffer Network. The Data Synchronization block will decide the % of the duty cycle of the

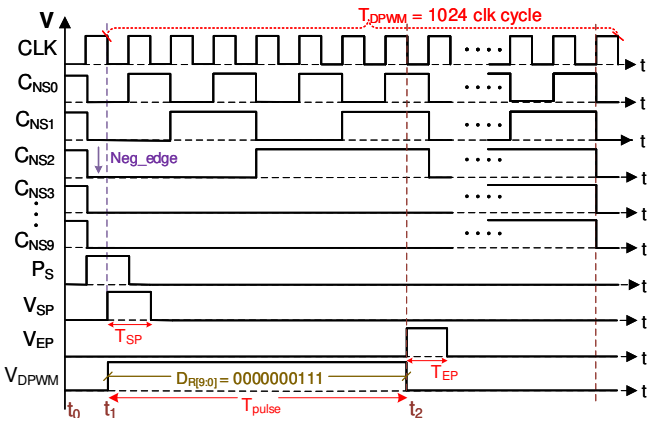

Fig. 2. Proposed DPWM timing diagram

DPWM. The Pulse Generator block originates V_{SP} (start of the pulse) and V_{EP} (end of the pulse) that point the start and end points in the timeline of V_{DPWM}, resultantly. During transitions, the Buffer Network block eliminates overshoots and provides better impedance matching for loads. The timing diagram of the proposed design is illustrated in Fig. 2. Based on the input code $IN_{[0:9]}$, the width of T_{pulse} will be varied. The 10-bit Magnitude Detector generates V_{EP} signal to mark the end point of the V_{DPWM}, when $C_{PE[0:9]} = IN_{[0:9]}$.

A. Data Synchronization

The Data Synchronization block consists of three subparts, which include the Data Register, Clock Counter, and Pre-synchronizer.

1) Clock Counter: The Clock Counter performs the most critical timekeeping operations for the DPWM architecture. The Clock Counter generates a binary representation (N bits) of the clock pulses which enables logic circuitry to produce time-delayed signals to determine the pulse width of the V_{DPWM}. The number of bits in the Clock Counter determines the resolution of the V_{DPWM}. The time delay is represented by the number of clock cycles.

In our prior design [6], for this timekeeping operation, a string of double-edge-triggered (positive edges for the present state and negative edges for the next state) DFFs were implemented. This causes a lot of redundant clock activity in the counter, especially at those bits close to MSB. This redundant clock activity causes meaningless power consumption and serious clock skew.

The proposed DPWM architecture minimizes the redundant clock activity by introducing a clock gating technique based on Conditional Capture Master-Slave D flip-flop (CCMS-DFF). The CCMS-DFF will be updated only when the present state C_{PEX} and next state C_{NEX} are not the same. Fig. 3 depicts logic implementation for the clock gating technique, where P_c signal generated through the exclusive-OR gate represents the conditional capture logic. The exclusive-OR gate ensures that the D flip-flop (DFF) is only updated when D_{in} is not equal to Q_{NE}. The clock gating action is controlled using an AND gate.

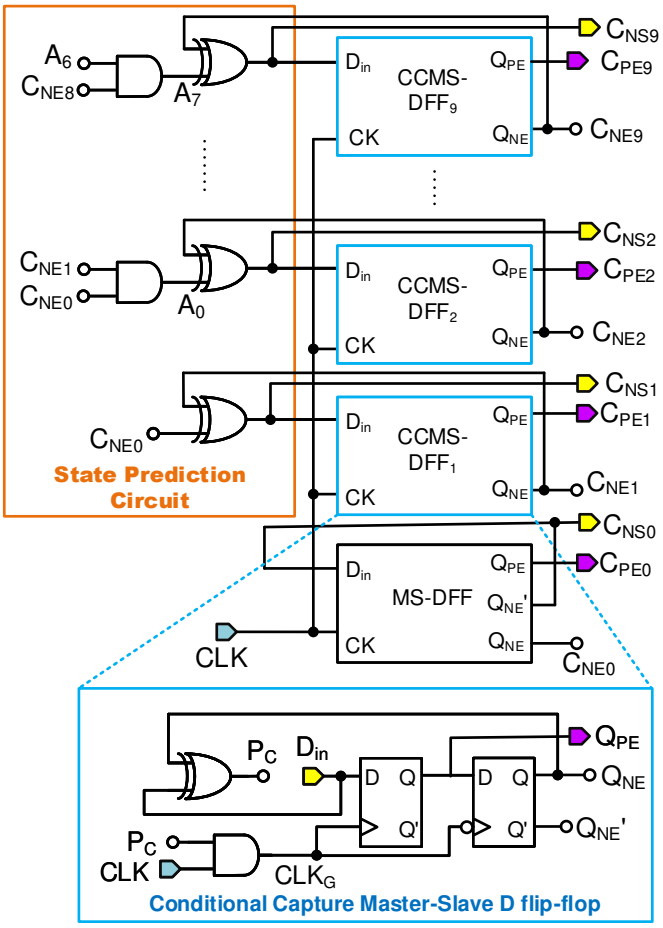

Fig. 3. Schematic of Clock Counter

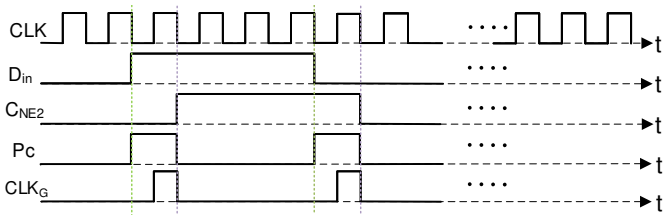

Fig. 4. Functional timing diagram of CCMS-DFF$_2$

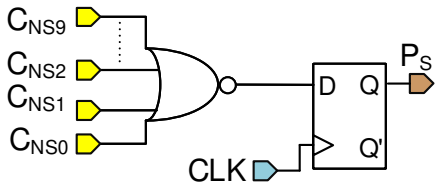

Fig. 5. Pre-synchronizer schematic

For instance, the functional timing diagram of CCMS-DFF$_2$ is illustrated in Fig. 4.

2) Pre-synchronizer: The Pre-synchronizer block determines the data sampling interval, which also coincides with the V_{DPWM} time period (T_{DPWM}). The period (T_{DPWM}) is

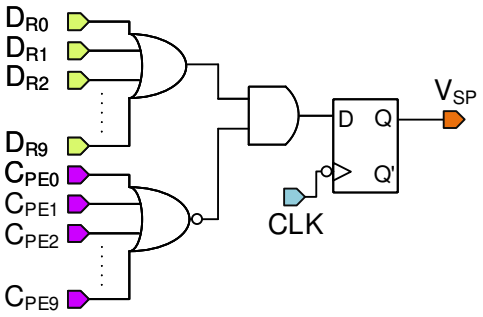

Fig. 6. Schematic of Zero State Interceptor

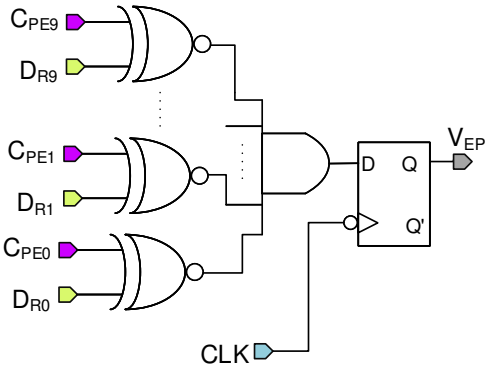

Fig. 7. Schematic of 10-bit Magnitude Detector

determined as binary multiples of clock period T_{CLK} as given in Eqn.(1).

$$T_{DPWM} = (2^N) * T_{CLK} \quad (1)$$

where N refers to the number of Clock Counter bits.

Illustrated in Fig. 5 is the schematic of the Pre-synchronizer, which generates P_S periodically after every T_{DPWM}. The 10-bit NOR gate detects when the counter is reset to its initial state represented by $C_{NS[0:9]}$ = 0000000000. The DFF produces a stable P_S signal from the 10-bit NOR gate through a delayed triggering at an alternative clock edge. This delayed transition ensures that the logic output reaches a stable state, thereby minimizing the occurrence of glitches in the P_S. A similar circuit is also implemented in the prior work [6], but the generated P_S signal suffered with half-clock cycle delay from the counter output.

To minimize the delay the 10-bit NOR gate inputs are taken from the State Prediction Circuit, $C_{NS[0:9]}$, instead of the Clock Counter outputs $C_{PE[0:9]}$. As the name suggests the State Prediction Circuit predicts the next state of the counter from the current state $C_{NE[0:9]}$. This means the 10-bit NOR gate output is generated when the current state output $C_{NE[0:9]}$ is equal to 1111111111.

3) Data Register: In the proposed DPWM architecture the Pre-synchronizer determines when the data needs to be sampled. The sampled data is stored throughout the T_{DPWM} interval to maintain the stability of the system. To accomplish this task, a 10-bit parallel-in-parallel-out register comprising of positive edge DFFs is used. Any input data changes during the T_{DPWM} interval will be updated at the positive edge of the P_S signal.

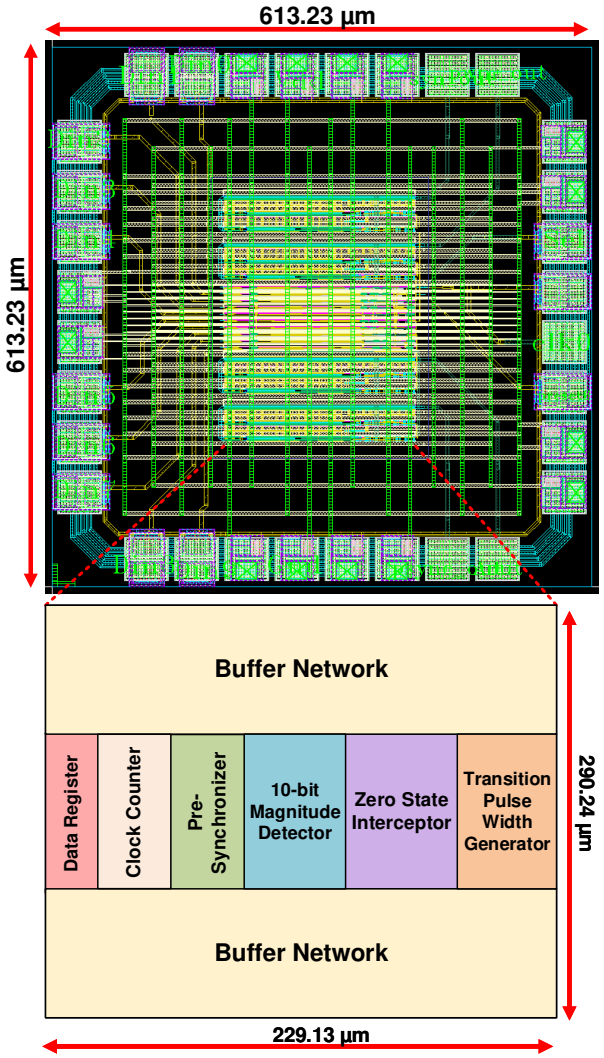

Fig. 8. DPWM layout and floor plan

B. Pulse Generator

The Pulse Generator block consists of three subparts, which include Zero State Interceptor, 10-bit Magnitude Detector, and Transition Pulse Width Generator.

1) Zero State Interceptor: As illustrated in Fig. 6, the Zero State Interceptor generates the start point signal V_{SP} periodically when the Clock Counter output $C_{PE[0:9]}$ is equal to 0000000000. As the name implies the circuit inhibits the V_{SP} signal when the Data Register output $D_{R[0:9]}$ is at zero state (0000000000). This interception is necessary, since no PWM signal needs to be generated when the data register output is zero. The circuit is implemented with the help of a 10-bit OR gate, which detects the zero state at the Data Register output and AND gate to perform the inhibition function.

2) 10-bit Magnitude Detector: The end point of the output PWM signal V_{DPWM} is defined as V_{EP} and is generated by

TABLE I
PERFORMANCE COMPARISON OF DPWM DESIGNS

	[13]	[12]	[5]	[6]	Our work
Year	2019	2021	2022	2023	2025
Publication	ICEIC	AICSP	ISCAS	MWSCAS	iEECON
Technology	65-nm	180-nm	180-nm	180-nm	40-nm
Verification	Post-Layout Sim.	Measurement	Post-Layout Sim.	Post-Layout Sim.	Post-Layout Sim.
VDD (V)	0.6	1.3	1.8	1.8	0.9
Clock frequency (MHz)	64	2	6.25	200	500
Resolution (bits)	6	5	4	8	10
Max. Duty Cycle	50%	70%	90.6%	99.6%	99.9%
Core area (mm^2)	0.0317	2.25	0.205	0.325	0.0665
Load	4.7 μH	10 μF & 2.2 μH	60 pF	10 μF & 8 μH	30 pF
Power Diss. (mW)	N/A	17.8 @ 2 MHz	5.05 @ 6.25 MHz	188 @ 200 MHz	5.12 @ 500 MHz

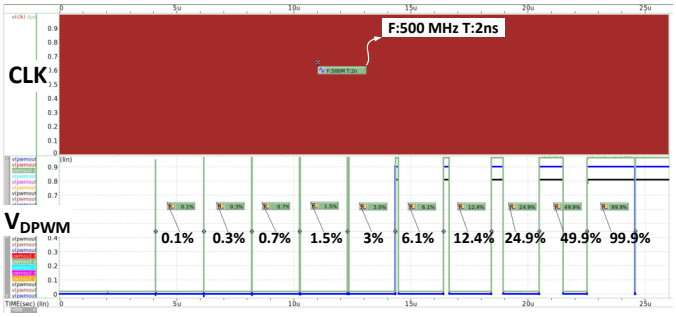

Fig. 9. 45-PVT-corner post-layout simulations of V_{DPWM}

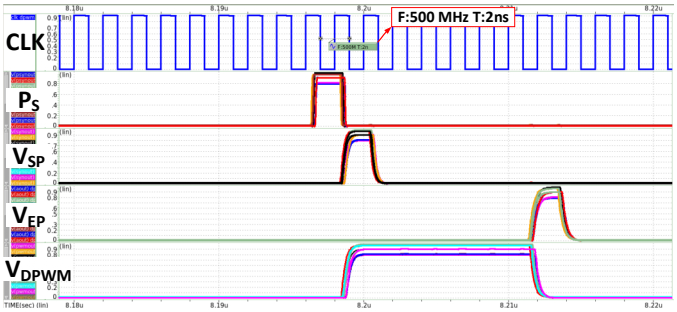

Fig. 10. 45-PVT-corner post-layout simulations of V_{DPWM} for $D_{R[0:9]}$=0000000111

the 10-bit Magnitude Detector when the Clock Counter output $C_{PE[0:9]}$ is equal to the Data Register output $D_{R[0:9]}$ which is user-defined. The schematic of 10-bit Magnitude Detector is illustrated in Fig. 7.

3) Transition Pulse Width Generator: The pulse width (T_{pulse}) of the V_{DPWM} is defined as the time difference between two signals V_{SP} and V_{EP} as shown in the Fig. 2. The T_{pulse} is inclusive of V_{SP} period (T_{SP}) while excluding V_{EP} period (T_{EP}). The design of this block is similar to our previous design [6].

C. Buffer Network

The Buffer Network utilizes a non-overlapping circuit depending on a split path architecture as reported in our previous design [7]–[11]. The Cross Coupled Delay Generation circuit introduces a dead time that eliminates shoot-through when the buffer is driven during transitions.

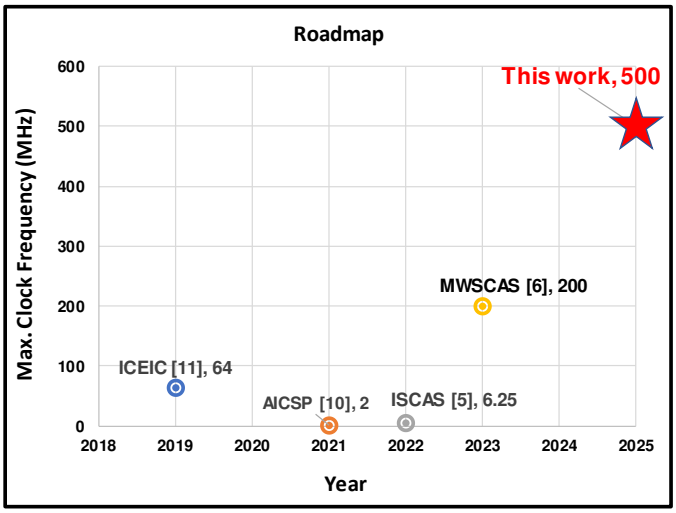

Fig. 11. Roadmap

III. VERIFICATION BY POST-LAYOUT SIMULATIONS

Using the 40-nm CMOS process, the proposed DPWM design is implemented. The chip layout is illustrated in Fig. 8. The design is analyzed at various process (SS, TT, FF, SF, FS), voltage (VDD, VDD-10%, VDD+10%), and temperature (0°C, 25°C, 75°C). To verify the functionality, the inputs $IN_{[0:9]}$ are applied from a 10-bit Johnson Counter. For a 500 MHz clock frequency, with a 30 pF load capacitance, the output V_{DPWM} at 45-PVT-corner post-layout simulations are illustrated in Fig 9. It can be observed that the duty cycle is varying from 0.1% to 99.9%. For $D_{R[0:9]}$=0000000111, the V_{SP}, V_{EP}, P_S, V_{DPWM} can be observed in Fig 10, at 45-PVT-corner simulations. The timing diagram shown in Fig. 2 is verified by the results of post-layout simulations as shown in Fig. 10. Table I presents a comparative analysis of the performance of our research in relation to earlier DPWM studies. Fig. 11 illustrates the maximum operating clock frequency roadmap of DPWMs in recent years [5], [6], [12], [13]. Apparently, the DPWM proposed in this investigation is with maximum operating clock frequency and also with maximum duty cycle.

IV. Conclusion

This study presents a DPWM using the clock gating technique using 40-nm CMOS process. In this design, a significantly small number of DFFs are used compared to prior works because of the modifications carried out in the 10-bit Magnitude Detector and the Data Register. The redundant clock activity leads to excess power consumption and clock skew, which is eliminated in this work by using clock gating in the CCMS. The duty cycle obtained is 0.1% to 99.9% at an operating frequency of 500 MHz with a load of 30 pF with a power dissipation of 5.12 mW. The proposed clock-gated DPWM is highly suitable for digitally controlled DC–DC buck converters in power management integrated circuits (PMICs), enabling high-resolution, energy-efficient voltage regulation at high operating frequencies

V. Acknowledgment

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