POGroup Layout Techniques of 7-nm FinFET Technology to Realize A 10-GHz Comparator

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***Abstract*—This paper presents a 10-GHz dynamic comparator implemented in 7-nm FinFET (TN7) technology for photonic neural network (PNN) prototyping. The design is based on the StrongARM latch architecture with inverter buffers added at both outputs to enhance symmetry and reduce offset. A POGroup-based layout technique is applied to merge closely spaced poly gates, improving uniformity and process tolerance while allowing flexible cell adjustment. Additional layout measures, including cut-poly separation, guard-ring isolation, and mitigation of MBE, LOD, and SALE2 effects, further enhance matching and robustness. Post-layout simulations using TSMC TN7 process demonstrate stable operations up to 10 GHz with full-swing output and low power consumption of 74.6 μW at the (TT, VDD, 25°C) corner. The compact 10.35 μm^2 core layout and 38.8 μm^2 total area make the design suitable for high-density ADC arrays in next-generation PNN systems.**

***Index Terms*—Comparator, FinFET, POGroup layout, StrongARM latch, 7-nm technology, PNN prototyping.**

I. Introduction

Photonic neural networks (PNNs) have emerged as a promising platform for next-generation artificial intelligence (AI) systems, combining the massive parallelism of optical computing with the flexibility of electronic control [1]. To realize these hybrid systems, GHz-level mixed-signal circuits such as digital-to-analog converters (DACs), transimpedance amplifiers (TIAs), and analog-to-digital converters (ADCs) play a vital role in bridging the electronic and photonic domains [2]–[6]. A key element in this architecture is the Mach–Zehnder Modulator (MZM), which converts electrical throughput signals into optical carriers for high matrix–vector multiplication (MVM) operations. The modulated optical power is detected by a photodiode (PD), amplified by a TIA, and converted to a voltage signal through an I–V conversion stage. This analog voltage is then digitized by the ADC array to interface with the digital core of the PNN system. The optical–electrical (O–E) interface implemented by our team is shown in Fig. 1.

Within the ADC, the comparator serves as the core decision-making component that determines both the accuracy and conversion speed of the entire system. Its performance directly affects the effective number of bits (ENOB), signal-to-noise ratio (SNR), and overall dynamic behavior of the converter. As PNN systems demand high-speed and energy-efficient data conversion under tight area constraints, achieving precise voltage comparison at nanosecond time scales and millivolt-level resolution has become a major design challenge. Also, high-speed and energy-efficient Comparator is an important circuit in the design of Active Gate Drivers [7]–[10].

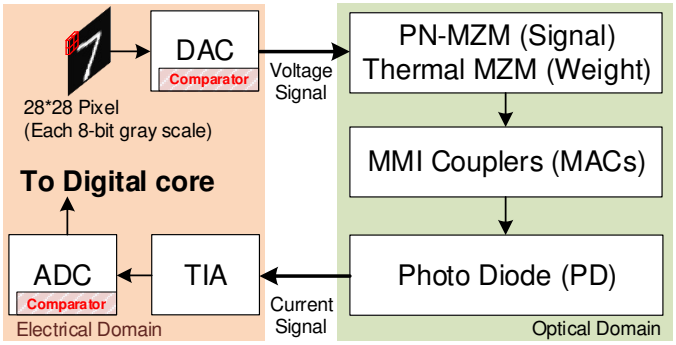

Fig. 1. The positioning of comparators in a PNN system

In deep-submicron technologies, especially at the 7-nm FinFET node and beyond, these challenges are intensified by lower supply voltages, device mismatches, and leakage variations [11]. Conventional dynamic comparators exhibit offset errors and kickback noise that degrade ADC and DAC linearity and power efficiency. Therefore, a compact, low-offset comparator optimized for minimal transistor width and robust operation across process–voltage–temperature (PVT) variations is essential for PNN prototypes.

This work presents the design techniques of a dynamic comparator implemented in 7-nm FinFET technology, optimized for minimum device width and low power consumption for integration in the ADC array of a PNN system. The proposed comparator adopts the StrongARM latch architecture [12], [13] with additional inverter buffers at both outputs to equalize and stabilize output resistance, thereby improving output balance and reducing mismatch-induced decision errors. Specifically, layout techniques such as POGroup drawing, manual guard ring implementation, and design considerations for metal boundary effect (MBE), length of diffusion (LOD), and self-

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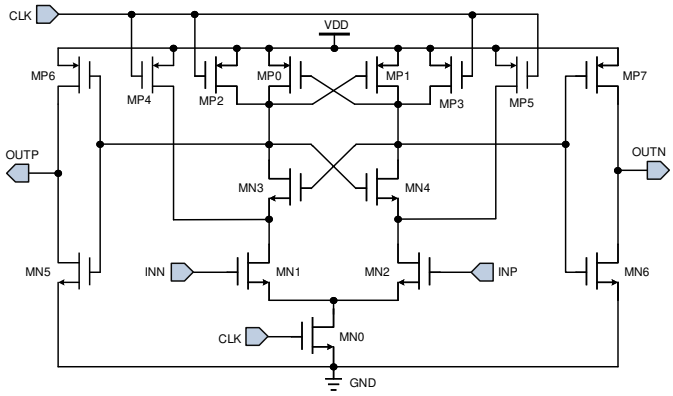

Fig. 2. The schematic of the dynamic comparator

aligned litho-etch-litho-etch (SALE2) are demonstrated to enhance matching and circuit robustness. The proposed design achieves high-speed operation and low power dissipation while maintaining a compact layout area, making it suitable for integration in high-density, low-energy photonic neural network systems.

II. Implementation of Dynamic Comparator

The proposed comparator is derived from the StrongARM latch architecture originally introduced by Kobayashi *et al.* [12] and later refined by Razavi [13]. Fig. 2 illustrates the schematic of the implemented design in 7-nm FinFET technology. The core structure preserves the differential input pair and cross-coupled regenerative latch of the classical StrongARM comparator, which provides near-zero static power consumption and rail-to-rail output swing. To further enhance stability, inverter buffers are inserted at both outputs to balance output resistance and improve signal symmetry. This modification equalizes the load conditions at the two output nodes, suppressing metastability and minimizing offset caused by device mismatch during regeneration. The comparator thus delivers consistent logic levels at 10 GHz operation.

The circuit operates in four sequential phases: precharge, amplification, regeneration, and decision. During the precharge phase, all internal nodes are reset to the supply voltage to remove any memory effect of previous states. When the clock signal rises, the differential pair converts the input voltage difference into a current imbalance that initiates the amplification phase. The cross-coupled pair then regenerates this differential signal with positive feedback until one output is driven to logic high and the other to logic low, completing the decision phase. This dynamic operation enables high-speed comparison with almost no static current path.

A. Design Optimization in 7-nm FinFET node

To meet the stringent area and speed requirements of PNN prototyping, all transistors were sized to the minimum device width permitted by the 7-nm process design kit (Process Code: TN7). Ultra-Low Threshold Voltage (ULVT) FinFETs were selected to achieve fast switching at a very low supply voltage.

TABLE I
Dimensions of the Transistors

MOS \ Dimensions	#Fin	#Finger	Width
MN0	12	4	8-nm
MN1∼2	12	2	8-nm
MN3∼4	4	2	8-nm
MN5∼6, MP0∼7	2	2	8-nm

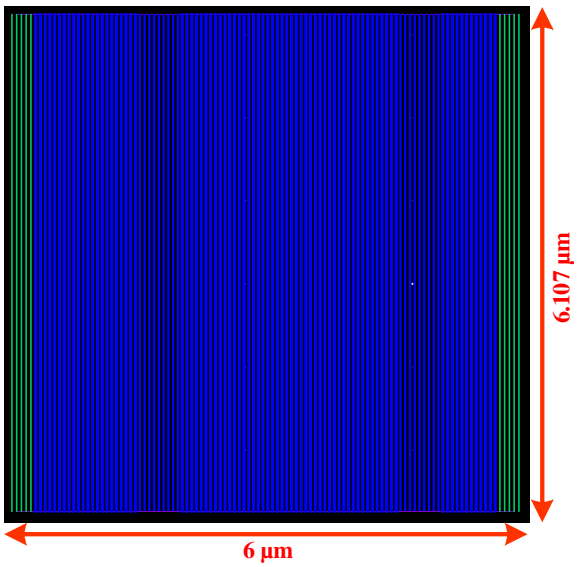

Fig. 3. Layout view illustrating POGroup merging and uniform poly distribution in the comparator core

The FinFET structure inherently provides improved matching and reduced short-channel effects, allowing aggressive scaling without significant loss of gain. Nevertheless, lower supply voltage and higher parasitic capacitances in advanced nodes necessitate careful adjustment of precharge timing and regeneration strength to ensure reliable operation at 10 GHz or above. The transistor dimensions and device parameters are summarized in Table I.

B. Layout Considerations and Process-Aware Design

Layout implementation in the 7-nm node requires strict adherence to design-rule constraints and uniformity measures to preserve circuit matching. The proposed comparator adopts a POGroup-based layout strategy, in which all closely spaced poly (PO) lines within a defined distance are merged into a single group according to the process design rule. A POGroup cell of size 36.6 μm^2 was developed as shown in Fig. 3. The shape of the POGroup is not necessarily square; it serves as the initial background structure to begin the layout flow. This grouping improves uniformity of the poly pitch, minimizes line-edge roughness, and helps automatically satisfy PO spacing constraints. Each transistor gate is defined by the poly (PO) layer, while dummy poly (DMYPO) structures are added on both sides of active devices to maintain pattern density and reduce edge-induced threshold voltage variation caused by over-undercut.

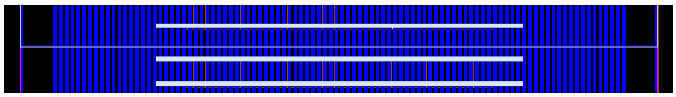

Fig. 4. Close-up view showing CPO layer cuts between N type ULVT PO and P type ULVT PO regions for VTH uniformity

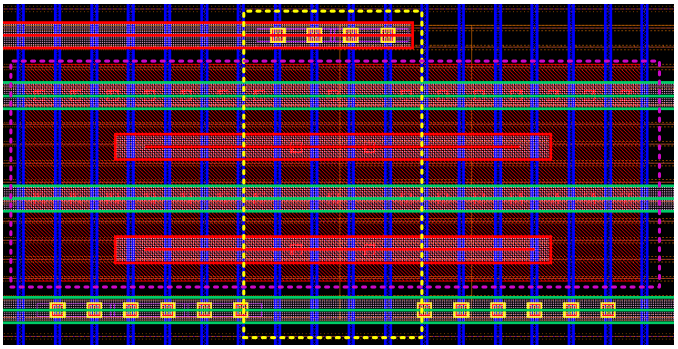

Fig. 5. Consideration of LOD effect

In addition to improving uniformity, the POGroup structure provides significant layout flexibility. The main circuit region can be moved and fitted within any POGroup shape, making the overall layout more adaptable to surrounding block geometries without violating process rules. This adjustability allows efficient floor-planning and eases the integration of analog and mixed-signal circuits within the tight constraints of the 7-nm FinFET process.

The cut-poly (CPO) layer is used to separate the N type ULVT PO (NP) and P type ULVT PO (PP) regions, preventing threshold shifts due to material abutment between the diffusion wells, as shown in Fig. 4. A guard ring (GR) is

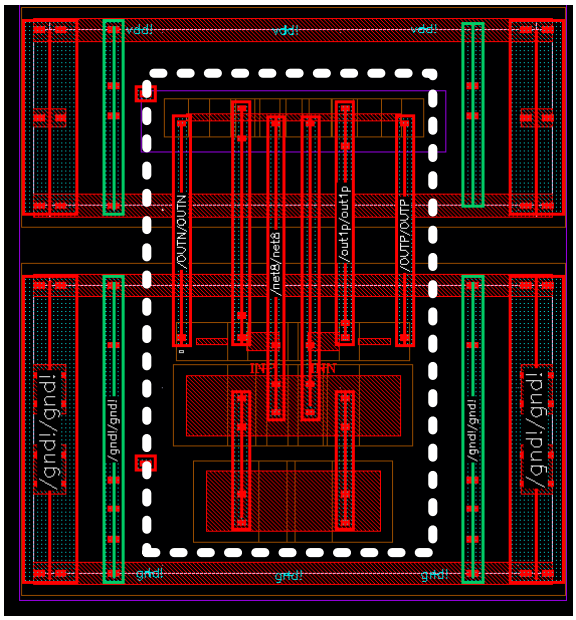

Fig. 6. SALE2 consideration in sensitive routing regions, highlighted by a white rectangular shape

TABLE II
POWER CONSUMPTION OF THE COMPARATOR

Clock Frequency	PVT Corner	Power (μW)
10 GHz	TT, VDD, 25°C	74.6
	FF, VDD+10%, 100°C	134
	SS, VDD-10%, 0°C	46.8
13 GHz	TT, VDD, 25°C	92.9
	FF, VDD+10%, 100°C	169
	SS, VDD-10%, 0°C	54.5

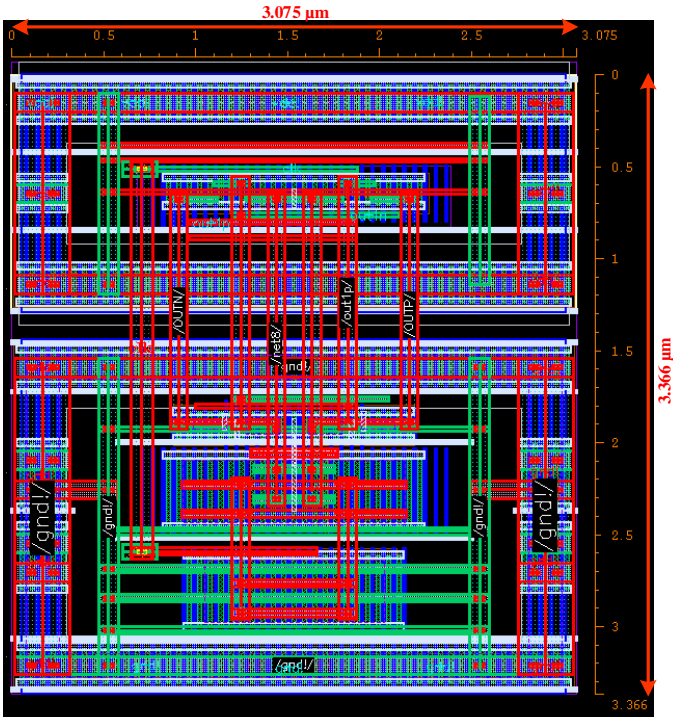

Fig. 7. Final layout-top view of the comparator showing symmetric routing

implemented around the entire comparator block to provide substrate isolation and suppress substrate noise coupling. The CPO length used for GR in this layout flow is not supported by automated tool generation; therefore, the GR structure was created manually to ensure continuity, mirror symmetry, and proper alignment with the active region.

The diffusion (OD) layer boundaries were carefully extended and enclosed by dummy diffusion cells to minimize length-of-diffusion (LOD) effects, which can introduce VTH variations near OD edges, as shown in Fig. 5. The OD considering all dummies is highlighted using pink color dotted line, and the core OD is highlighted using yellow color dotted line in Fig. 5. Additional design provisions were made to mitigate metal boundary effect (MBE) and self-aligned litho-etch-litho-etch (SALE2) process variations. MBE was reduced by inserting CPO cuts at NP/PP abutments, while SALE2 variation was minimized by using a single metal mask (mask-1) for critical interconnects to ensure consistent linewidth across the comparator, as shown in Fig. 6.

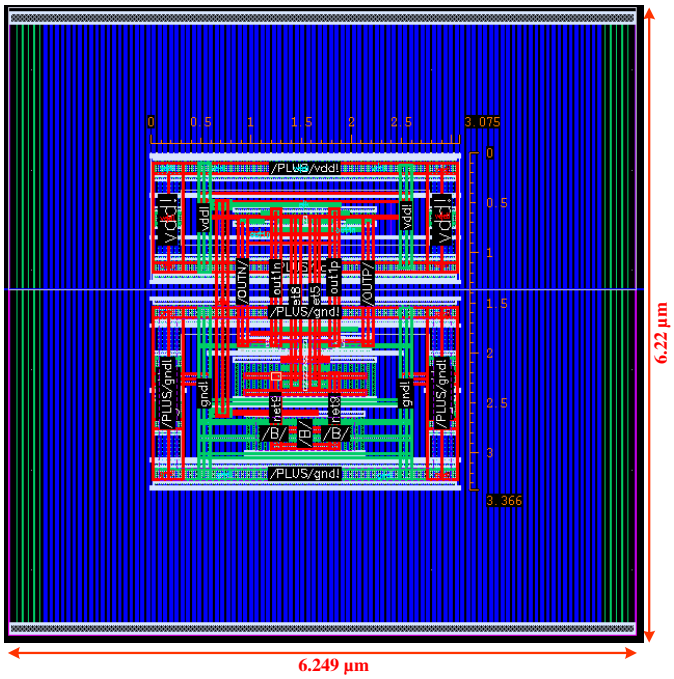

Fig. 8. Complete layout of the proposed design

III. Post-Layout Simulation Results

The proposed design is implemented using the TSMC TN7 process, with a core circuit area of 10.35 μm^2, as shown in Fig. 7. The complete layout, including the POGroup structure, is shown in Fig. 8, occupying a total area of 38.8 μm^2.

Post-layout simulations were performed at three extreme PVT corners: (TT, VDD, 25°C), (FF, VDD+10%, 100°C), and (SS, VDD-10%, 0°C). The simulation testbench used a differential input voltage defined as $V_{\text{INP}} = V_{\text{CM}} + V_o$ and $V_{\text{INN}} = V_{\text{CM}} - V_o$, where $V_{\text{CM}} = 0.4$ V and $V_o = 2.5$ mV. The average power consumption values of the proposed design at the three PVT corners are summarized in Table II. The Monte Carlo analysis plot (500 runs) for process variation is shown in Fig. 9. For a 10 GHz clock frequency, the results are shown in Fig. 10. The comparator was also simulated at frequencies up to 13 GHz, demonstrating robust high-speed operation with full output swing, as shown in Fig. 11.

IV. Conclusion

A 10-GHz comparator in 7 nm FinFET technology is presented for data converters in photonic neural network systems. The design achieves compact area and low power through minimum-width transistor sizing and POGroup-based layout. Inverter buffers improve output balance and stability, while dummy poly insertion, guard-ring isolation, and CPO layer control enhance matching and reduce variations. Post-layout simulations confirm robust full-swing operation and reliable 10 GHz decision speed across PVT corners. The results demonstrate a power-efficient and layout-scalable solution for mixed-signal PNN interfaces.

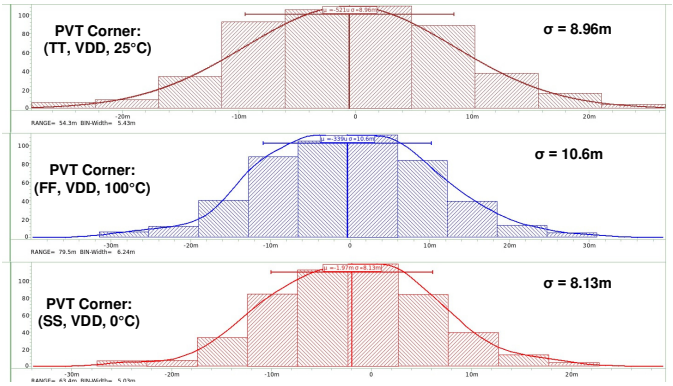

Fig. 9. Monte Carlo simulation results for process variation

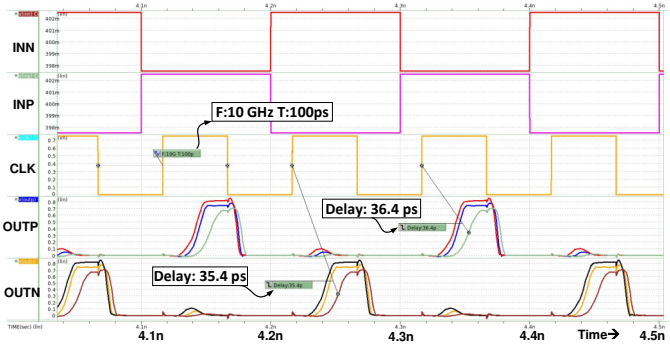

Fig. 10. Post-layout simulation results of the comparator at a 10 GHz clock frequency

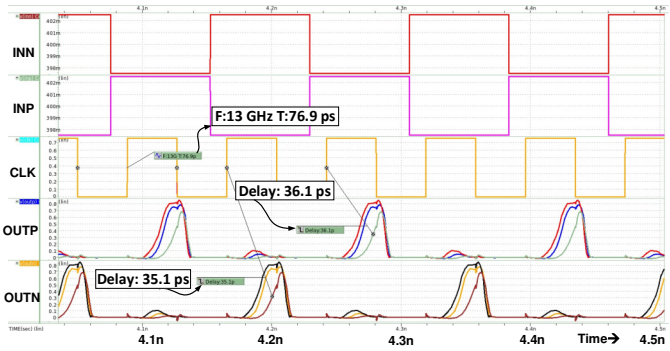

Fig. 11. Post-layout simulation results of the comparator at a 13 GHz clock frequency

Acknowledgment

The successful completion of this research was supported by the academic resources and research infrastructure provided by the Taiwan Semiconductor Research Institute, National Institutes of Applied Research. We hereby express our sincere gratitude.

This work was partially funded by National Science and Technology Council (NSTC), Taiwan, under grant NSTC 114-2923-E-110-001-, NSTC 112-2923-E-006-003-MY3, NSTC 112-2221-E-110-063-MY3 and NSTC 114-2218-E-110-009-.

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