

An All-NMOS Adaptive Active Gate Driver with Detection-Free CSIV Spike Suppression

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Abstract—This paper presents a novel SiC MOSFET gate driver designed using TSMC 0.18- μm CMOS HV technology, featuring a fully NMOS output stage with self-triggered oscillation suppression and adaptive drive currents. The Boost-Damp buffer activates only during Common Source Inductance Voltage (CSIV) spike events using intrinsic low-pass filtering, avoiding extra detection circuits. An Active Float Bridge enables safe signal transfer across multiple floating grounds, while a feedback mechanism dynamically adjusts the drive current during switching, including the Miller plateau. Post-layout simulations show 28.9 ns rise time, 20.5 ns fall time, 138 mW power @ 500 kHz, 983 $\mu\text{m} \times 1678 \mu\text{m}$ overall chip area, and a core area of 678.31 $\mu\text{m} \times 1451.9 \mu\text{m}$, making it compact and efficient for high-speed SiC applications.

Index Terms—Gate driver, SiC MOSFET, Boost-Damp buffer, Active Float Bridge, floating grounds, drive current, CSIV Spike

I. INTRODUCTION

Traditional power discrete gate drivers typically use an open-loop control with bulky passive components, lacking active feedback and the ability to adapt to voltage and temperature variations [1]. While some active gate drivers (AGDs) integrate a feedback through external programmable devices (e.g., FPGAs, microcontrollers), this approach increases system size, cost, and power consumption, and requires reprogramming for different power devices [2], [3]. On-chip AGDs have been proposed to resolve these issues, but many suffer from high power consumption, poor noise immunity, or simplistic Miller detection schemes [4], [5]. An AGD design using Differential Timing-Based Miller Detection (DTMD) improves accuracy and reduces level shifter losses via power gating, but still exhibits large rise/fall times [6]. Another AGD designed using digital multi-level power gating circuit suffers with high power consumption, and large rise/fall times [7].

This work presents a novel gate driver architecture for SiC MOSFETs that features a fully NMOS-based output buffer combined with a self-triggered oscillation suppression mechanism and adaptive driving current control. Unlike conventional PMOS-NMOS designs, the proposed all-NMOS structure enhances switching speed and efficiency while leveraging a Boost-Damp (B-D) source buffer that activates only during Common Source Inductance Voltage (CSIV) spike events without requiring external detection circuitry.

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II. ALL-NMOS ADAPTIVE ACTIVE GATE DRIVER

Fig. 1 illustrates the All-NMOS adaptive active gate driver for SiC MOSFETs that incorporates an adaptive, fully NMOS-based output buffer architecture. It is specifically developed to address challenges such as parasitic oscillations, particularly CSIV spikes, and to improve switching performance and efficiency in high-speed power electronics applications. The Output Stage consists of a Main Source Buffer and a Sink Buffer. The Main Source Buffer initiates the turn-on operation, while the Sink Buffer handles the turn-off. To suppress parasitic oscillations that occur during fast switching, especially at the gate-source node of the SiC MOSFET, a Boost-Damp (B-D) Source Buffer with a control circuit is introduced. The B-D Source Buffer shares the same output node as the Main Source Buffer, but it is connected via a different low-pass filter path with lower impedance. This difference in impedance allows the circuit to detect high-frequency spikes without additional detection circuits. Control of these buffers is managed through several specialized sub-circuits, like the Main source buffer control, the Sink buffer control, and the Active float bridge. This architecture also includes several pre-existing circuits such as the Split-path circuit and Delay match [8]–[10].

A. Main source buffer control

The Main source buffer control circuit is shown in Fig. 2. It plays a crucial role in managing the safe and reliable activation and deactivation of the Main Source Buffer in the proposed gate driver. Since the output stage operates under a floating ground potential (V_{ss1}), the control circuit must accurately process input signals and generate logic levels that can toggle the buffer without signal corruption or device stress.

The circuit primarily operates by detecting the positive and negative edges of the input control signals sig_src_plus and sig_src_minus , respectively. When sig_src_plus transitions positively, it generates a short pulse through capacitive coupling, which is rectified by diodes $D_{\text{plus_pos}}$ and $D_{\text{plus_neg}}$. This pulse activates transistor M1, discharging the node V_r to a low logic level. As a result, transistor M3 turns ON, raising node V_s and setting the SR-latch1. This action activates the Main Source Buffer, allowing it to source current to the gate of the SiC MOSFET during the turn-on phase.

Conversely, when sig_src_minus transitions negatively, it also generates a pulse that is rectified through $D_{\text{minus_pos}}$ and $D_{\text{minus_neg}}$. This triggers M2, charging node V_r to a

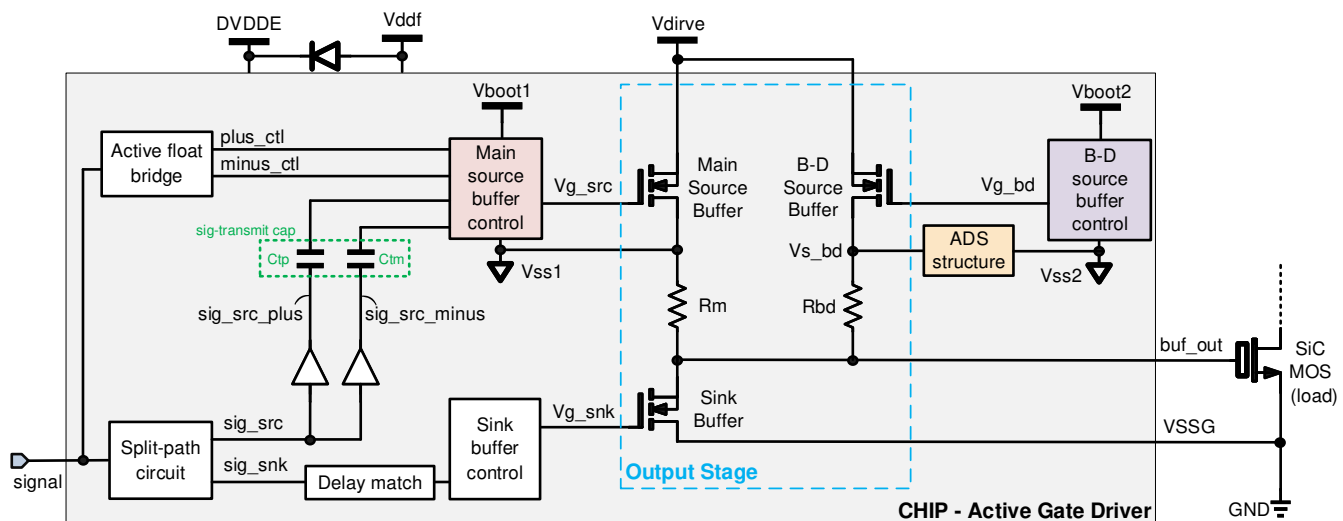


Fig. 1. Proposed Active Gate Driver architecture

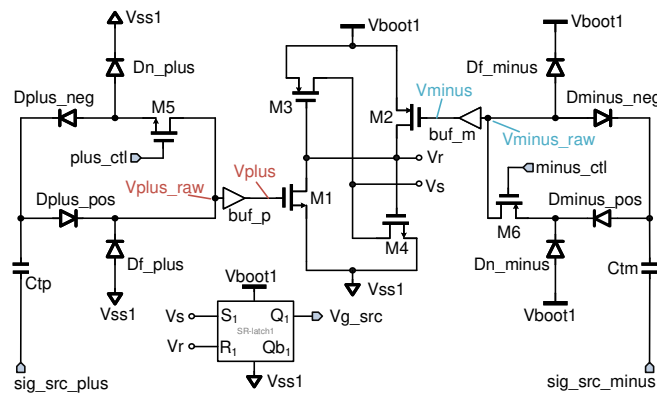


Fig. 2. Schematic of Main source buffer control

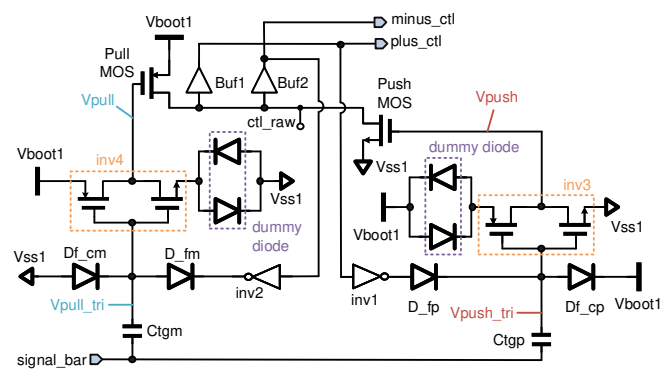


Fig. 3. Schematic of Active float bridge

high logic level and turning ON transistor M4, which pulls Vs low. The SR-latch1 is reset in this phase, thereby turning OFF the Main Source Buffer and handing over control to the Sink Buffer for the device turn-off operation.

The circuit also incorporates mechanisms to manage voltage level transitions associated with the floating ground system (Vss1). During the rise of system voltages, the following diodes, Df_plus and Df_minus, ensure that intermediate control voltages (Vplus_raw and Vminus_raw) track the floating ground, thereby preventing over-voltage stress on sensitive components. Similarly, during falling transitions, the draining diodes, Dn_plus and Dn_minus, safely discharge any trapped charge that could otherwise falsely trigger the control logic.

B. Active float bridge

The Active float bridge circuit ensures safe and complete transmission of control signals between the gate driver's logic domain and its floating output stages, which operate at different ground potentials (i.e., V_{ss1} , V_{ss2} , and V_{SSG}). In this design, it is responsible for presetting and delivering the

plus_ctl and minus_ctl signals to the Main source buffer control without distortion or damage, even when large common-mode voltage changes occur during high-speed switching.

The schematic of Active float bridge is shown in Fig. 3, it uses a push-pull structure consisting of Push MOS and Pull MOS devices, driven through intermediate inverters and charge-transfer capacitors (Ctgp, Ctg_m), to quickly force control nodes in the floating domain to the desired logic levels. Feedback diodes (D_{fp}, D_{fm}) prevent false activation during reset phases, while following diodes (D_{fcp}, D_{fcm}) ensure that internal voltages track the floating system's potential, avoiding over-voltage stress. Dummy diodes are included for device matching and symmetry.

C. B-D source buffer control with Adaptive drive strength (ADS) structure

The Boost-Damp (B-D) buffer control circuit manages the activation of the B-D Source Buffer, which is designed to suppress CSIV spike oscillations during SiC MOSFET turn-on. Instead of using a dedicated sensing circuit, it detects oscillations indirectly by exploiting the difference in frequency

TABLE I
PERFORMANCE COMPARISON

	[3]	[4]	[9]	[11]	This work
Year	2022	2023	2024	2024	2025
Publication	ISPSD	MWSCAS	APCCAS	ISOC	ISCAS
Technology (nm)	180 BCD + FPGA	T18HVG2 (180)	T18HVG2 (180)	T18HVG2 (180)	T18HVG2 (180)
Driver type	Active	Active	Active	Active	Active
Verification	Meas.	Post Sim.	Post Sim.	Post Sim.	Post Sim.
VDD (V)	1.8, 3.3 & 20	12	5 & 10	5 & 10	5 & 12
f_{V_PWM} (MHz)	0.1	0.5	0.5	0.5	0.5
t_{rise} (ns)	N.A.	153 at 12 V	28.4 at 10 V	261 at 10 V	28.9 at 12 V
t_{fall} (ns)	N.A.	187 at 12 V	36.1 at 10 V	234 at 10 V	20.5 at 12 V
Chip area (mm ²)	6.25	16.3443	5.523	5.145	1.649
P_{dis_total}	79.51 mW*	32.7 W	210 mW	167 mW	138 mW

*Power consumption of FPGA is excluded

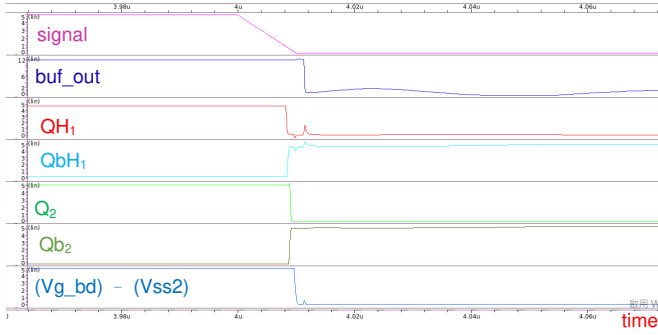


Fig. 8. B-D source buffer control working during the falling edge

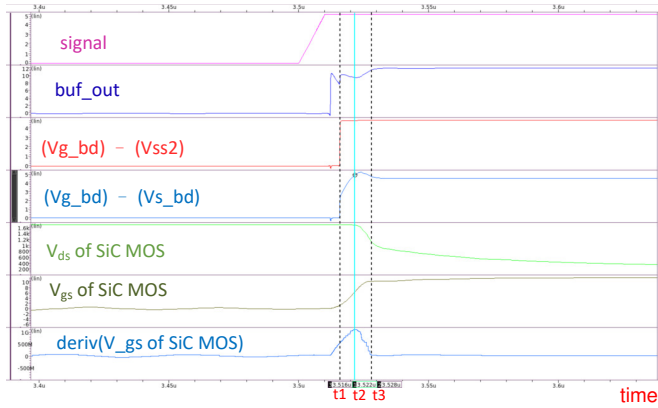


Fig. 9. Adaptive drive strength optimization

detects the turn-on command, sets the latch without false triggering, and drives the output through the floating domain. Fig. 8 illustrates the turn-off operation of the B-D source buffer control. The CSIV-induced voltage difference between V_{g_bd} and V_{ss2} triggers the control latches, enabling the B-D buffer to inject compensating current and suppress output ringing during the turn-off transition. The ADS mechanism in Fig. 9 demonstrates attenuation during high di/dt during the interval (t_1 - t_2) to avoid overshoot and enhancement during the Miller plateau (t_2 - t_3) to accelerate switching while maintaining stability, respectively.

With supply voltages of $V_{drive} = 12$ V, $DVVDE = 5$ V and $V_{ddf} = 5$ V, the AGD demonstrates a rise time of 28.9 ns, a fall time of 20.5 ns, a rise delay of 40.2 ns, a fall delay of 30.2 ns, and a power consumption of 138 mW at 500 kHz as the worst-case conditions in all-PVT-corner simulations. The comparison of the prior works for power transistor drivers is summarized in Table I. It might appear that a lower power consumption of 79.51 mW was reported in [3]. Notably, they exclude FPGA power, which can be in the order of several watts. Hence, it implies that the combined power consumption of [3] (79.51 mW + FPGA P_{dis}) is much higher than the total power consumption of the proposed AGD (138 mW). Additionally, Table I shows that our core area (1.649 mm²) is 73.6%, 89.9%, 70.1% and 67.9% smaller than [3], [4], [9] and [11], respectively, with no off-chip FPGA or external logic required.

IV. CONCLUSION

The proposed gate driver employs a fully NMOS-based output stage combined with a self-triggered Boost-Damp (B-D) buffer and adaptive drive strength control to deliver high-speed, low-noise switching for SiC MOSFET applications. The design leverages the natural low-pass filtering between the Main and B-D buffer paths to detect and suppress CSIV-induced oscillations without dedicated sensing circuits, while the Active Float Bridge ensures reliable signal transfer across multiple floating grounds. Post-layout simulations validate the control logic, floating interface, and adaptive B-D operation, demonstrating robust performance across all extreme PVT corners. This architecture offers an efficient, compact, and robust solution for next-generation high-speed SiC gate driving with effective EMI mitigation and enhanced switching stability.

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