A Multi-band Resilient PLL-Based Clock Generator with State-Aware Debounce Control and DAC-assisted Biasing for Trustworthy AI Systems

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***Abstract*—This paper presents a multi-band resilient PLL-based clock generator, addresses the demand for stable, low-jitter, and stable timing generation in dynamic environments. Reliable clocking is very much needed in such systems to secure deterministic behavior and maintain system integrity. The proposed architecture includes a State-Aware Debounce control that quantifies frequency band switching conditions and eliminates unnecessary transitions, and thus enhancing stability during dynamic operation. A binary weighted current DAC is used for frequency control, and an extra high frequency current bank is added to compensate for non-uniform VCO gain (K_{VCO}) over 32 frequency bands, enhancing gain consistency at higher frequencies. Furthermore, a DAC-assisted biasing allows for adaptive operating-point tuning across process, voltage, and temperature fluctuations, which improves overall loop robustness. Implemented in 16-nm FinFET CMOS process, the proposed design exhibits 0.583-ps RMS jitter and consumes 3.52 mW of power, indicating its applicability for high-performance, low-power, and dependable clock generation in trustworthy AI hardware.**

***Index Terms*—Multi-band PLL, Resilient clock generator, Low-jitter timing, State-aware debounce control, DAC-assisted biasing.**

I. Introduction

AI systems require reliable and stable hardware execution, regardless of dynamic workloads, making it crucial in modern AI hardware implementations [1]. In fact, AI accelerators based on systolic array architectures are made up of massively parallel processing units that ought to be synchronized across several cores to provide efficient and deterministic computing [2]. Adaptive clocking have been widely looked into to maintain timing coordination, enables quick frequency modification and better efficiency in response to dynamic AI workloads [3]. However, typical PLL-based clock generator continue to be highly susceptible to process, voltage, and temperature (PVT) fluctuations, especially when performing multi-band operation, resulting in deteriorated stability, increased phase noise, and potential loss of lock [4]. As a result, developing durable and power efficient resilient clock generators has become a major task for reliable AI systems. These problems highlight the necessity for resilient clock systems capable of maintaining predictable performance despite aggressive scaling and highly varied operational environments.

For example, inductor-less PLLs were tailored to meet area efficiency, but they caused high power consumption and phase noise [5]. While, ring oscillator based voltage controlled oscillators (VCOs) in PLLs remain susceptible to supply and substrate noise variations in FinFET based designs [6], besides near threshold feedback loops struggle with current mismatch and PVT variations [7]. Though sub-sampling PLLs (SS-PLLs) are particularly effective in minimizing in-band noise, but switching between needed frequencies is susceptible to limited capture ranges and glitches [8].

The digital PLL opt to mitigate the non-linearity of digital controlled oscillators requires complex logic circuit for calibration and exhibits high power consumption [9]. A fractional-N PLL results in latency that often needs precise timing and gating alignment, though its sensitivity to calibration predominantly needs LMS-based tuning to suppress spurs caused by phase mismatch [10]. A mixed-signal based PLL with digitally assisted calibration and switched-capacitor sampling phase detectors has shown enhanced PVT resilience, diminished reference spur, and minimal integrated jitter across an operating range [11]. Beyond design and implementation issues, one of the significant oversights resides in how clock generators adapt to environmental stress, especially single-event upsets (SEUs) [12].

The proposed design overcomes these gaps by presenting a multi-band robust PLL-based clock generator with state-aware debounce control and Digital to analog converter (DAC) assisted biasing. The proposed design aims to enable reliable clock generator while maintaining spectral purity and lock stability over a 32 frequency bands with uniform incremental band frequency. With the help of State-Aware Debounce logic utilized to minimize transient disturbances and DAC-assisted biasing for improving the linearity of voltage controlled oscillator (VCO), the proposed design creates a safe and high-precision clocking framework for next-generation AI technology. Furthermore, it improves robustness against change in supply changes, making it ideal for AI trustworthy systems.

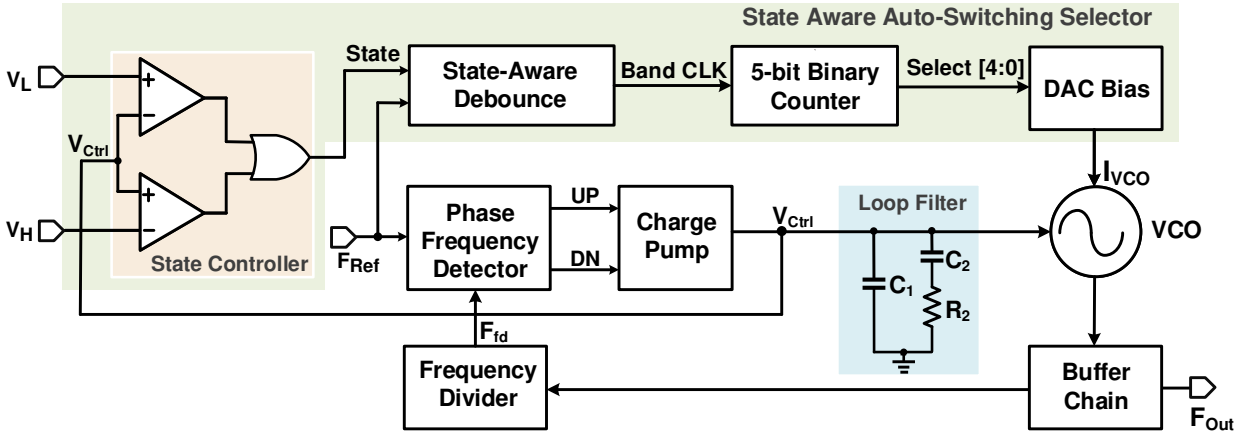


Fig. 1. Block diagram of the proposed PLL with state-aware auto-switching selector

II. System architecture

The proposed architecture is based on a phase-locked loop (PLL) structure with an additional state-aware auto-switching selector, as shown in Fig. 1. The main PLL loop includes the phase frequency detector (PFD), charge pump (CP), voltage controlled oscillator (VCO), buffer chain, and frequency divider.

The phase frequency detector (PFD) compares the reference input clock F_{Ref} to the feedback clock F_{fd} generated by the divider. Based on the phase and frequency difference, PFD generates UP and DN signals that operate the charge pump (CP). The CP converts these signals into currents, which charges or discharges the loop filter and produce the control voltage V_{Ctrl}, controls the oscillation frequency of the VCO. The VCO output is routed through a buffer chain to increase signal quality and stability. The buffered signal is then split by the frequency divider to produce the feedback clock F_{fd}, which is fed back into the PFD, resulting in a closed-loop system.

In addition to the traditional PLL, the system features a state-aware auto-switching selector for different 32-band operations. This module dynamically adjusts the VCO bias (I_{VCO}) over several frequency bands by continuously monitoring the control voltage (V_{Ctrl}) and making deterministic state decisions.

The proposed state-aware auto-switching selector operates as follows:

- The State Controller continuously monitors the control voltage V_{Ctrl}.
- Based on predefined thresholds V_L and V_H, the state controller determines its operating state:
  - If $V_L < V_{Ctrl} < V_H$, considered as an *in band state*.
  - If $V_{Ctrl} > V_H$ or $V_{Ctrl} < V_L$, considered as an *out of band state*.
- The detected State is passed to a State-Aware Debounce logic, which evaluates the validity of transitions and ensures stable state decisions by rejecting spurious glitches.
- The debounce logic samples the state using the reference clock F_{Ref} and checks for a specific transition sequence:
  1) First sample: *in band state*
  2) Second sample: *out of band state*
  3) Third sample: *out of band state*
- The condition is evaluated based on the sampled sequence to confirm a valid state transition.
- If the condition is satisfied, a Band CLK '1' is generated, drives the 5-bit up/down counter.
  - If a Band CLK '1' is received, the digital band code (Select[4:0]) is incremented.
  - If a Band CLK '0' is received, the digital band code (Select[4:0]) remains unchanged.
- The 5-bit up/down counter outputs the updated Select[4:0] code to a DAC bias.
- The DAC bias, converts the Select[4:0] into corresponding analog current levels (I_{VCO}), which are supplied to the VCO for bias adjustment.
- The VCO controls its oscillation frequency to ensure that the PLL stays stable across different operating zones.

When the predefined conditions are met, the selector automatically shifts frequency bands, allowing the PLL to operate over many frequency ranges while remaining stable, dependable, and unaffected. Consequently, the State-Aware Auto-Switching Selector provides a dependable digital control path for adaptive frequency-band switching and thus improves lock resilience and reduces noise-induced erroneous transitions.

A. State-Aware Debounce logic

The State-Aware Debounce logic, shown in the Fig. 2, receives the State signal from the State Controller and is also triggered by F_{Ref}. It consists of three cascaded D flip-flops that suppress transient fluctuations and maintain the temporal stability of the input state. The circuit generates the band clock (Band CLK) to trigger the subsequent band selection logic after ensuring that the system remains in the required condition throughout several clock cycles. The debounce logic effectively prevents excessive band switching induced by transient disturbances.

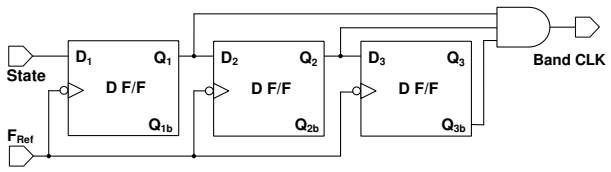


Fig. 2. Schematic of the State-aware debounce logic

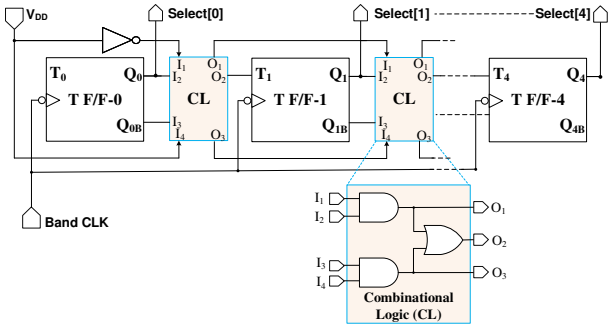


Fig. 3. Schematic of a 5-bit binary counter

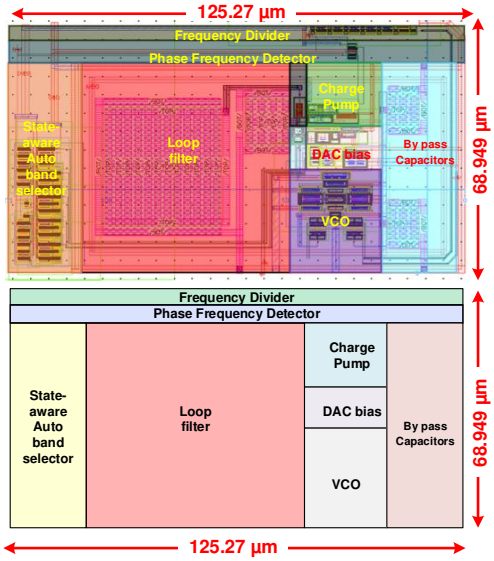


Fig. 4. Layout and floor plan of the proposed PLL

B. A 5-bit binary counter

The 5-bit binary counter in Fig. 3 is synchronous and controlled by the Band CLK signal from the State-Aware Debounce circuit. The counter output, Select[4:0], represents one of 32 frequency bands and has direct control over the DAC biasing network. Each increment of Select[4:0] increases the output frequency F_{Out}, ensuring a consistent frequency progression across the tuning range. The counter only updates its status when Band CLK is set to logic '1', allowing the band code to proceed consecutively. When Band CLK is set to logic '0', the current value of Select[4:0] is retained, ensuring stable operation during inactive times.

Furthermore, the counter output, Select[4:0] has cyclic (wrap-around) behavior, switching from 11111 to 00000 when it reaches its maximum count. This enables continuous traversal throughout all frequency bands, allowing the system to finally reach the required target band even if it is briefly skipped during operation. As a result, the suggested design maintains robust operation and ensures eventual convergence without requiring additional control signals.

C. The DAC bias

The proposed design employs a binary-weighted current DAC to control frequency and band selection in the PLL, since the proposed PLL runs across 32 frequency bands. An additional high frequency current bank is included to compensate for Voltage controlled oscillator (VCO) gain (K_{VCO}) between bands. The VCO control current (I_{VCO}) generated by the DAC bias compensates for the reduced VCO sensitivity at higher frequencies, thereby maintaining a constant gain K_{VCO}. The DAC-assisted biasing network continually changes the I_{VCO}, resulting in a more linear relationship between control voltage (V_{Ctrl}) and output frequency (F_{Out}).

The VCO control current is given by DAC bias is:

$$I_{VCO} = I_b - I_{band} + I_{Cal} \tag{1}$$

where I_b represents nominal DAC bias level and I_{base} is the band-selection current given by

$$I_{band} = I_{S[4]}.S[4] + I_{S[3]}.S[3] - I_{S[2]}.S[2] - I_{S[1]}.S[1] - I_{S[0]}.S[0] \tag{2}$$

where $I_{S[i]}$ represents the weighted current contribution associated with each digital control bit, and S[4:0] is the 5-bit digital band selection code (Select[4:0]), which determines the required VCO bias current (I_{VCO}) for frequency tuning, allowing for accurate and linear control throughout all 32-bands.

The calibration current is expressed as

$$I_{Cal} = I_c - I_{S[3]}.S[3] - I_{S[2]}.S[2] - I_{S[1]}.S[1] - I_{S[0]}.S[0] \tag{3}$$

Here, I_c is the base calibration current.

III. Post-Layout Simulations

Fig. 4 depicts the floorplan and layout of the proposed PLL with a core area of $125.27\,\mu\text{m} \times 68.95\,\mu\text{m}$ (about $0.00864\,\text{mm}^2$). The layout is organized to minimize routing parasitics and connections between analog and digital blocks. The frequency divider and phase-frequency detector (PFD) are positioned at the top for direct feedback routing. The loop filter is centrally arranged, while the VCO is adjacent to the charge pump and DAC bias circuits, reducing sensitive node parasitics. The state-aware band selection is segregated to minimize digital noise coupling. Bypass capacitors near the VCO improve supply stability and ensure reliable PLL operation.

Fig. 5 depicts the post-layout band switching waveform of the proposed PLL. Firstly, F_{Out} operates at 7.83 GHz, which corresponds to Band 31. As the select signals shift consecutively, the PLL transitions to Band 30 and settles at 8.10 GHz,

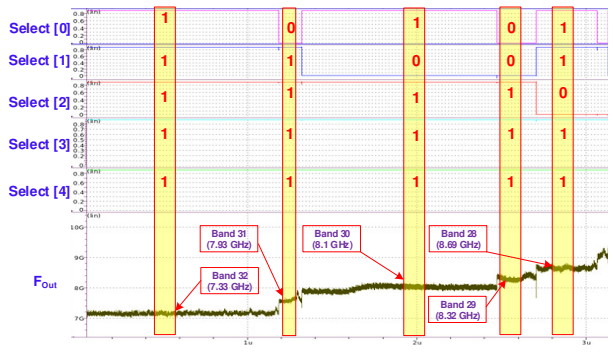


Fig. 5. Post layout simulation results of band switching

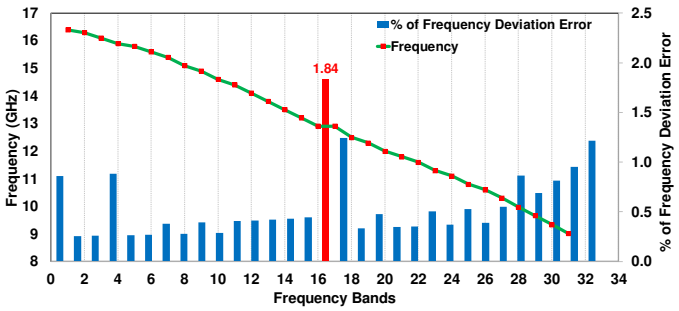


Fig. 6. Post layout simulation results of 32 frequency bands and percentage of frequency deviation error at TT (Typical–Typical, 0.9 V, 25°C) corner

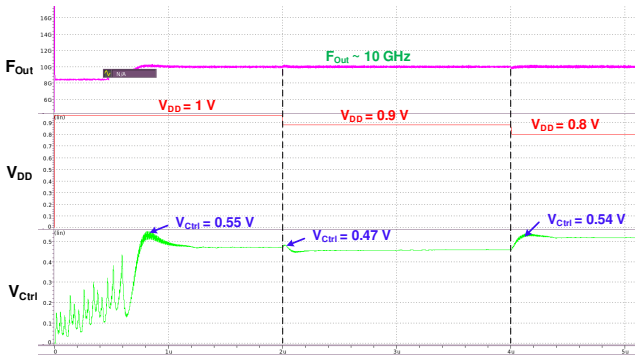


Fig. 7. Supply voltage (V_{DD}) variation of the proposed PLL at TT (Typical–Typical, 25°C) corner

then to Band 29 at 8.23 GHz, and lastly to Band 28 at 8.60 GHz. Each transition demonstrates consistent settling behavior and smooth frequency transfer across adjacent bands with almost equal increments from one band to another band. The waveform confirms that the band selection signals (Select[4:0]) and output frequency response are properly synchronized during dynamic band changes.

In Fig. 6, the post-layout simulation results at the TT (Typical–Typical, 0.9 V, 25°C) corner demonstrate a 32-band multi-band tuning characteristic with a monotonic frequency decline indicates full coverage across all bands. The band spacing is evenly distributed, showing adequate coarse tuning resolution. Most bands have a low frequency deviation error (<0.5-1%), indicating accuracy and correctness. A high inaccuracy

TABLE I
PERFORMANCE COMPARISON WITH PRIOR WORKS

Parameters	**[11]**	**[5]**	**[12]**	**[7]**	**This work**
Year	2023	2024	2025	2026	2026
Technology (nm)	4	22	16	16	16
Results	Meas.	Meas.	Meas.	Sim.	Sim.
F_{Ref} (MHz)	76.8	80–200	259	250	117–171
F_{Out} (GHz)	4	2.4	19.5	4	∼ (7.8–16.4)
Jitter (ps)	0.44	1.274	0.02	4.45	**0.583**
Power (mW)	4.34	8	36.5	0.072	**3.52**
FoM_{jitter} (dB)	-240.8	-229	-251.16	-238.459	**-239.2**
$FoM_{jitter\text{-}N\text{-}Area}$ (dB)	-270.97	-261	-271.8	-272.433	**-277.85**
Area (mm^2)	0.36	0.025	0.065	0.0064	**0.00864**

of roughly 1.84% is recorded between frequency bands 16 and 17, most likely due to parasitic effects. The State-Aware Debounce logic ensures stable tuning by filtering band update decisions based on consistent state transitions over consecutive cycles. This eliminates false switching caused by transient fluctuations and increases resilience during band selection.

Furthermore, under TT (Typical–Typical, 25°C) corner operation with variable supply voltage V_{DD}, the proposed PLL maintains stable operation. Fig. 7 shows that even with stepped supply voltage, the output frequency remains constant (10 GHz), indicating superior robustness against supply variations. The control voltage (V_{Ctrl}) settles quickly without any sustained oscillations. Table I presents a comparison of proposed multi-band PLL-based clock generator with the prior works, achieves 0.583 ps RMS jitter while consuming 3.52 mW. The proposed design attains the highest $FoM_{jitter\text{-}N\text{-}Area}$ (-277.85 dB) while occupying a minimal area of $0.00864\,mm^2$.

IV. CONCLUSION

This paper presents a reliable multi-band PLL design for accurate and steady timing for Trustworthy AI systems. The State-Aware Debounce control provides operation over 32 bands throughout a broad frequency spectrum of approximately 7.8-16.4 GHz, with each band separated by nearly equal frequency increments while eliminating redundant switching. The proposed design achieves low power consumption through efficient DAC management and enhanced biasing while also delivering stable operation with improved VCO linearity. The design implemented in 16 nm FinFET CMOS process, achieves a balance of timing accuracy and power efficiency. The findings demonstrate that the proposed PLL is a durable and effective design, offering reliable wide band frequency range suitable for Trustworthy AI systems.

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