Performance-Driven Multi-Objective Evolutionary Optimization of CMOS OTA Design

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***Abstract*—This study presents a new closed-loop performance-driven framework that combines Cadence circuit level modeling with MATLAB-based Multi Objective Genetic Algorithm (MOGA) optimization for the automated design of operational transconductance amplifiers (OTAs). As MOGA can produce a well-distributed Pareto front while navigating high-dimensional design spaces and preserving trade-off information, it is widely used. To improve optimization performance, the framework uses elitism, blended crossover, annealed mutation, and an adaptive fitness function with weighted penalties. MATLAB-based optimization results, which demonstrate fitness declining from 2.847 to 0.324 and hyper volume growing from 0.214 to 0.873 over 100 iterations, validate convergence and variety. Critical metrics, such as DC gain (126.01 dB), UGB (370.98 MHz), phase margin (157.92°), slew rate (0.145 V/µs), and power (101.69 µW), are confirmed to satisfy the desired criteria through validation using Cadence EDA tools. The proposed approach enables Pareto-optimal, specification-compliant, and scalable OTA implementation suitable for automated design.**

***Index Terms*—Pareto front, adaptive fitness function, optimization, and Multi-Objective Genetic Algorithm (MOGA).**

I. Introduction

The increasing complexity of modern CMOS technology and the requirement to meet several frequently incompatible design requirements have made the design of high-performance analog circuits more challenging [1]. The operational transconductance amplifier (OTA) is a common analog building block used in biomedical systems, filters, and data converters. Careful trade-offs between important factors, such as gain, bandwidth, power consumption, noise, and linearity, which are intrinsically interrelated, are necessary to achieve the best OTA performance. Conventional analog design approaches, which use circuit simulators, mainly rely on iterative trial-and-error and designer experience.

The fact that traditional methods, while correct, are time-consuming and offer little insight into multidimensional trade-off spaces, increasing the gap between acceptable design time and design accuracy, highlights the need for automated optimization strategies [2]. Performance-driven design techniques have become an efficient way to automate analog circuit optimization by merging circuit simulators with optimization algorithms [3]. This allows for the rapid exploration of huge, complicated design spaces while maintaining SPICE-level accuracy.

For convex and well-behaved problems, standard methods of optimization such as gradient-based methods, sequential quadratic programming, and heuristic single-objective approaches [4] are effective; however, in highly nonlinear, multimodal analog design spaces, they frequently suffer from premature convergence, sensitivity to initial conditions, and limited scalability [5]. Moreover, many traditional approaches rely on simplified objective functions, which confuse trade-off relationships and limit designers to certain operating points.

On the other hand, population-based and evolutionary optimization techniques like Genetic Algorithms (GA), Differential Evolution (DE) with the static penalty function are more resilient to non-convexity and parameter coupling [6], [7]. Multi-Objective Genetic Algorithms (MOGAs) are the most efficient of these, producing a variety of Pareto-optimal solutions that let designers choose the best operating point [8]. The MOGA-SPICE framework effectively balances OTA trade-offs among gain, bandwidth, phase margin, power, and slew rate by evaluating conflicting goals [9].

This paper presents a performance-driven multi-objective evolutionary optimization approach for CMOS OTA design. By effectively exploring high-dimensional design spaces with MATLAB-based MOGA optimization, the technique generates a well-distributed Pareto front. Cadence circuit-level simulations are used to validate the results. An adaptive fitness function with weighted penalties, elitism, blend crossover, and annealed mutation further improves optimization performance to ensure both fast convergence and a range of solutions.

II. Problem Description

Referring to Fig. 1, a typical two-stage operational transconductance amplifier (OTA) design in [10] is presented as a constrained multi-objective optimization problem and comprises two cascaded stages to achieve high gain. The objective is to determine the optimal transistor sizes and bias currents that meet the predetermined target requirements within the feasible design space shown in Table I. According to Eqn. (1), certain design variables, such as transistor widths and bias currents, have a significant impact on circuit performance.

$$\mathrm{X} = [\mathrm{W}_1, \mathrm{W}_3, \mathrm{W}_5, \mathrm{W}_7, \mathrm{W}_9, \mathrm{I}_1, \mathrm{I}_2]^{\mathrm{T}} \in \mathrm{R}^7 \tag{1}$$

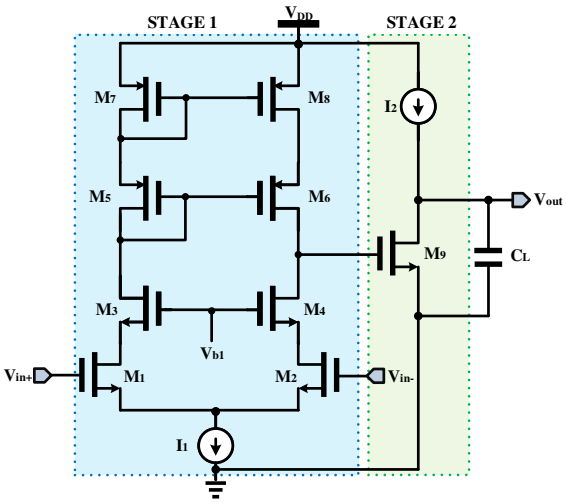


Fig. 1: High-Performance Two-Stage OTA [10]

TABLE I: Target OTA Performance Specifications

OTA Performance Metric	Constraint(X)
DC Gain (dB)	≥ 120
UGB (MHz)	≥ 372
$f_{3\text{dB}}$ (kHz)	44.89
Phase Margin (°)	≥ 60
Slew Rate (V/μs)	≥ 0.1
CMRR (dB)	≥ 140
PSRR (dB)	≥ 45
Power (μW)	≤ 102

An actual value design vector of seven elements is described by R^7, where I_1 and I_2 stand for the primary bias currents, and W_i indicates the widths of the MOSFETs (M_1, M_3, M_5, M_7 and M_9). The performance of the two-stage amplifier are determined by these design parameters, directly affect the transconductance (g_m), output resistance (r_o), parasitic capacitance, and bias levels. On fabrication limitations and specification requirements further limit the design space as shown in Eqn. (2).

$$\mathrm{X} \in \mathcal{X}, \quad \mathbf{lb} \leq \mathrm{X} \leq \mathbf{ub} \tag{2}$$

where the feasible region defined by the lower bound (lb), upper bound (ub) of the design variables represented by $\mathcal{X}$. Eqn. (3) defines the resulting circuit performance measures.

$$\mathbf{P}_{\text{target}} = \begin{bmatrix} \mathrm{G(X)} \\ \mathrm{UGB(X)} \\ \mathrm{f_{3dB}(X)} \\ \mathrm{PM(X)} \\ \mathrm{SR(X)} \\ \mathrm{CMRR(X)} \\ \mathrm{PSRR(X)} \\ \mathrm{P_{dc}(X)} \end{bmatrix} \in \mathrm{R}^8 \tag{3}$$

The DC gain is represented by G(·), the unity-gain bandwidth by UGB(·), the -3dB bandwidth by $f_{3\text{dB}}(\cdot)$, the phase margin by PM(·), the slew rate by SR(·), the common-mode rejection ratio by CMRR(·), the power-supply rejection ratio by PSRR(·), and the static power consumption by $P_{dc}(\cdot)$. In this case, the design vector with eight real-valued parameters is represented as R^8. Given the target specification vector $\mathbf{P}_{\text{target}}$ in Table I, the optimization problem is formulated as :

$$\min_{\mathrm{X}} \ \text{Objective (X)} = \sum_{\mathrm{i}=1}^{8} \mathrm{W_i} \left| \frac{\mathbf{P}_{\text{sim,i}}(\mathrm{X}) - \mathbf{P}_{\text{target,i}}}{\Delta_{\mathrm{i}}} \right| \tag{4}$$

$$\mathbf{P}_{\text{sim}}(\mathrm{X}) \approx \mathbf{P}_{\text{target}}, \quad \mathrm{X} \in \mathcal{X} \tag{5}$$

According to Eqn. (4), the optimization can be expressed as the minimization of the normalized divergence between the simulated and target performance metrics, and Eqn. (5) defines the related constraints. While the normalization terms Δ_i provide a fair contribution from measurements with varying scales, the weighted factors W_i are adaptively changed to meet the desired constraints as shown in Table I. There is no ideal method because the performance goals of OTA, such as gain against bandwidth and power usage versus stability, are intrinsically incompatible. Thus, a Pareto-optimal collection of non-dominated solutions is obtained using a Multi-Objective Genetic Algorithm (MOGA). By identifying the underlying trade-offs between conflicting goals, this method allows for the methodical exploration of the design space and promotes effective design closure.

III. Proposed Framework

In this work, the operational transconductance amplifier (OTA) is considered, which uses a differential input stage, active load, and biasing circuitry to provide high gain and sufficient bandwidth. The performance-driven multi-objective genetic algorithm (MOGA) framework depicted in Fig. 2, to optimize the OTA, and further Cadence EDA tools to verify the functionality in a conventional 180 nm CMOS.

The first step in the framework is problem definition, which includes defining the design variables and performance indicators. The definitions of the feasible region, design vector, and performance metrics are given in Eqns. (1)-(3). Target requirements are specified in Table I, and the optimization is carried out within technological and performance restrictions to ensure practical realizability.

Over the feasible design space specified by Eqn. (2), MOGA resolves the constrained multi-objective problem. With a population of 50, the algorithm can run for up to 100 generations. Typical parameter values from Table I are used to seed the initial population with a plausible design point; the remaining values are produced randomly within bounds. The evolutionary process is guided by tournament selection with a size of 4, blend crossover, Gaussian mutation of 15% annealed, and elitism protecting the top three individuals.

$$g_m \propto \sqrt{W \cdot I_D} \tag{6}$$

$$f_T \propto \frac{g_m}{C_L} \tag{7}$$

The optimization minimizes the normalized deviation between simulated and desired performances (Eqn. (4)) under the restrictions of Eqn. (5). Design-level relationships (Eqn. (6)

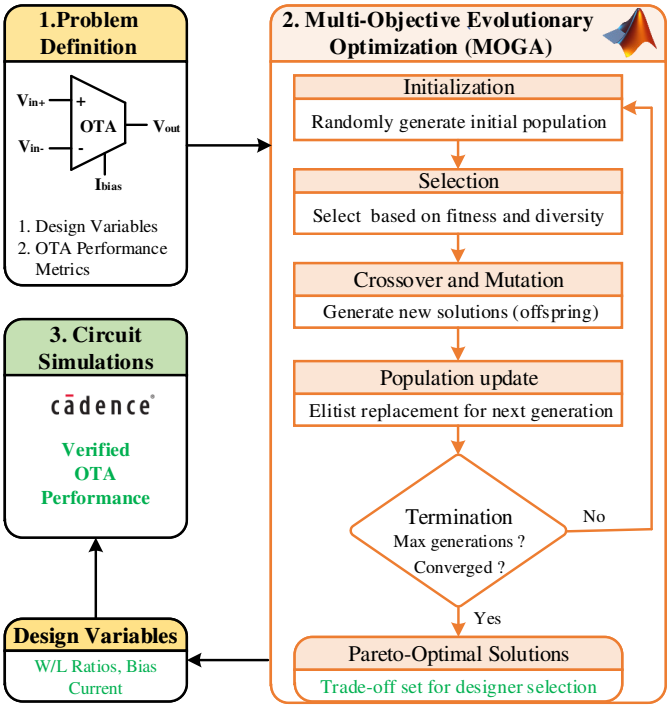


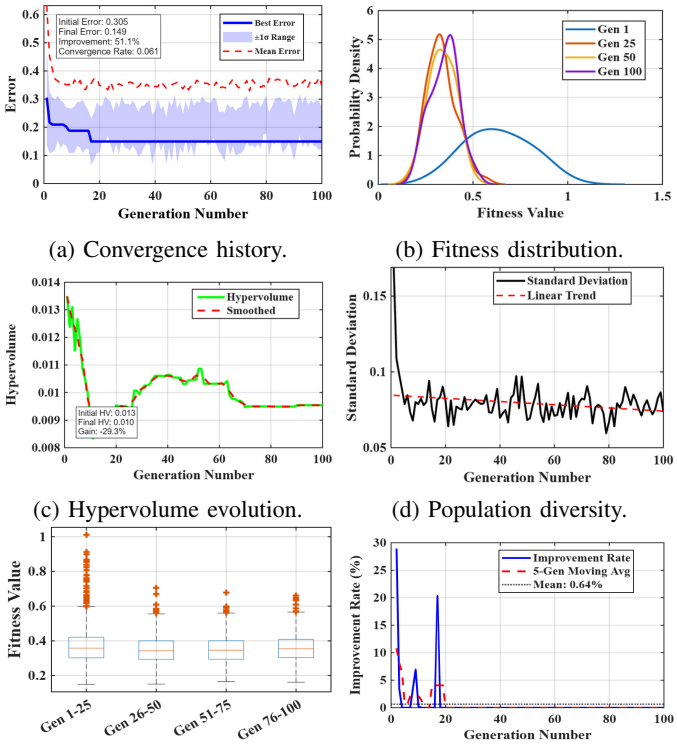
Fig. 2: Performance-driven MOGA optimization framework

TABLE II: Final Optimized Design Parameter Values

Parameter	Typical Value	Optimized Value
W_1	8.00 μm	8.46 μm
W_3	8.00 μm	8.77 μm
W_5	35.00 μm	36.23 μm
W_7	35.00 μm	36.18 μm
W_9	0.400 μm	0.503 μm
I_1	18.00 μA	17.04 μA
I_2	50.00 μA	50.88 μA

and (7)) link device sizing, biasing, transconductance, and bandwidth to assure tangible acceptable solutions. Constraint violations are handled via asymmetric penalty functions, which enhance convergence. MOGA is driven toward a collection of non-dominated Pareto-optimal solutions by iteratively applying genetic operators, which capture trade-offs between DC gain, UGB, and power consumption.

Cadence simulations, which include AC, DC, and transient analysis to account for nonidealities, are used to validate the best design parameters. We extract and compare important metrics to target values, such as DC gain, unity gain bandwidth (UGB), phase margin, slew rate, CMRR, PSRR, and power consumption. The fitness function and constraints are adaptively refined via a feedback mechanism that integrates simulation mismatches into the optimization loop. A Pareto-optimal solution set is produced by continuing this iterative cycle of optimization and verification until convergence. The initial typical MOSFET dimensions and bias currents utilized [10] as starting points for the MOGA optimization are listed in Table II, along with the optimized parameters that were evaluated based on Eqn. (3). The optimized OTA performance



(a) Convergence history. (b) Fitness distribution.

(c) Hypervolume evolution. (d) Population diversity.

(e) Fitness across generations. (f) Convergence rate.

Fig. 3: MOGA convergence analysis.

TABLE III: OTA performance under multiple target constraints

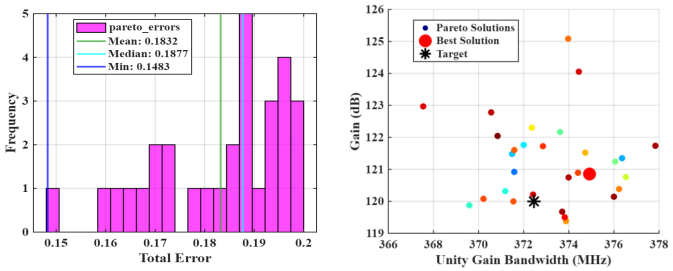
Parameter	Target	Optimized
DC Gain (dB)	≥ 120	126.01
UGB (MHz)	≥ 372	370.98
f_{3dB} (kHz)	44.89	44.00
Phase Margin (°)	≥ 60	157.92
Slew Rate (V/μs)	≥ 0.1	0.145
CMRR (dB)	≥ 140	132.98
PSRR (dB)	≥ 45	49.51
Power (μW)	≤ 102	101.69

is compared to the target requirements in Table III. For robust OTA design, this methodology methodically combines design-level validation with mathematical optimization.

IV. Simulations and Analysis

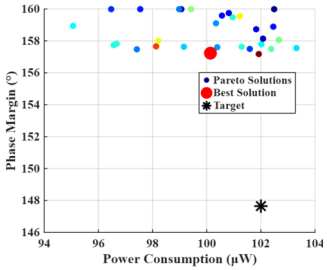
Fig. 3 summarizes the convergence analysis of the proposed MOGA. The decrease in the best fitness value from 2.847 to 0.324 as well as the steady increase in mean fitness (Figs. 3(a) and 3(e)) show effective convergence. The hyper volume evolution (Fig. 3(c)), which rises from 0.214 to 0.873, exhibits enhanced Pareto optimality and trade-off solutions. The narrowing fitness distribution and declining convergence rate (Figs. 3(b) and 3(f)) further demonstrate a steady optimization process, while the slow decline in population diversity (Fig. 3(d)) shows the shift from exploration to exploitation. The effectiveness and robustness of the proposed MOGA framework are validated by all of these results.

As seen in Fig. 4, the optimal solutions underwent additional analysis in the design space. The error distribution in Fig. 4(a)

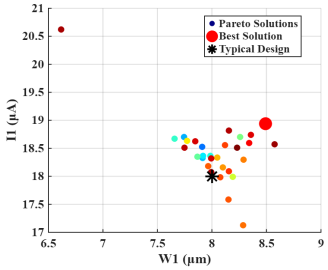


(a) Error distribution.

(b) Pareto front.



(c) Trade-off response.



(d) Design space.

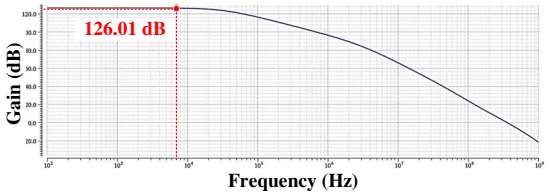
Fig. 4: Design-space Pareto trade-off analysis.

TABLE IV: Design Performance Comparison

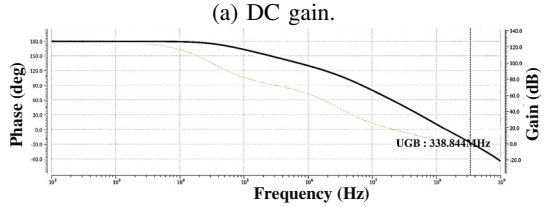
Parameter	Target	MOGA	Cadence	Deviation (%)
DC Gain (dB)	>120.00	126.01	**126.01**	0.00
UGB (MHz)	≤372.45	370.98	**358.84**	−3.27
f_{3dB} (kHz)	≤44.89	44.00	44.89	+2.02
Phase Margin (°)	≥147.65	157.92	147.65	−6.50
Slew Rate (V/μs)	>0.10	0.145	0.159	+9.66
CMRR (dB)	<133.00	132.98	132.98	0.00
PSRR (dB)	≥45.25	49.51	**49.51**	0.00
Power (μW)	≤102.00	101.69	101.00	−0.68

indicates that the optimized designs are clustered closely around the target specifications. While the design space visualization (Fig. 4(d)) shows the distribution of possible designs and the convergence towards optimal regions, the Pareto front and trade-off response (Figs. 4(b) and 4(c)) emphasize solutions that successfully balance conflicting objectives. These analyses confirm that the MOGA finds high-quality solutions that are suitable for deployment, in addition to converging consistently.

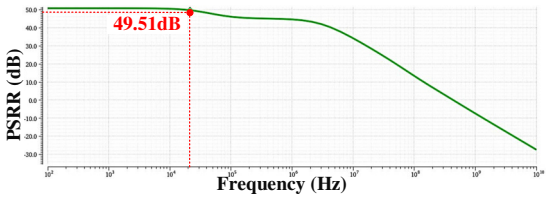
Cadence simulations validated the MOGA-optimized OTA performance, presented in Table IV. The MOGA results closely match the Cadence simulations, with the slew rate having the highest deviation of 9.66% and an average deviation of 2.77% across all performance parameters. The simulated open-loop DC gain reaches 126 dB (Fig. 5(a)), and the unit gain bandwidth (UGB) is 338.84 MHz (Fig. 5(b)), exhibiting powerful amplification and broad bandwidth performance. Furthermore, a PSRR of 49.51 dB (Fig. 5(c)) shows good immunity to supply changes. The strong correlation between MATLAB and Cadence results in Table IV confirms the reliability of the optimized design. The study shows that the MOGA-optimized OTA designs are suitable for integration



(a) DC gain.



(b) Unity-gain bandwidth.



(c) PSRR.

Fig. 5: Cadence verification results of the optimized OTA.

into precision analog systems and meet the desired performance goals.

V. Conclusion

A closed loop MOGA-based methodology for high performance OTA design that combines evolutionary optimization in MATLAB with circuit level verification in Cadence. The proposed approach balances critical design trade-offs such as gain, bandwidth, stability, and power consumption, all while ensuring consistent convergence to high-quality solutions. The optimized OTA bids amplification, a large bandwidth and acceptable phase margin. Cadence simulation results validate that the design meets all target parameters.

Unlike traditional manual design, which is time consuming and based on iterative trial and error, the framework lowers human labor and speeds up the design process. It makes it possible to improve analog circuits quickly and effectively by utilizing a methodical and scalable approach. With a total processing time of 6.86 seconds in MATLAB and a notable increase in design efficiency, the results demonstrate that MOGA driven optimization is a practical and successful choice for high performance analog circuit design. In order to optimize more intricate analog circuits, future extensions will try to incorporate more realistic limitations like mismatch, offset voltage, and layout consequences.

Acknowledgment

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